Fast Physical Models for Si LDMOS Power Transistor Characterization

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***Abstract* — A new quasi-two-dimensional (Q2D) model is described for microwave laterally diffused MOS (LDMOS) power transistors. A set of one-dimensional energy transport equations are solved across a two-dimensional cross-section in a "current-driven" form. This process-oriented nonlinear model accounts for thermal effects, avalanche breakdown and gate conduction. It accurately predicts DC and microwave characteristics as demonstrated by comparison with measured DC characteristics, transconductance, forward gain, S_{21}, and large-signal gate and drain charges for a LDMOS transistor. The model is fast, taking less than 30 ms to extract a 50 point DC I_{DS}-V_{DS} characteristic and less than 5 ms to produce *S*-parameters at a single frequency.**

***Index Terms* — Field Effect transistor (FET), laterally diffused MOS (LDMOS), quasi-two-dimensional (Q2D), transistor model.**

I. Introduction

The RF LDMOS device structure used in silicon FETs is now the dominant device technology used in high power wireless infrastructure power amplifier (PA) applications. Their highly flexible structure has delivered the superior linearity and efficiency, high gain, compatibility with low cost packaging platforms and excellent reliability required by a demanding RF power market. For example, LDMOS technologies are now achieving 73% efficiency with 23 dB gain, breakdown voltages of exceeding 110 V over 1 Watt/mm gate periphery and operating frequencies up to 3.8 GHz [1]. Fig. 1 shows an LDMOS die in a microwave power package.

Fig. 2 shows a schematic cross-section of the simplified intrinsic LDMOS transistor, which is the foundation for the physical Q2D model and simulator. A low gate access resistance, important for the large dimensions of RF power devices such as LDMOS, is provided by a WSi/polysilicon gate. The threshold voltage and turn-on characteristics of the device are established by a boron doped p-channel (PHV) and a low doped arsenic n-type drift (NHV) region is designed to support high breakdown voltages, $V_{BR,}$ low on-state resistance, $R_{ds(on)}$, and good Hot Carrier Injection (HCI) reliability.

A tradeoff between V_{BR} and $R_{ds(on)}$ complicates LDMOS device optimization since a decrease in NHV concentration reduces both parameters. Reduced Surface Field (RESURF) structures minimize this issue and analytical studies of multi-RESURF structures show that a 23% reduction in $R_{ds(on)}$ can be achieved without any degradation in V_{BR} [2]. RESURF techniques also help mitigate high field avalanche breakdown

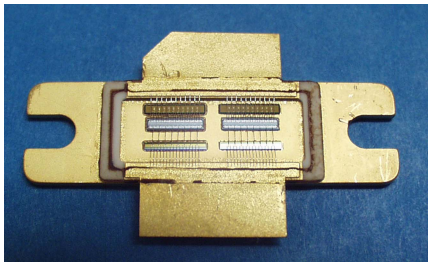

Fig. 1. Photograph of LDMOS microwave transistor (*courtesy of Freescale Semiconductor, Inc.*).

mechanisms in the drift region that result in high gate current and eventual burnout [3][4].

The transconductance, g_m, is related to the forward gain S_{21} and high and wide values for the former can be achieved via a reduction in drift resistance, which in turn enhances the device's high frequency performance [5]. Furthermore, a high transconductance in the saturation regime ensures good linearity since the device characteristic is approximately linear about the operating point in saturation.

A quasi-two-dimensional (Q2D) modeling approach, used successfully to model compound semiconductor microwave MESFETs and HEMTs [6]-[9], achieves the simplicity, speed and robustness of physical compact models, while providing an accurate model by taking into account the most important physical phenomena occurring in the device. The two main existing approaches to modeling the intrinsic LDMOS transistor are both based on the drift-diffusion approximation (neglecting hot carriers) and centered on either the inversion-charge (IC) or surface-potential (SP) of the MOSFET channel.

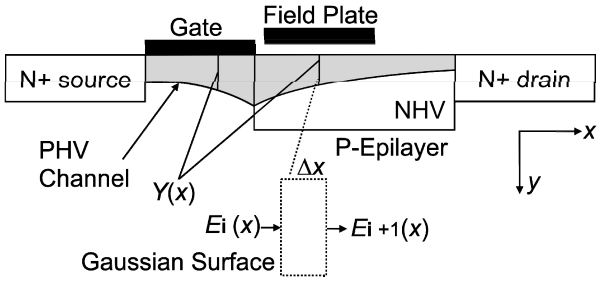

Fig. 2. Domain and structure of Q2D the model for the intrinsic LDMOS transistor. The area shaded light grey represents the active channel.

Here, the drain current and terminal charges are indirect functions of the terminal voltages through either the surface potential or the inversion charge density. In recent years it is the former approach that has taken lead position [10].

A new Q2D time-domain transport formulation, accounting for displacement current, is described here and the microwave performance of the LDMOS device is characterized using a multi frequency extraction scheme. An important advantage of the Q2D approach to the nonlinear modeling of LDMOS is that it directly relates physical device structure to DC, RF and microwave parameters, and allows accurate predictive transistor modeling. The algorithm is extremely fast, able to evaluate a 50 point DC I_{DS}-V_{DS} characteristic in less than 30 ms and *S*-parameters at a single frequency in less than 5 ms, on a core i7 PC. This is 1000s of times faster than commercially available full 2D device simulators, which makes it fast enough for use in circuit simulation software.

II. The Quasi-two Dimensional Physical LDMOS Simulator

A. Basic Assumptions

The intrinsic transistor is modeled as a series PHV-NHV network where the former region is treated as a short channel ideal MOSFET and the latter a series combination of the n-side space charge and quasi-neutral (QN) regions of a reverse biased p+/n diode. Essentially, the nonlinear Q2D model assumes that the electric field in the active channel region is one-dimensional (1D) while retaining a sufficiently accurate 2D physical description of the conduction channel. Under these assumptions, and application of Gauss' law to an incremental volume with uniform cross-sectional area defined by the Gaussian surface shown in Fig. 1, one can reduce the 2D Poisson equation to 1D slices

$$\left[E_i(x)-E_{i-1}(x)\right]Y_i(x)=\frac{q\Delta x}{\varepsilon_{Si}}\left[N_i(x)-n_i(x)\right], \qquad (1)$$

where *E(x)* is the lateral component of electric field, subscript *i* represents the step at each incremental length of conduction channel Δx, ε_{Si} is the silicon permittivity, $Y(x)$ is the total active channel height, $n(x)$ is the carrier density and $N(x)$ the effective doping density, which is a function of the doping density in the *y* direction. To obtain the drain-to-source voltage, V_{DS}, this is then solved self-consistently with a simplified 1D solution of the hot electron equations in a "current-driven" form, where the static drain-to-source current through the device, I_{DS}, is assumed constant; note that from here *i* subscripts are mostly omitted for clarity.

B. Transport Model

The current impressed at the source terminal, I_S, is given by

$$I_S=ZY(x)\left[qn(x)v(x)+\varepsilon_{Si}\frac{\partial E(x)}{\partial t}\right]+\frac{\partial Q_g(x)}{\partial t}, \qquad (2)$$

where *Z* is the device width. Note that the first term in (2) is the instantaneous channel current and the second term is the displacement current due to the gate charge $Q_g(x)$. Gate leakage current is ignored as the conductive component of the intrinsic gate current is negligible in LDMOS [1]. The conductive channel height in the PHV region is determined by

$$Y(x)=Q_{inv}(x)/qN_A(x). \qquad (3)$$

The lateral electric field is the driving force for the reverse saturation drift current, where the PHV inversion channel charge per unit gate area responsible for current conduction, $Q_{\text{inv}}(x)$, is based on the charge sheet model [11] and given by

$$\begin{aligned}\left|Q_{inv}(x)\right| &= \left[V_{GS}-\varphi_S(x)\right]C_{ox}-\sqrt{2\varepsilon_{Si}qN_A(x)\varphi_S(x)}\\ &= C_{ox}\left[V_{GS}-(V_T(x)-V(x))\right]\end{aligned}. \qquad (4)$$

Here, $\varphi_S(x)$ is the surface potential, $N_A(x)$ is the acceptor impurity density of the p-type (boron-doped) silicon, V_{GS} is the gate-to-source voltage, $V_T(x)$ is the threshold voltage, $V(x)$ is the channel potential and C_{ox} is the oxide capacitance per unit area equivalent to ε_{ox}/d_{ox}, where ε_{ox} and d_{ox} are the gate oxide permittivity and thickness respectively.

Assuming no current flows within vertical space charge regions associated with the field plate and reverse biased NHV/P-Epilayer boundary, $w_{FP}(x)$ [12] and $w_{Vert}(x)$ [13] respectively, the effective cross-sectional area of lateral current flow is $ZY(x)$ where the active channel height is

$$Y(x)=d_{NHV}-w_{Vert}(x)-w_{FP}(x) \qquad (5)$$

for $x \le L_{FP}$. Here, L_{FP} is the length of the field plate and d_{NHV} is the NHV depth, which is assumed constant along its length.

Rearrangement of (2), the current continuity equation, and Gauss equation produces a quadratic in, $E(x)$, where one of the roots is positive and used to obtain the channel electric field [7]. This is then solved together with a simplified equation for average electron energy, ω, given by

$$\frac{\partial\omega}{\partial x}=\frac{q}{20}\left(21E(x)-3\sqrt{\left(40{E_{SS}}^2(x)+9E^2(x)\right)}\right), \qquad (6)$$

where $E_{ss}(x)$ is the measured steady state electric field [14].

An avalanche breakdown model for conduction channel breakdown is incorporated in the simulation, where the impact ionization current, I_{avl}, is expressed in terms of multiplication factor, *M*:

$$I_{avl}=(M-1)I_{DS}=\int_0^{L_{PHV+NHV}}\alpha\,dx-1. \qquad (7)$$

The ionization rate, α, is evaluated using the function

$$\alpha = A \exp\left(-\frac{Eii}{E(x)}\right) \tag{8}$$

where $A = 2.45 \times 10^{-6}$ cm^{-1} and $E_{ii} = 1.92 \times 10^{6}$ V/cm have been determined for electrons at the silicon surface [15].

Thermal effects are modeled using a method similar to that previously published for Q2D simulations [16], and a simplified approach uses the average channel temperature T_C rise, mean thermal resistance R_{TH} and ambient temperature T_0:

$$T_C = V_{DS} I_{DS} R_{TH} + T_0 . \tag{9}$$

C. Physical Simulation Algorithm

The simulation proceeds by solving the discretized model equations over the simulation domain, extending from the edge of the source contact to the edge of the drain contact, for given instantaneous values of I_S and V_{GS}. To determine the initial electric field at the source end of the PHV channel, $E(x = 0)$, the current continuity equation is used under the assumption that electrons are cool ($v = \mu E$) in the low field region. At each mesh point, the model variables including the channel charge and conductive channel height are calculated and the steady state electric field, which is a function of average electron energy, $w(x)$, is obtained from curve fits to Monte Carlo simulation data [17]. The channel electric field then is calculated by solving a discretized version of the coupled current continuity and Gauss equation, and this is numerically integrated to obtain its corresponding channel potential:

$$V_i(x) = V_{i-1}(x) + E_{i-1}(x)\Delta x . \tag{10}$$

This procedure is implemented at each mesh point until the PHV/NHV boundary is reached. The outputs are used as boundary conditions for the NHV simulation, which is implemented in a similar way to that of the PHV channel but here the conductive channel height is obtained from (5). Thus the Q2D algorithm gives access to the DC characteristics in a "current-driven" form, where V_{DS} is the channel potential at the source for given instantaneous values of I_{DS} and V_{GS}.

A physics based small-signal characterization of the device is obtained using a previously reported multi-frequency *S*-parameter extraction scheme [7]. This is a two-stage process that utilizes short- and open-circuit terminations and makes use of V_{GS} and I_S as independent variables, and the gate current and I_{DS} as dependent variables. Frequency dependent admittance parameters of the intrinsic device are produced, to which parasitic impedances are added so that corresponding *S*-parameters are obtained by conversion formulas. The time-domain LDMOS simulation can also be applied to large-signal simulation by embedding the device model in a suitable circuit simulator. Alternatively, the quasi static equivalent circuit model can be extracted from the physical simulation and used in a modified harmonic balance simulation as in [18].

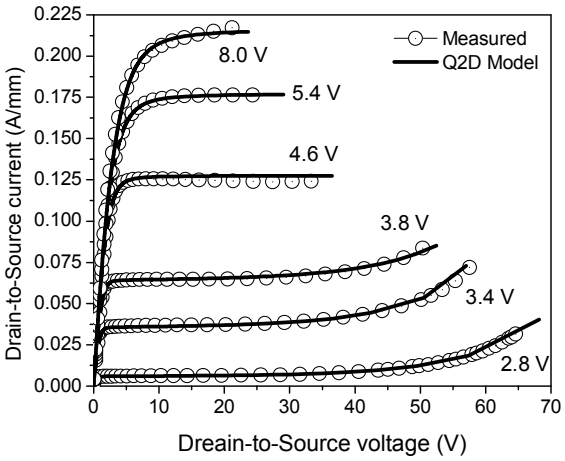

Fig. 3. Comparison between measured and simulated DC characteristics of a 4.8 mm intrinsic LDMOS transistor.

III. Device Characteristics

The Q2D simulator has been used to characterize a 4.8 mm intrinsic LDMOS transistor and Fig. 3 shows good agreement between measured and simulated data over a wide range of gate biases; the simulated data were produced using physical data and no fitting of parameters or measured data. Isothermal DC measurement data were referenced to the intrinsic device plane by de-embedding the extrinsic resistances from raw data taken at the measurement plane and the measured and simulated data are scaled to match the gate periphery.

Fig. 4 compares the measured and modeled DC transconductance for the same transistor, further demonstrating that our Q2D model for LDMOS provides an accurate description of the intrinsic LDMOS DC characteristics over a wide range of bias conditions. The simulated and measured forward transmission coefficient (gain), S_{21}, are compared in Fig. 5, showing that the magnitudes are in very good agreement; the phase data agree less well and the model is being refined to address this. Finally, Fig. 6 demonstrates good agreement between the conservative gate and drain charges, obtained through a large-signal Root model extraction from intrinsic measured data [1], and Q2D modeled data.

IV. Conclusion

We have described a new Q2D physical model, which has been applied to a 4.8 mm LDMOS transistor and shows good agreement in both DC and microwave simulations over a wide range of bias conditions. The model facilitates accurate and predictive LDMOS transistor nonlinear modeling, sufficiently fast for circuit simulation applications, and is applicable to the large-signal simulation of LDMOS transistors for microwave power amplifier applications and for process-oriented optimization of LDMOS power devices.

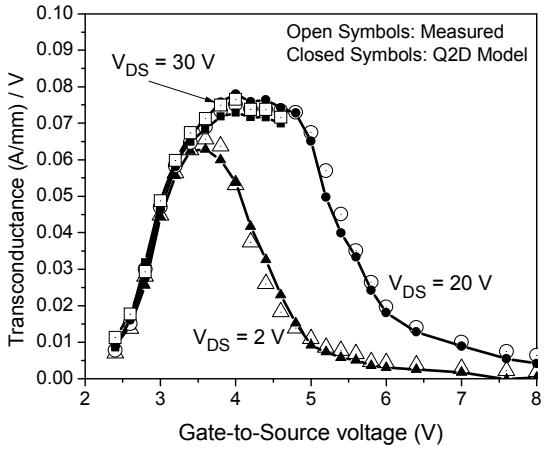

Fig. 4. Comparison between measured and modeled de-embedded DC transconductance of a 4.8 mm intrinsic LDMOS transistor.

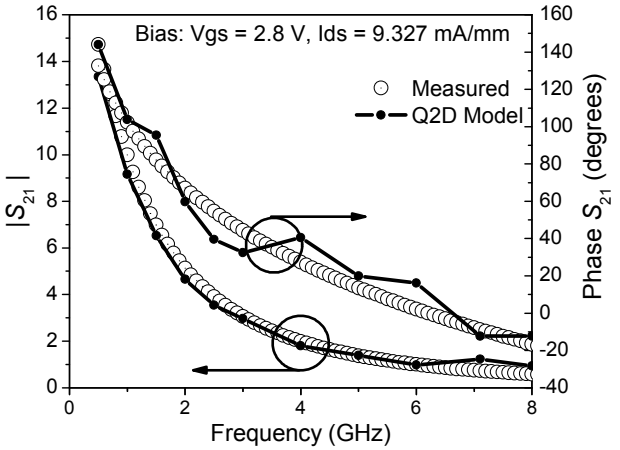

Fig. 5. Measured and modeled de-embedded forward transmission coefficient, $S_{21,}$ of a 4.8 mm intrinsic LDMOS transistor.

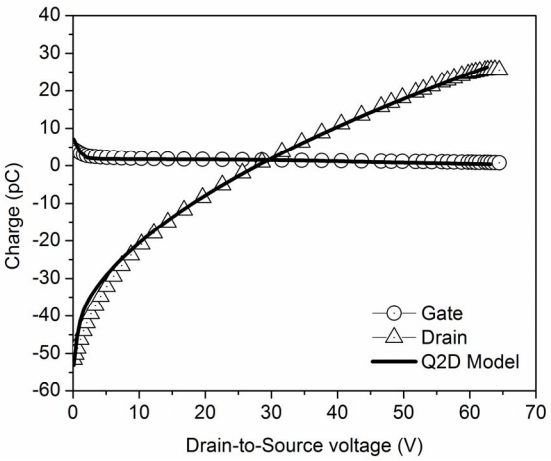

Fig. 6. Measured and modeled gate and drain charges verses drain-to-source voltage for 2 GHz and a gate voltage equal to 2.8 V.

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