Published in in *Materials Research Society Symposium Proceedings*, 2011, pp. 69-74

Solution Processable Nanowire Field-Effect Transistors

Charles Opoku[1], Lichun Chen[2], Frank Meyer[2], Maxim Shkunov[1]

[1]Advanced Technology Institute, University of Surrey, Guildford, GU2 7HX, UK
[2]Merck Chemicals, Chilworth Technical Centre, Southampton, SO16 7QD, UK

ABSTRACT

Hybrid field-effect-transistors (FETs) with germanium nanowire (NW) arrays and organic gate dielectric are presented. The nanowire deposition steps are fully compatible with printed electronics route. NW FETs demonstrate good performance with On/Off ratios of ~10^3 and hole mobilities of ~13 cm^2/Vs in both nitrogen and air atmosphere. These results suggest that the hybrid nanowire FETs could be used in large area inexpensive electronics.

INTRODUCTION

Fabrication of field-effect transistors using semiconducting 'inks' at low temperatures and on a large area substrates could potentially give rise to low-cost and disposable electronics that can also be lightweight and flexible if produced on plastics substrates. The solution processability of such devices is making them even more attractive since they can be printed without the need for high vacuum techniques and energy-demanding high temperature fabrication steps.

Recently a number of principle approaches including organic semiconductors [1], amorphous silicon (a-Si) [2], solution processable semiconducting oxides[3, 4], and semiconducting carbon nanotubes[5] have been undertaken for large area printable, flexible transistors. All of them had some challenges, hampering their applications for high-performance solution-processable printable transistors, either due to mobility limitations of about 1 cm^2/Vs (organics and a-Si) or high temperature processing (oxides) and purification drawbacks (single wall carbon nanotubes).

Semiconducting nanowire materials are offering a potential breakthrough in the area of high performance printable transistors. Inorganic nanowires maintain most of the bulk single crystal properties, including semiconducting behavior, crystal lattice structure, and efficient charge transport irrespective of nanowire diameter. The synthesis of nanowires can be completely separated from device fabrication thus allowing two-fold advantage. Firstly, controlled growth of nanowires can be tailored to produce high-quality single-crystal structures with a desired length-to-width ratio; secondly, these nanomaterials may be formulated into 'inks' for selective low-temperature additive deposition on substrates. If the alignment of these nanowires upon deposition can be controlled to 'bridge' device electrodes, then device performance per nanowire is expected to be comparable to that of traditional single-crystal semiconductor technology. Clear advantages of nanowire approach are the ease of processing, wide prospects for self-assembly 'bottom-up' fabrication, compatibility with plastic substrates, and also possibility for fast device prototyping based on additive printing technology.

Currently there have been no reports on using single crystalline germanium nanowire arrays for top-gate configuration FETs, despite the fact that Ge has very high 'bulk' electron and hole mobilities (~3900cm^2/Vs, 1900 cm^2/Vs respectively)[6], and thus offers excellent opportunities for high performance FETs.

In this work we demonstrate solution-processable Ge nanowire-array-based FETs with a top-gate spin-on amorphous fluoropolymer gate dielectric.

EXPERIMENTAL

Ge nanowires used in this work were synthesized via a gold nanocrystal-seeded supercritical fluid-liquid-solid (SFLS) method[7, 8]. Ge NW array FETs were fabricated by transferring solution-suspended Ge nanowires (~0.3mg/ml in isopropanol) onto clean glass substrates, resulting in randomly orientated NWs with coverage densities of ~ 0.2 NWs/µm^2. Electrical contacts to the Ge NW arrays were produced with standard photolithography to achieve ~100-150 nm thick chromium source/drain electrodes, as shown in Figure 1. After contact deposition step, FET structures were oxygen plasma etched to remove residual photoresist, and ~ 1µm thick Cytop™ (Asahi Glass) film was deposited by spin-coating. Devices were finished by shadow-mask deposition of ~50 nm gold gate electrode on top of polymer dielectric layer.

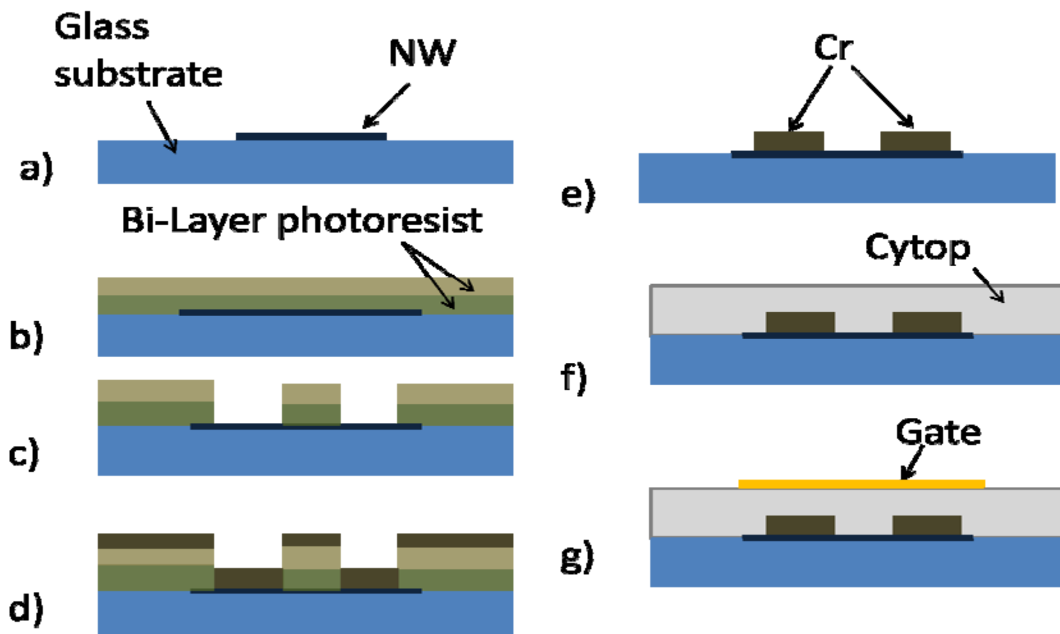

Figure 1 Fabrication steps of a multiple Ge nanowire FET. (a-b) Ge NWs are solution cast onto a cleaned glass substrate, followed by spin coating a bi-layer photoresist (PMGI-SF6 from MichroChem Corp, followed by S1805 from Rohm and Haas electronic materials). (c) Substrates are exposed to UV through a photo-mask, and developed in a resist developer. (d-e) 100 to150nm thick Cr layer is sputtered over entire substrate and lift-off process is conducted in acetone to define the source/drain contacts. (f-g) Cytop™ is spin coated onto substrates to achieve a ~1µm thick film. This is then followed by the evaporation of ~50nm Au gate electrode.

RESULTS AND DISCUSSION

I-V characteristics were obtained in N_2 atmosphere and in ambient air after 24-hour exposure using a semiconductor characterization system (Agilent4142b). In all cases, the hybrid Ge NW array FETs exhibited p-type accumulation regime, consistent with previous reports on Ge nanowires synthesized by the SFLS method[7, 9].

For the FET devices measured in N_2 atmosphere (Figure 2), a threshold voltage (V_T) and device on/off ratio were extracted to be ~12V and 10^3 respectively. V_T was found by fitting a straight line to the linear sections of the transfer characteristics. The attained on/off ratio was found to be consistent with Ge NW based FETs in the literature[10]. The on/off ratio can be considered as the amplification factor of the Ge NWs conductance in response to an electric field, extracted by the logarithmic ratio of the maximum current (I_{max}) and the minimum current (I_{min}), expressed as $log_{10}(I_{max}/I_{min})$. In N_2 atmosphere a sub-threshold swing s (where $s = \Delta V_g/[log_{10}(I_{max}/I_{min})]$ of ~ 8V/dec is calculated for a V_g range between +20V and +10V. In this work, s value attained for the hybrid FETs is some 60 times larger than the best reported for bulk Ge FETs[10], and 15 times worse than the best reported data for Ge NW FETs with multiple nanowires as the semiconducting channel[11]. It is anticipated that further enhancement in sub-threshold swing can be achieved by adopting a thinner gate dielectric layer.

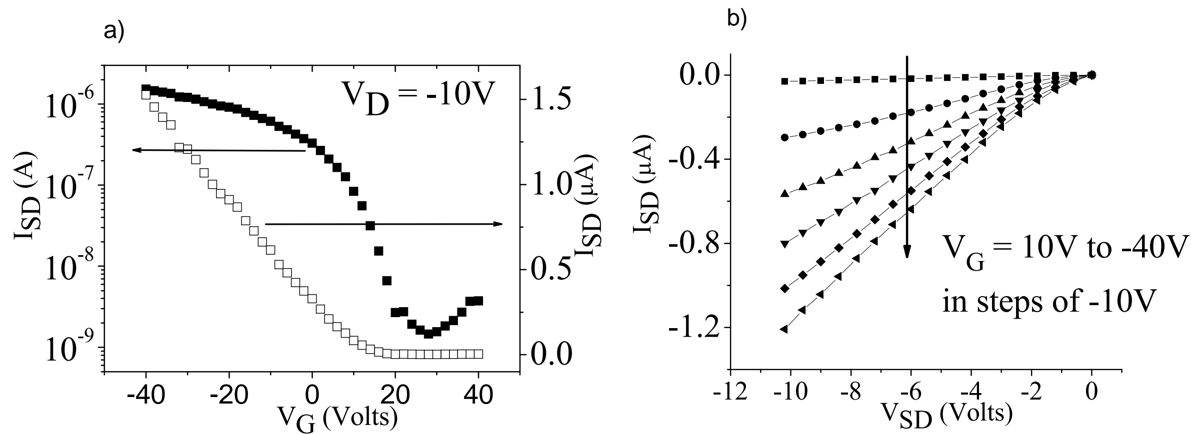

Figure 2 Transfer (a) and output (b) characteristics for the top-gate Ge nanowire-array FET measured in dry nitrogen atmosphere.

The same FET devices were re-measured in air (Figure 3), and parameters were extracted in a similar manner. Device on/off ratio was close to 10^3, and threshold voltage V_T was found to be ~9V, which is only 3V deviation from that obtained in the N_2 atmosphere, which demonstrates good device ambient stability. Sub-threshold swing s was estimated to be 9V/dec.

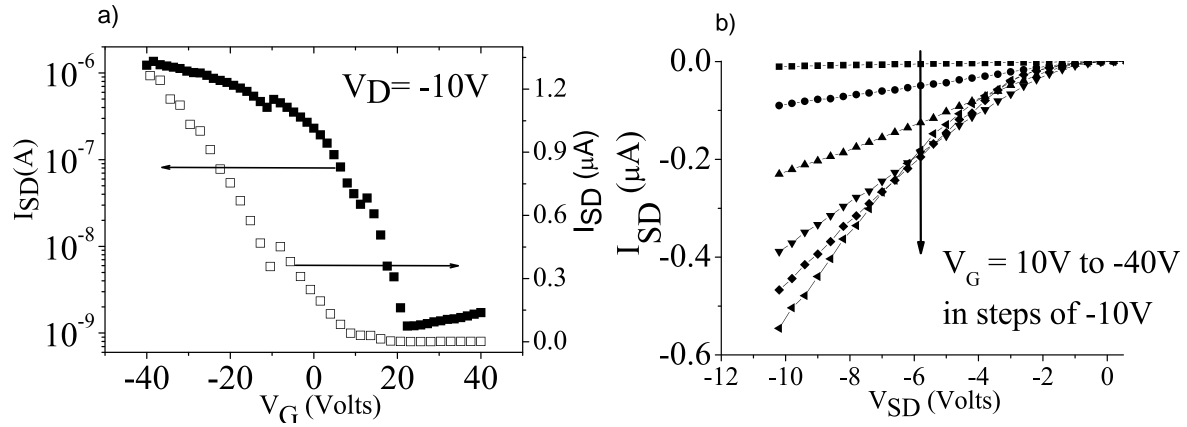

Figure 3 Transfer (a) and output (b) characteristics for the top-gate Ge nanowire-array FET measured in ambient air after 24h exposure.

Another important parameter, device transconductance (g_m), was estimated from transfer characteristics using equation $gm = dI_d/dV_g$. In both nitrogen and air atmosphere, the *gm* value was found to be ~0.04μS. Considering 3 NWs (each having an average diameter ~100 nm) representing the channel, we estimated the effective channel width to be 0.3μm, using $W_{\mathrm{eff}} = Nd$. Where *N* is the number of NWs in the channel, and *d* is the average diameter. Using W_{eff}, we calculated a normalized *gm* (as per transistor width) of ~0.1μS/μm. The normalized g*m* attained here was found to be considerably higher than what was expected for a-Si (~0.01 μS/μm), but comparable to poly-Si (0.2-0.8 μS/μm)[11].

With the extracted *gm* of ~0.04μS, the effective carrier mobility (μ_p) was then calculated using the following approach.
The capacitance (C_i) of three nanowires in FET channel was deduced by modifying the cylinder on plate model, which is often used to determine coupling capacitance in single NW FETs. C_i was estimated as ~0.3 fF, where $C_i = N.2\pi\varepsilon_o\varepsilon_r.L/(cosh^{-1}[(r+h)/r]$ [11-13]. ε_o is the relative permittivity, ε_r is the dielectric constant of the Cytop (~2.2)[14]. *L* is device channel length (~10μm), *r* is the average radii per NW (~50nm), and *h* is the Cytop film thickness (~1μm). Hole mobility (μ_p) was determined to be ~13 cm^2/Vs using equation $\mu_p=gm\times L^2/(V_d\times C_i)$.

Evidently, the hole mobility attained in this work is significantly lower than the theoretical limit predicted for Ge. Such drastic reduction in mobility may be attributed to surface scattering of carriers as a result of the large surface to volume ratio of Ge NWs and also high density of surface trap states, caused by amorphous surface oxide layers and adsorbed ambient species, such as polar water molecules [15, 16].
Nevertheless, a mobility of 13 cm^2/Vs is promising because; firstly, it exceeds a value of 2 cm^2/Vs obtained previously for SFLS grown germanium nanowires[17] and secondly, a much thinner gate dielectric layer would allow for enhanced gate coupling to the NWs, thus enhancing carrier mobility as well as the sub-threshold slope. An example of such enhancement for metal oxide nanowires has already been demonstrated with nano-self-assembled dielectrics [18].

The hole mobility attained for our device is still higher than what is routinely achieved in a-Si and amorphous organic semiconductors (~1cm^2/Vs and ~ 0.1cm^2/Vs respectively) [19, 20]. We

note that our hybrid FETs exhibit significant contact resistance when Cr is used as the source and drain electrodes, and this is apparent from the nonlinear current trace in the output scans at low S-D voltage in Figures 2(b) and 3(b). We also point out that the multiple Ge FETs made in this way exhibit significant hysteresis in the transfer scans (not shown here), which thought to be caused by the existence of surface states on Ge NWs. This hysteresis effect was stronger for the devices measured in air, and resulted in a more pronounced threshold voltage shift and consequently lower maximum current values in the output scans shown in Figure 3(b) compared to the transfer scan current values in Figure 3 (a). The exact nature of the trap states causing hysteresis and methods to remove/passivate them are beyond the scope of this paper.

CONCLUSIONS

In summary, single crystalline Ge NWs and a polymeric dielectric were used to construct a hybrid FET on glass. The fabrication process undertaken for such FETs shows good compatibility with low temperature processing techniques. FET mobility of 13 cm^2/Vs was realized in nitrogen atmosphere and in ambient air, and demonstrated good stability. This approach of using a polymeric insulator and inorganic Ge NW arrays opens the possibility for high performance FETs that are compatible with printing technologies for low cost device assembly.

REFERENCES

[1] A. Dodabalapur, "Organic and polymer transistors for electronics," *Materials Today,* vol. 9, pp. 24-30, 2006.

[2] C. Hilsum, "Flat-panel electronic displays: a triumph of physics, chemistry and engineering," *Philosophical Transactions of the Royal Society Mathematical Physical and Engineering Sciences,* vol. 368, p. 1027, 2009.

[3] S. K. Park, Y.-H. Kim, H.-S. Kim, and J.-I. Han, "High Performance Solution-Processed and Lithographically Patterned Zinc-Tin Oxide Thin-Film Transistors with Good Operational Stability," *Electrochem. Solid-State Lett. ,* vol. 12, p. H256, 2009.

[4] H. Faber, M. Burkhardt, A. Jedaa, D. Kaelblein, H. Klauk, and M. Halik, "Low-Temperature Solution-Processed Memory Transistors Based on Zinc Oxide Nanoparticles," *Adv. Mater.,* vol. 21, pp. 3099-3104, 2009.

[5] Q. Cao and J. A. Rogers, "Ultrathin Films of Single-Walled Carbon Nanotubes for Electronics and Sensors: A Review of Fundamental and Applied Aspects," *Adv. Mater.,* vol. 21, p. 29, 2009.

[6] S. M. Sze, *Physics of semiconductor devices*: Hoboken, N.J. : Wiley-Interscience, 2007

[7] T. Hanrath and B. A. Korgel, "Nucleation and Growth of Germanium Nanowires Seeded by Organic Monolayer-Coated Gold Nanocrystals," *JACS,* vol. 124, pp. 1424-1429, 2002.

[8] T. Hanrath and B. A. Korgel, "Supercritical Fluid–Liquid–Solid (SFLS) Synthesis of Si and Ge Nanowires Seeded by Colloidal Metal Nanocrystals," *Adv. Mater.,* vol. 15, pp. 437-440, 2003.

[9] T. Hanrath and B. A. Korgel, "Chemical surface passivation of Ge nanowires," *JACS,* vol. 126, p. 15466, 2004.

[10] D. Wang, Q. Wang, A. Javey, R. Tu, H. Dai, H. Kim, P. C. McIntyre, T. Krishnamohan, and K. C. Saraswat, "Germanium nanowire field-effect transistors with SiO and high-kappa HfO gate dielectrics," *Appl. Phys. Lett.,* vol. 83, pp. 2432-2434, 2003.

[11] X. Duan, C. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles, and J. L. Goldman, "High-performance thin-film transistors using semiconductor nanowires and nanoribbons," *NATURE,* vol. 425, pp. 274-278, 2003.

[12] W. Lu, P. Xie, and C. M. Lieber, "Nanowire Transistor Performance Limits and Applications," *IEEE TRANSACTIONS ON ELECTRON DEVICES,* vol. 55, pp. 2859-2876, 2008.

[13] D. Kim, Y.-K. Park, S. C. Ha, J. S. Huh, J. Na, J. Kim, and Gyu-Tae, "Photoconductance of aligned SnO2 nanowire field effect transistors," *Appl. Phys. Lett.*, vol. 95, pp. 043107 1-3, 2009.

[14] W. L. Kalb, T. Mathis, S. Haas, A. F. Stassen, and B. Batlogg, "Organic small molecule field-effect transistors with CytopTM gate dielectric: eliminating gate bias stress effects," *Appl. Phys. Lett.*, vol. 90, p. 092104, 2007.

[15] B. A. Korgel and T. Hanrath, "Influence of Surface States on Electron Transport through Intrinsic Ge Nanowires," *J. Phys. Chem. B,* vol. 109, p. 5518, 2005.

[16] D. Wang, Y.-L. Chang, Q. Wang, J. Cao, D. B. Farmer, R. G. Gordon, and H. Dai, "Surface Chemistry and Electrical Properties of Germanium Nanowires," *JACS,* vol. 126, p. 11602, 2004.

[17] A. D. Schricker, S. V. Joshi, T. Hanrath, S. K. Banerjee, and B. A. Korgel, "Temperature dependence of the field effect mobility of solution-grown germanium nanowires," *J. Phys. Chem. B,* vol. 110, p. 6816, 2006.

[18] J. Sanghyun, I. Fumiaki, C. Pochiang, C. Hsiao-Kang, Z. Chongwu, H. Young-geun, L. Jun, F. Antonio, J. M. Tobin, and B. J. David, "High performance InO nanowire transistors using organic gate nanodielectrics," *Appl. Phys. Lett.,* vol. 92, p. 222105, 2008.

[19] C. D. Dimitrakopoulos and P. R. L. Malenfant, "Organic Thin Film Transistors for Large Area Electronics," *Adv. Mater.,* vol. 2, 2002.

[20] A. Kuo, T. K. Won, and J. Kanicki, "Advanced Amorphous Silicon Thin-Film Transistors for AM-OLEDs," *IEEE Transactions,* vol. 55, 2008.