Understanding, Modeling and Optimizing Vacancy Engineering for Stable Highly Boron-Doped Ultrashallow Junctions

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Abstract

This work presents breakthrough results on the physics, modeling and application of ion-implanted vacancies for high-performance B-doped ultrashallow junctions. We demonstrate for the first time electrically active B concentrations approaching 10^{21}/cm^3, achieved by low-temperature annealing, without preamorphisation. Source/drain (S/D) junctions formed by advanced vacancy engineering implants (VEI) are activated far above solubility, are stable with respect to deactivation, and are practically diffusionless. Furthermore sheet resistance R_s is predicted to stay almost constant with decreasing junction depth X_j, outperforming other S/D engineering approaches beyond the 45 nm node.

Introduction

Conventional approaches to PMOS source-drain formation use preamorphisation via the 'SPER' method or high temperature short-time processes (Flash/sub-melt laser, etc). These methods form end-of-range defects which contribute to junction leakage and drive deactivation and transient enhanced diffusion during subsequent thermal steps. These difficulties have to be combated with additional measures which add complexity. Furthermore electrical activation is limited to the solid solubility in amorphous silicon at the processing temperature, thus pushing industry towards more expensive flash/laser options as junction depths are scaled down.

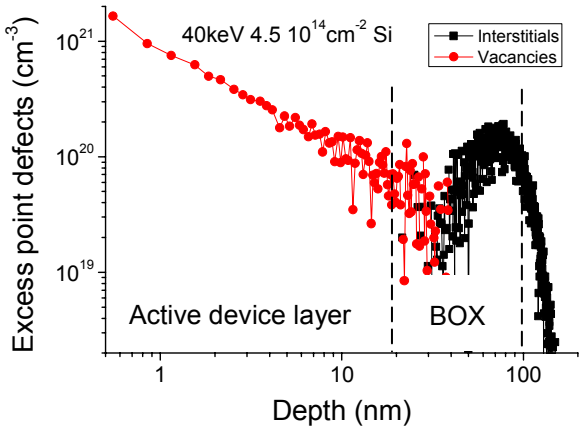

Fig. 1: Monte Carlo-simulated depth profiles of excess V and Si_i produced by a 40keV Si implant. A barrier to Si_i, e.g. a SOI BOX oxide (vertical lines) excludes Si_i from the active device layer

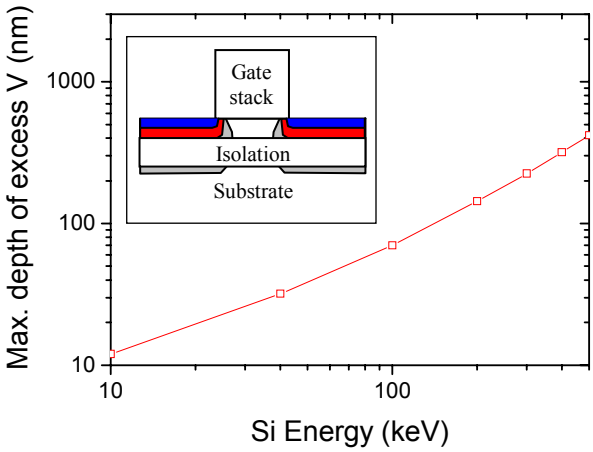

Fig. 2: Depth of transition from excess V to excess Si_i, versus energy. Inset schematic shows section thru implanted SOI MOS structure: B-doped region -blue, V-rich region -red, Si_i-rich region - gray.

In the vacancy engineering approach, B is implanted into crystalline silicon that has been prepared with a high concentration of excess vacancies by a co-implant process. The concept has been known for a number of years (1-3) but up to now has not yielded the level of B activation needed for PMOS source-drains or extensions. The key to *advanced* VEI, proposed here, lies in two features. First, it is applied to semiconductor layers, e.g. SOI, which have finite thickness, the co-implant conditions being chosen to generate an excess vacancy profile $V(x)$ throughout the layer under the implant window.

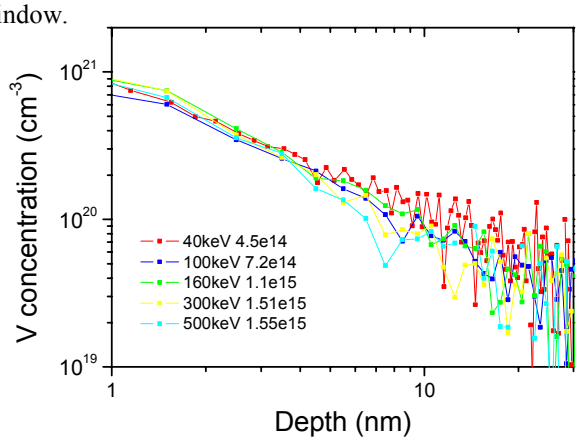

Fig. 3: Excess V distributions for different Si energies. The doses are scaled to overlay the concentration profiles. The results match the approximate curve $V(x)=10^{21}\text{cm}^{-3}/x(\text{nm})$.

0-7803-9269-8/05/$20.00 (c) 2005 IEEE

Second, the co-implant species and dose/energy combination is chosen to generate an excess vacancy concentration that is very high close to the surface, profiled to match the shape of the implant that is to be activated, but without amorphising the semiconductor crystal in the B implanted volume. Whilst some elements of advanced VEI have been discussed and exploited in earlier work (2,4), this is the first time that all of the key elements have been fully understood and synergistically applied together.

Modeling the implanted vacancy profile

Figs. 1-4 show results of Monte Carlo simulations for the case of Si co-implants, indicating that the criteria set out in the introduction can be met over a broad range of dose/energy conditions. Figs. 1 and 3 show how the excess vacancy concentration starts from a very high value close to the entry surface, and falls approximately inversely with depth. At a characteristic depth the excess point defect switches from the vacancy to the interstitial, but by a suitable choice of implant energy this transition depth can be placed beneath the silicon top layer, either in the BOX oxide or the silicon below it. Fig. 2 shows how this transition depth varies with implanted ion energy, for the case of Si implantation.

The rapid rise in *V(x)* towards the entry surface of the co-implantation ion beam is well represented and explained by a simple analytical model that neglects (what turn out to be) small effects arising from beam energy loss, sputtering and secondary recoils. The main contribution to *V(x)* in this near-surface region is an integral representing the 'missing' primary recoils that *would have arrived* at depth *x*, *had the silicon crystal extended indefinitely* above the actual silicon surface (Fig. 5). This key point does not appear to have been discussed in the published literature up to now. It means that VEI is potentially very well suited to future down-scaling of source-drain dimensions, because a reduction in source-drain depth places the dopant in a region of higher vacancy concentration.

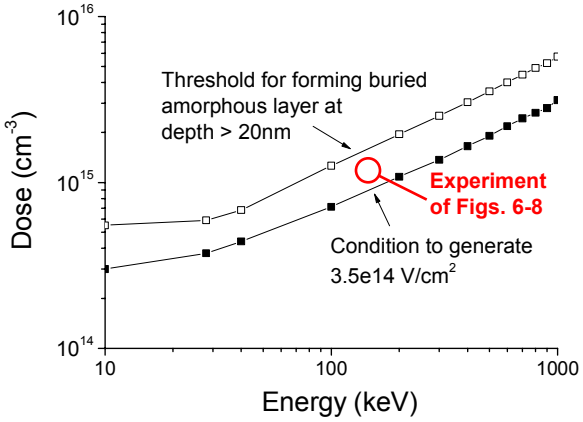

Fig. 4: Approximate operating range for V engineering with Si ions, lying between an upper limit determined by amorphisation and a lower limit where too few V are generated.

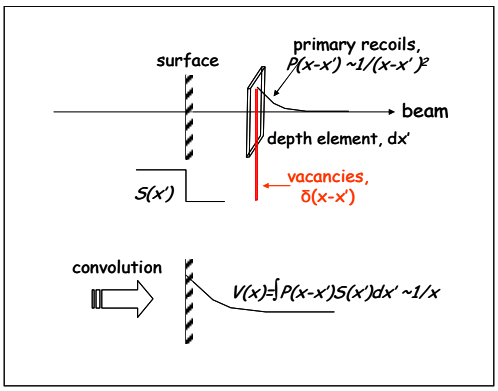

Fig. 5: Analytical model sheds light on steepness of the near-surface vacancy depth profile *V(x)*. Neglecting *dE/dx* and secondaries, *V(x)* derives directly from the primary recoil distribution *P(x)*.

Impact on boron activation and diffusion

The near-surface vacancy profile has a dramatic impact on the solubility of ultrashallow B implants. B clustering in crystalline silicon requires a supply of interstitials, and can be suppressed by eliminating them. By introducing a high concentration of vacancies before B implantation, essentially no B clustering is possible except where the B "+1" interstitial concentration exceeds the implanted vacancy concentration. Thus if the vacancy concentration approaches $10^{21}/cm^3$, a similar concentration of electrically active B can be achieved.

At the same time that clustering is suppressed, the elimination of self interstitials ensures that there is essentially no transient enhanced diffusion of the implanted B. In principle some TED can take place during the recombination of vacancies and interstitials in the very early stages of annealing, but this is only important at very low co-implantation doses (5) and is almost negligible in the present dose regime. The presence of a vacancy excess may also slightly assist in reducing the metallurgical junction depth of the B implant before annealing, as the excess vacancies will impede room-temperature migration of B (6,7).

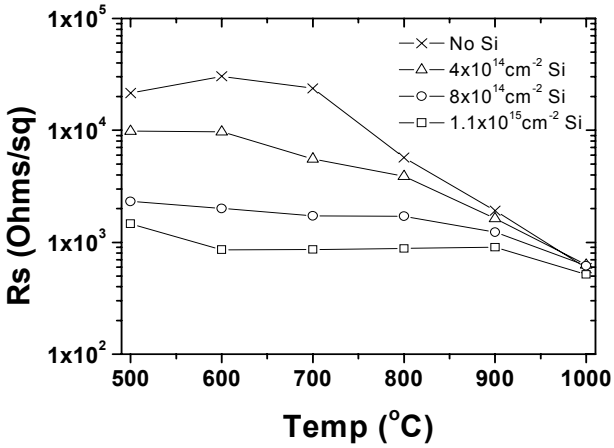

Fig. 6: R_s values for a 500 eV $1.10^{15}/cm^2$ B S/D co-implanted with 160 keV Si to various doses and annealed. A stable R_s value of 800Ω/□ is achieved with the highest dose.

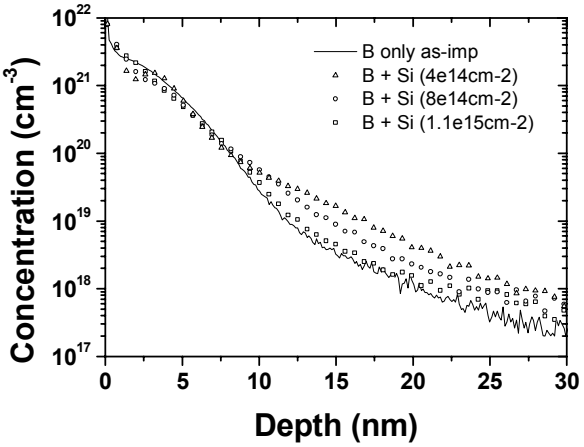

Fig. 7: B SIMS depth profiles corresponding to the R_s data in Figure 6, for an annealing temperature of 700°C. The highest dose gives almost no diffusion, but activation is high (Fig.9)

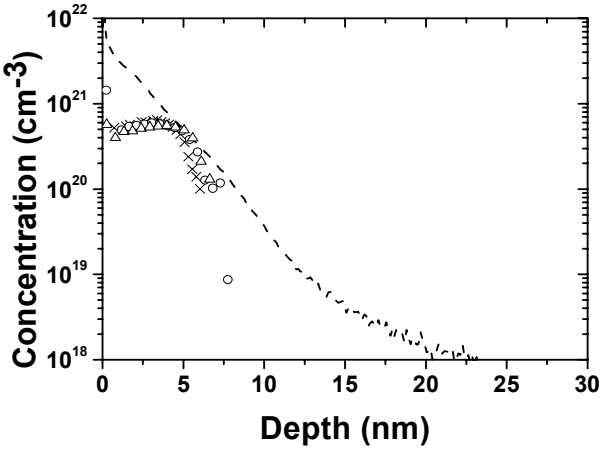

Fig. 9: SIMS (dashed curve) and repeated DH profiles (symbols) for a B S/D with 1.1 10^{15}/cm^2 Si co-implant. The active concentration reaches a maximum value of approx. 7.10^{20}/cm^3.

Figures 6-9 show the impact of 160 keV Si co-implantation on the sheet resistance, and on the atomic and electrical profiles, of 500 eV implanted B in silicon. The results show near-diffusionless B activation up to concentrations of ~7.10^{20}/cm^3, with R_s~860Ω/□ and metallurgical X_j~15 nm, both stable up to about 800°C without the use of short-time processing.

Looking in more detail, Fig. 6 shows that at low temperatures VEI reduces sheet resistance (improves activation) progressively as the co-implant dose is increased. This continues to hold until the top layer is completely amorphised by the VEI implant (higher doses, not shown).

Fig. 7 shows SIMS data from samples annealed at 700°C, showing how VEI reduces diffusion, while at the same time the 'kink' concentration at which B diffuses out from the implant peak increases with the VEI dose. The kink effectively disappears at the highest dose, because in that case there is almost no diffusion at 700°C.

Fig. 8 shows temperature dependent results at the highest VEI dose, showing that after a sufficient thermal budget a kink does appear, and that the kink concentration is substantially higher at this dose, at about 5.10^{20} cm^{-3}. A detailed measurement of the electrically active B concentration profile, obtained by differential Hall profiling, is shown in Fig. 9 together with the corresponding SIMS data for the total atomic concentration. Assuming a Hall scattering factor of 1 we find a peak active B concentration of approximately 7.10^{20} cm^{-3}.

By scaling the dose closer to the amorphous limit (Fig. 5) we expect that sheet resistances in the range R_s~500-600Ω/□ should be attainable. It may even be possible to push this limit further by increasing the VEI dose beyond the limit for buried amorphous layer formation. Initial experiments show that, provided the buried amorphous layer extends fully to the back of the silicon top layer, it regrows downwards towards the silicon/BOX oxide interface, leaving no significant extended defects within the silicon top layer (8).

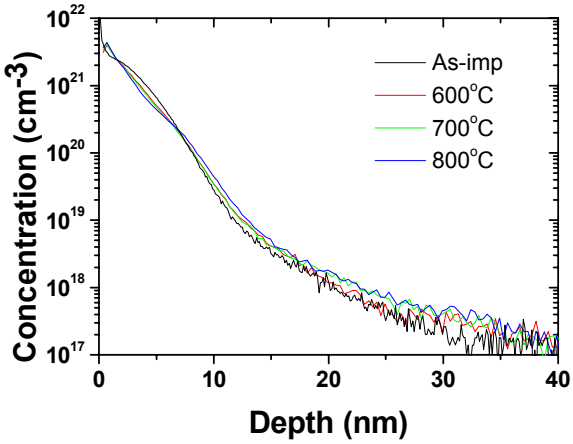

Fig. 8: B SIMS profiles with the highest Si dose, after annealing at temperatures in the range 600-800°C. There is little diffusion but a 'kink' appears at ~5.10^{20}/cm^3, consistent with high activation level.

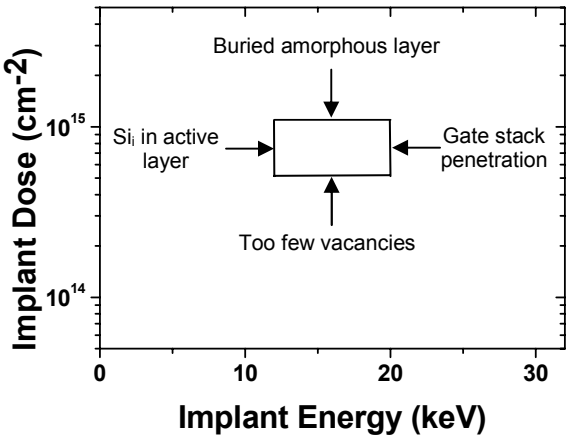

Fig. 10: Process window for V engineering using Si co-implants in a nominal 45 nm node SOI MOSFET (L_g=40 nm, t_{SOI}=10 nm). Details of the process limits (arrows) are in the text.

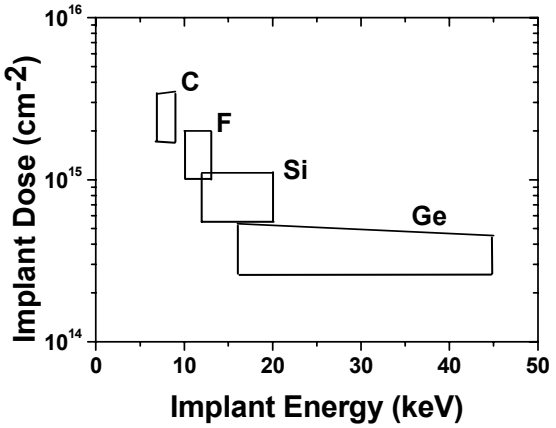

Fig. 11: Approximate process windows from continuum simulations (SUSPRE) for V engineering using C, F, Si or Ge in the nominal 45 nm SOI MOS technology given in Fig. 10.

Application of VEI to 45 nm technology and beyond

Typical VEI process windows at the 45 nm technology node are illustrated in Fig. 10 (for Si co-implants) and Fig. 11 (for C, F, Si, Ge). The window limits are set by the need to avoid (A) buried amorphous layer formation, (B) insufficient vacancies for optimal activation, (C) a Si_i-rich layer in the bottom portion of the active silicon layer, (D) penetration of the VEI implant through the gate stack. Straggle is lowest with the Ge implant, enabling a wider process window, and the optimal Ge implant dose is no more than a few 10^{14} cm^{-3} – less than that for a typical source-drain extension implant.

As discussed in the previous section, the upper limit of the process window (constrained by buried amorphous layer formation) can be extended if downward SPER is considered acceptable. This leads to a higher limit (not shown), which is approximately determined by the dose where the buried amorphous layer reaches the shallow B implant, leaving the near-surface crystallinity intact.

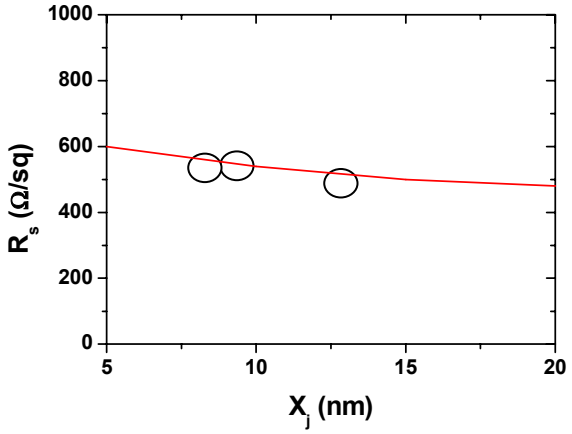

Fig. 12: Predicted R_s/X_j trend for VEI (curve) compared to the ITRS 2004 update (open symbols). R_s increases only slightly as X_j is reduced, due to increase in activation with proximity to the surface.

Concerning the 2D aspects of the point defect distributions following a vacancy engineering implant, it should be noted that a small volume (close to where the pocket implant is usually located, also seen in the inset to Fig. 2) is Si_i-rich. Geometrical considerations suggest this will have little impact on the S/D dopant, but may help protect against deactivation of the n-type pocket implant by vacancies.

Finally, Fig. 12 sketches the predicted outlook for future scaling of sheet resistance as junction depths decrease. Since V(x) rises towards the silicon surface, shallower B implants will be more highly activated, so the R_s/X_j curve is almost flat apart from the slight effect of decreased mobility. The projected sheet resistance scaling meets the ITRS specifications without the use for advanced processing methods such as flash or laser processing.

Conclusions

Simulation and physical experiments have shown that advanced VEI has the potential to provide outstanding PMOS source-drain performance and scalability. When successfully integrated in CMOS technology, the VEI approach uniquely offers the opportunity to re-use knowledge, process module concepts and equipment over several future device generations.

Acknowledgements

We thank Prof. Roger Webb for useful discussions, and for providing the SUSPRE and Cascade simulators for use in this work.

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