Simulation study of overlap capacitance in source-gated transistors for current-mode pixel drivers

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Abstract—Contrary to conventional design principles, current-driven pixel drivers based on source-gated transistors (SGTs) achieve their optimal drive current and speed with a deliberate 5 - 10μm gate-source overlap. Total pixel circuit area need not increase, as the additional device area can be compensated by reducing the pixel storage capacitor. Numerical simulations demonstrate the viability of SGTs for emissive pixel drivers and high gain, low power, robust circuits for emerging sensor arrays.

Index Terms— TFT, OLED, active matrix, display, Schottky barrier, pixel circuit, energy efficiency, layout optimization

I. INTRODUCTION

As display screens continue to progress from a means of delivering information to pervasive entertainment, the competing pressures of improved image quality and low-cost fabrication will increase. Emissive, OLED-based screens show a performance advantage over competing technologies due to their high contrast [1, 2], energy efficient [3, 4], flexible [5–7] and arbitrary-shape [8–10] form factor. Significant progress has been made recently in gate driver circuit design [11–14] and complex pixel circuits, with timing strategies optimized for age compensation or areal uniformity [15–20]. Yet many practical challenges remain [19, 21].

Image uniformity and energy efficiency can be further improved by optimizing the pixel drive transistor itself. Source-gated transistors (SGTs) [22–25] purposely include a potential barrier at the source, as the main means of inducing current saturation. Optimized SGTs have significant advantages compared to traditional thin-film transistors (TFTs); a much lower saturation voltage [22–24], [26–29]; practical absence of short channel effects [23, 24, 30, 31]; and extremely low dependence of drain current on drain voltage [24, 26, 28, 32–34]. These properties are particularly desirable for current-driven pixels, as they enable: increased energy efficiency; more compact pixel designs for higher aperture ratios; and improved image uniformity, respectively. These devices differ marginally in their fabrication from TFTs and can be realized in practically all the usual material systems, thus being easily integrated in existing large-area processes.

The source-gate overlap required for SGT operation may be inherent in the fabrication. Even as this overlap and the unique current control mechanism lowers the maximum device speed, switching is still sufficiently fast for an OLED display pixel. An optimal range for source-gate overlap is found, which: is easily achievable in fabrication; does not reduce the dynamic performance appreciably; and incurs no significant areal penalty in the pixel circuit layout. The recommendations we derive are different to those expected for TFT circuits.

II. DEVICE MODELING AND CHARACTERISTICS

Device simulations were performed with the Silvaco Atlas (v. 5.19.17.C) suite. Staggered-electrode, top-gate devices have: self-aligned gate and drain electrodes; full overlap between the gate and the source over the length of the source (denoted S); a 5μm source-drain gap; a 40nm semiconductor layer (a-Si or poly-Si, both using the default parameters for materials and defects from the simulator); and a 50nm SiO2 gate insulator. Aluminium was used as the ohmic drain contact. The source barrier was set by specifying the electrode work function and the barrier lowering parameter was α = 4nm.

D.c. simulations were performed to extract transfer and output characteristics. Capacitances and a.c. conductances between all pairs of terminals were computed at f = 1kHz.

Figure 1a shows the schematic of a simple two-transistor, one capacitor (2T-1C) circuit for an OLED emissive (sub-) pixel [35]. Drive transistor, T1, sinks current through the OLED during operation. (Sub-)pixel brightness can be unequivocally set by applying a given potential to the gate of T1 through pass transistor T2. When the DATA line is driven at the desired potential, opening T2 with the SELECT signal charges capacitor CSTORE. Once T2 is turned off, CSTORE keeps the gate potential of T1 at the desired value for the duration of the frame. Conflicting requirements intervene in the optimization of the design [36]: the emissive (aperture) area A should be maximised; CSTORE should be small enough to charge rapidly and to maximize A, but large enough to retain enough charge despite the leakage current of T2; T2 should have a high on/off ratio; T1 should occupy minimal area, but be able to source the required output current, which should not vary with drain-source voltage (VDS).

Here, we propose using a source-gated transistor (SGT)
The output conductance, \( g = \frac{I_{\text{sat}}}{V_{\text{DD}}} \), has an extremely small value in saturation that, despite the relatively large variation of current with distance in the accumulation layer present in the source region (drain current), explained by the resistive potential drop with increasing \( V_{\text{DD}} \). For larger values, this dependence reduces as the source area. For small \( S \), the dependence of \( V_{\text{DD}} \) on \( S \) is, of course, independent of source length. The subthreshold region of both TFTs and SGTs is controlled by the semiconductor and is of no interest to this study. Transfer curves for polysilicon SGTs are presented in Figure 2b. Subthreshold behavior differs from the a-Si SGTs in Figure 1a due to altered material properties.

Current levels are comparable between poly-Si and a-Si devices for a given source work function, however, poly-Si SGT transconductance is somewhat higher due to the greater carrier mobility, a second-order effect in SGTs. Lowering the barrier to 4.52eV raises the current and reduces dependence on \( S \). The higher current is a direct result of the lower barrier, while the lower value of \( S \) for which current saturates with \( S \) is attributed to higher resistive potential drop in the semiconductor, and thus a reduction of the contribution to drain current from the bulk of the source[23, 39].

### III. FREQUENCY BEHAVIOR VS. DEVICE GEOMETRY

The most efficient geometry for d.c. current output has \( S \approx 8 \mu m \). Concerning dynamic performance, the gate-source overlap increases gate capacitance, and thus reduces the frequency response. Figure 2c shows the proportion of total gate capacitance represented by \( C_{GS} \) for various \( S \) and source work function. A-Si and poly-Si devices with self-aligned gate/drain and \( d = 5 \mu m \) are shown. Usual design directions would suggest that \( S \) should be minimized for fast operation (e.g. in Figure 3, for \( S > 8 \mu m \), \( C_{GS} \) is > 80% of gate (below 1pS/μm device width) for all values of \( S \). Together with the low saturation voltage, this is an essential benefit of SGTs, which can thus be used as current sources or series drivers with reduced distortion and superior energy efficiency.
capacitance). Two SGT operating characteristics recommend that source-gate overlap be larger than in conventional TFTs.

First, in the pixel circuit, the structure formed by the source, semiconductor, gate insulator and gate is connected in parallel with the $C_{\text{STORE}}$. From Figure 2c, it can be observed that the gate-source capacitance of a SGT operated in saturation is similar to that of a MIM or a MIS capacitor of the same area, due to the accumulated charge layer at the semiconductor-insulator interface [23, 38, 39] in this bias condition. The drive transistor’s $C_{\text{GS}}$ can thus be used as part of the required storage capacitance with practically the same areal efficiency as a MIM capacitor. Using SGTs, even with their required gate-source overlap, will not compromise pixel layout.

Second, in OLED displays, fast switching of $T_I$ is not required, but optimization is desirable. SGT drain current $I_D$ increases initially proportionally with $S$, then saturates as $S$ increases. Concurrently, the gate-source capacitance $C_{\text{GS}}$ of the transistor is to a good approximation proportional to $S$, and the $C_{\text{GS}}$ is itself the dominant term in the total gate capacitance $C_G$. We can consider cut-off frequency $f_T = g_m / (2\pi C_G)$ as a figure of merit representative of switching speed, where $g_m = dI_D / dV_G$ is the transconductance.

There is then a range of optimal $S$ where $f_T$ is maximised, intuitively at values of $S$ beyond which the current dependence on $S$ becomes sublinear (while the $C_{\text{GS}}$ keeps increasing in proportion to $S$). Figure 4 shows the extracted values for $f_T$ at different bias conditions for the a-Si SGT, poly-Si SGT and a-Si TFT, respectively. Both SGTs show an initial increase of $f_T$ with $S$, then $f_T$ reduces, as the additional capacitance introduced by larger $S$ has a greater contribution to $f_T$ than the increased $g_m$. Both technologies show a peak in $f_T$ around $S = 8\mu m$, with the higher absolute value reached by the poly-Si devices attributed to higher carrier mobility. The TFT exhibits a completely different behavior. For no value of $S$ greater than zero does $f_T$ improve, since current does not change with $S$ and gate-source overlap increases gate capacitance, lowering $f_T$. The TFT’s $f_T$ is 5-30 times higher than that of the SGTs depending on bias and $S$, due to its larger $g_m$ in the absence of the source barrier. Even so, the SGT’s $>250\text{kHz}$ is ample for this application. Figure 4 also confirms the SGT’s tolerance to geometrical variations. In high-throughput printing, alignment errors may occur, yet the SGT’s $f_T$ is practically unchanged.

IV. CONCLUSIONS

SGTs offer significant advantages to current driver circuits: the low saturation drain voltage can potentially reduce power consumption by allowing a lower supply voltage to be used. In emissive pixel circuits, SGT drivers can improve the uniformity of light emission through: low drain-voltage dependence of drain current; tolerance to geometrical variations during processing; and (e.g. in a-Si:H and ZnO), improved bias stress stability.

To fully exploit SGT features, circuit design techniques require adaptation. Contrary to conventional rules, SGTs acting as drive transistors in current-mode drivers benefit from a source-gate overlap of several microns for increased current injection and optimal speed. When the transistor is used in a pixel driver circuit, its source-gate overlap also acts as a storage capacitor, and its area substitutes a portion of the usual MIM capacitor, with potentially no increase of total circuit size. Arrays of precision low-power analog circuits for emerging flexible sensors should find similar benefits from these design rules.

Fig. 3. Gate-to-source capacitance as a proportion of total gate capacitance and its dependence on $S$ for SGTs modelled in different materials and with different values of the source metal work function. The gate capacitance is dominated by the gate-source component even at comparatively small values of $S$. While overlap capacitance increases linearly with $S$, total drain current eventually saturates due to the two-dimensional injection at the source.

over a large range of $S$ ($4 – 16\mu m$ in Figure 4a). Drain current is also insensitive to $S$ for large $S$ (see Figure 1d).

With flat output curves for reduced non-linearity and low saturation voltage for power efficiency, the properties shown here make SGTs robust, versatile drivers for emissive pixels.

Fig. 4. Calculated cut-off frequency ($f_T$) and its dependence on gate bias and source-gate overlap for a) an a-Si:H SGT with source contact work function $WF = 4.67\text{eV}$; b) a poly-Si SGT with $WF = 4.67\text{eV}$; c) an a-Si:H TFT with ohmic contacts. The optimal source-gate overlap is zero for the TFT, but in the range of 4-16$\mu m$ for the SGT as a result of the interplay between transconductance and gate capacitance.