Boron activation and diffusion in pre-amorphised silicon and silicon-on-insulator

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Submitted for the Degree of Doctor of Philosophy from the University of Surrey

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October 2007

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to my parents and aunt
ABSTRACT

For the next generation of electronic products, transistors need to be reduced in size and are required to be highly activated with ultra shallow source / drain extension regions. For p-type dopant implants, a promising fabrication approach is the use of pre-amorphising implants (PAIs). This reduces boron channelling and increases electrical activation due to solid-phase epitaxial re-growth. For technology nodes of 45 nm and beyond, silicon-on-insulator (SOI) is seen as the substrate of choice. Therefore the behaviour of dopants in these substrates needs to be studied to assess whether their electrical and diffusive properties differ from those observed in bulk silicon (Si).

Besides forming an amorphous layer, PAIs generate an interstitial-rich region just below the former amorphous / crystalline interface, which on annealing develop into so-called 'end of range' (EOR) defects. These evolve during prolonged annealing, releasing interstitial Si atoms that interact with the boron implant. This causes undesired effects, such as transient enhanced diffusion (TED) and boron-interstitial cluster (BIC) formation, the latter manifested as electrical deactivation. The main aims of this work are to investigate the silicon / buried oxide interface in SOI as a sink for Si interstitials and then to tailor the implant conditions to reduce BICs and TED.

The research used a series of processing conditions and analytical techniques to study the electrical and structural properties of the samples, with support from Monte Carlo simulations. The results show that optimised PAI (32 keV 1x10^15 Ge cm^-2) in SOI can produce junctions with little de-activation and reduced TED. Optimised PAI in SOI with a 500 eV 2x10^15 B cm^-2 implant led to an reduction in deactivation by a factor of six, from 480 Ω/□ in bulk Si to 80 Ω/□ in SOI. This produced stable sheet resistance values ~800 Ω/□ over a range of anneal temperatures (700 – 1000 °C). At peak electrical B deactivation (850 °C), junction depth in SOI was reduced by a factor of 1.5x from 42.5 nm in bulk Si to 27.5 nm in SOI at a B concentration of 1x10^18 cm^-3. The mechanisms responsible for these improvements in SOI are (1) the buried oxide interface acting as an efficient interstitial sink, with a near zero value for recombination length. (2) The as-implanted excess interstitial population being reduced by trapping in the buried oxide.

The methods described in this thesis are fully compatible with current industrial processes without the need for additional new equipment or process steps at extra costs, making it an attractive alternative and complement to current techniques.
ACKNOWLEDGEMENTS

I would like to take this opportunity to express my very special thanks to my two project supervisors, Dr Karen Kirkby and Prof Nick Cowern, for giving me this opportunity to undertake this research as a postgraduate PhD student. I very much appreciate their patience, help, concern and easy approachableness as supervisors. They have devoted much of their time giving me invaluable advice, technical background and guidance despite their busy schedules.

Dr Benjamin Colombeau deserves a big thank you for his very useful guidance from the start of my PhD, his experience, vast technical knowledge, valuable time and friendship proved to be essential for this project and for my personal progression, without which I would not be where I am today.

Also Erik Collart from Applied Materials (my industrial collaborator) for generously supplying me with the wafers and implants used in this research, as well as his keen interest and expertise throughout my work.

I also appreciate very much the huge amount of SIMS analyses performed by Dr Massimo Bersani, Dr Damiano Giubertoni and Dr Salvatore Gennaro and for extending our collaboration to include a group in Bologna, Italy, who carried out TEM analysis. Therefore I would like to thank also Andrea Parisini for all the TEM analysis, valuable interpretation and for such a fast turn around.

My co-workers Dr Andy Smith, Jim Sharp, Nick Bennett and Max Kah generously helping me with laboratory work when needed, useful technical discussions, a lot of help with conference presentations and great company socially on every occasion. In addition Andy also helped me a lot throughout my PhD in terms of his extra guidance, knowledge and useful advice.

On the experimental side of things I would like to thank Dr Chris Jeynes and Dr Zinat Tabatabaian, for their very invaluable help on using the Tandetron Accelerator and for teaching me how to carry out RBS analysis and interpretations of these results using the Data Furnace – also Adrian Cansell for helping me to get the beam going pretty much every time I used the accelerator.
A big thank you to Prof Roger Webb for extending my funding for another 3 months in order for me to finish my final experiments and continue writing up, as well as useful discussions about carrying out the simulations, and to Prof Russell Gwilliam for organising financial help for me to attend IIT 2006 as well as being great company and support at every conference that I've been to.

Technical and administration staff for helping me in the laboratory, computer support and day to day business, alphabetically: Darryl Patto, Dean Mansfield, Gary Strudwick, John Underwood, Julie Maplethorpe, Karen Arthur, and Richard Rigby.

My family, especially my parents and my aunt for all of their support emotionally, financially, helping me move into various student accommodations countless times and providing me with all the encouragement to continue my studies. Their help has been pivotal for my survival during my extra three and a half years of studying at University.

I appreciate the patience of my work colleagues for surviving my loud voice in the office as well as all of my friends from outside of the office for providing me with a great social life – I will never forget all of your support. These people are listed alphabetically:

Alberto Latorre  Fred Gardes  Mark Whiteley  Roberto Gourlay
Anders Bull  James Benson  Megan Estorninho  Rudi Wieler
Anthony Miller  Jim Sheppard  Mel Webb  Sam Shaw
Bane Timotijevic  Jiyoung Lee  Mike Akers  Simon Howe
Bill Headley  Julie Miller  Mona Sahlabadi  Solmaz Golchin
Cameron Johnston  Kat Lederle  Natacha Mureau  Steve Lyth
Charlie Jeynes  Katie Buckley  Nick Wright  Steve Steer
Claire Mercier  Ken Lim  Nicoleta Gaciu  Steven Payne
Clare Summers  Kerill Dunne  Oliver Praderas  Theresa Damon
Daria Saeidi  Kim Shouler  Oliver Redmond  Tim Sinnamon
Dave Alexander  Lewis Wong  Paul Watts  Tracey Sletten
Dave Jones  Lisa Ahmed  Pinguang Yang  Wojciech Polak
Dave Thomson  Lise Uytterhoeven  Prash Mistry  Yann Tison
Eldad Yahel  Luc Montehliet  Quan Phan  Yoji Miyajima
Elena Timoner  Machos Bourlai  Richard Heap  Yvonne Hubner
Ernesto Mendoza  Marcos Bote  Richard Wainwright  Zoe Chen
Faye Stacey  Mark Rowe  Rita Morais  and more ...
PUBLICATIONS

RELEVANT PAPERS:
(1) "Electrical activation of solid-phase epitaxially re-grown ultra-low energy boron implants in Ge pre-amorphised silicon and SOI"
JJ Hamilton, EJH Collart, B Colombeau, C Jeynes, M Bersani, D Giubertoni, JA Sharp, NEB Cowern and KJ Kirkby

(2) "Understanding the role of buried Si/SiO₂ interface on dopant and defect evolution in PAI USJ"
JJ Hamilton, EJH Collart, B Colombeau, M Bersani, D Giubertoni, JA Sharp, NEB Cowern and KJ Kirkby

(3) "The effect of the buried Si/SiO₂ interface on dopant and defect evolution in PAI USJ"
JJ Hamilton, B Colombeau, JA Sharp, NEB Cowern, KJ Kirkby, EJH Collart, M Bersani and D Giubertoni

(4) "Effect of B dose and Ge pre-amorphisation energy on the electrical and structural properties of ultra-shallow junctions in silicon-on-insulator"
JJ Hamilton, EJH Collart, B Colombeau, M Bersani, D Giubertoni, M Kah, NEB Cowern and KJ Kirkby

(5) "Modelling and Simulation of the Influence of SOI Structure on Damage Evolution and Ultra-Shallow Junction Formed by Ge Pre-amorphisation Implants and Solid Phase Epitaxial Re-growth"
KRC Mok, B Colombeau, M Jaraiz, P Castrillo, JE Rubio, R Pinacho, MP Srinivasan, F Benistant, I Martin-Bragado and JJ Hamilton
(6) "Diffusion and activation of ultra shallow B implants in silicon-on-insulator: End-of-range defect dissolution and the buried Si/SiO₂ interface"
JJ Hamilton, B Colombeau, JA Sharp, NEB Cowern, KJ Kirkby, EJH Collart, M Bersani, D Giubertoni and A Parisini

(7) "Optimal pre-amorphisation conditions for the formation of highly activated ultra shallow junctions in Silicon-On-Insulator"
JJ Hamilton, EJH Collart, M Bersani, D Giubertoni, S Gennaro, NS Bennett, NEB Cowern and KJ Kirkby

(8) "Boron diffusion and activation in SOI and Bulk Si: The role of the buried interface"
M Aboy, L Pelaz, J Monserrat, FJ Bermúdez and JJ Hamilton

(9) "Boron deactivation in pre-amorphised silicon-on-insulator: Efficiency of the buried oxide as an interstitial sink"
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OTHER COLLABORATIVE PAPERS:
(10) "Advanced front-end processes for the 45nm CMOS technology node"
EJH Collart, SB Felch, H Graoui, D Kirkwood, S Tallavarjula, JA Van den Berg, JJ Hamilton, NEB Cowern and KJ Kirkby

(11) "Comparison of Elemental Boron and Boron Halide Implants into Silicon"
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Journal of Applied Physics (in press)

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### Glossary of Terms

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<thead>
<tr>
<th>Abbreviation</th>
<th>Full Form</th>
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<tbody>
<tr>
<td>4pp</td>
<td>Four Point Probe</td>
</tr>
<tr>
<td>a/c</td>
<td>Amorphous / Crystalline</td>
</tr>
<tr>
<td>a-Si</td>
<td>Amorphous Silicon</td>
</tr>
<tr>
<td>AMAT</td>
<td>Applied Materials</td>
</tr>
<tr>
<td>B</td>
<td>Boron</td>
</tr>
<tr>
<td>BIC</td>
<td>Boron Interstitial Cluster</td>
</tr>
<tr>
<td>C</td>
<td>Carbon</td>
</tr>
<tr>
<td>c-Si</td>
<td>Crystal Silicon</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>DI</td>
<td>Deionised</td>
</tr>
<tr>
<td>EOR</td>
<td>End of Range</td>
</tr>
<tr>
<td>F</td>
<td>Fluorine</td>
</tr>
<tr>
<td>FDL</td>
<td>Faulted Dislocation Loop</td>
</tr>
<tr>
<td>Ge</td>
<td>Germanium</td>
</tr>
<tr>
<td>He</td>
<td>Helium</td>
</tr>
<tr>
<td>HREM</td>
<td>High Resolution Transmission Electron Microscopy</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated Circuit</td>
</tr>
<tr>
<td>ITRS</td>
<td>International Technology Roadmap for Semiconductors</td>
</tr>
<tr>
<td>Lg</td>
<td>Gate Length</td>
</tr>
<tr>
<td>MC</td>
<td>Monte Carlo</td>
</tr>
<tr>
<td>MEIS</td>
<td>Medium Energy Ion Scattering</td>
</tr>
<tr>
<td>MOSFET</td>
<td>Metal Oxide Semiconductor Field Effect Transistor</td>
</tr>
<tr>
<td>Ns</td>
<td>Active Carrier Dose</td>
</tr>
<tr>
<td>P</td>
<td>Phosphorus</td>
</tr>
<tr>
<td>PAI</td>
<td>Pre-amorphising Implant</td>
</tr>
<tr>
<td>PDL</td>
<td>Perfect Dislocation Loop</td>
</tr>
<tr>
<td>PEELS</td>
<td>Parallel Electron Energy Loss Spectroscopy</td>
</tr>
<tr>
<td>PMOS</td>
<td>P-type Metal Oxide Semiconductor</td>
</tr>
<tr>
<td>PPC</td>
<td>Process Products Corporation</td>
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<tr>
<td>PTEM</td>
<td>Plan-View Transmission Electron Microscopy</td>
</tr>
<tr>
<td>Rs</td>
<td>Sheet Resistance</td>
</tr>
<tr>
<td>RTA</td>
<td>Rapid Thermal Anneal</td>
</tr>
<tr>
<td>s/d</td>
<td>Source / Drain</td>
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<tr>
<td>Si</td>
<td>Silicon</td>
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<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Description</th>
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<tbody>
<tr>
<td>Si/SiO₂</td>
<td>Silicon / Silicon Dioxide</td>
</tr>
<tr>
<td>SIMS</td>
<td>Secondary Ion Mass Spectroscopy</td>
</tr>
<tr>
<td>SPER</td>
<td>Solid Phase Epitaxial Re-growth</td>
</tr>
<tr>
<td>SOI</td>
<td>Silicon-On-Insulator</td>
</tr>
<tr>
<td>SSI</td>
<td>Small Scale Integration</td>
</tr>
<tr>
<td>TED</td>
<td>Transient Enhanced Diffusion</td>
</tr>
<tr>
<td>TEM</td>
<td>Transmission Electron Microscopy</td>
</tr>
<tr>
<td>μ</td>
<td>Mobility</td>
</tr>
<tr>
<td>ULSI</td>
<td>Ultra-Large Scale Integration</td>
</tr>
<tr>
<td>USJ</td>
<td>Ultra Shallow Junction</td>
</tr>
<tr>
<td>$V_H$</td>
<td>Hall Voltage</td>
</tr>
<tr>
<td>$X_J$</td>
<td>Junction Depth</td>
</tr>
<tr>
<td>XTEM</td>
<td>Cross-Sectional Transmission Electron Microscopy</td>
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</table>
A semiconductor material is a solid-state material whose electrical conductivity can be controlled by doping and by an externally applied field. It is in this material that transistors are made. The transistor was discovered by three scientists William Shockley, John Bardeen and Walter Brattain in 1947 at Bell Labs [1]. This triggered an electronic revolution and soon replaced the current technology at the time, the “vacuum tube” – due to its smaller size, higher reliability and long life.

However after transistors started becoming commonplace and shrunk in size they soon began to reach a physical human handling limit in terms of connecting, resistors, capacitors and other electronic components together by wires. Then in 1959 (twelve years after the discovery of the transistor) the solution arrived, the “Integrated Circuit” (IC). This device, which was independently invented by two scientists, Jack Kilby from Texas Instruments and Robert Noyce at Fairchild Semiconductor allowed for an entire electronic circuit to be built onto a single chip and was the size of a pencil point [1].

Since their invention ICs have evolved very quickly, constantly getting smaller and smaller and with this the ability to fit a larger quantity of devices on to each chip. At the same time manufacturing wafer size has increased (currently 300 mm), expanding the number of ICs per wafer. Since the 1960's the industry has moved from Small Scale Integration (SSI) to the present Ultra Large Scale Integration (ULSI), with a component count of ~10^9. Reduction of the transistor size on an IC also has the bi-product of increasing speed, reducing cost and power consumption. These advantages are coupled with the demand for smaller, faster, cheaper electronic products used in the everyday world.

Currently transistor size has reached the 45 nm technology node, planned to be in production this year [2]. Technology node or generation is a method of referring to transistor size, based on the half-pitch (average width between the start of one metallisation lane to another) of a Dynamic Random Access Memory (DRAM) manufactured at that technology level [3]. The 45 nm technology node was forecasted to be in production by 2010 according to the International Technology Roadmap for Semiconductors ITRS. The ITRS is a US led consortium of industrial, academic and government organisations with the objective of detailing future directions of research in an effort to overcome technological challenges and to ensure cost-effective
advancements in the performance of the integrated circuit [3]. In order to keep up with the requirements of the ITRS, transistors need to be downscaled; however problems soon begin to arise from this process. For complementary metal oxide semiconductor (CMOS) devices one of these challenges, and the focus of this thesis, is the scaling of the source / drain (s/d) extension region.

The requirements for these s/d extension regions are highly activated ultra-shallow box-like doping profiles. This translates as having a shallow junction depth ($X_j$) combined with a low sheet resistance ($R_s$). Ion implantation is the preferred method to create these junctions, as it has the advantages of being repeatable and can precisely control the dopant implant depth and dose. Subsequent to implantation rapid thermal annealing (RTA) is required to repair the damage created by the implant process and to move the dopant atoms from interstitial onto substitutional lattice sites, up to their solubility limit. Once on these substitutional sites the dopant atoms form bonds with the neighbouring silicon (Si) and introduce either shallow donor or acceptor levels into the band gap, thus making the material conduct via electrons or holes and changing its resistivity.

For p-channel Metal Oxide Semiconductor (PMOS) transistors the requirements for s/d extension regions are hard to achieve. Since boron (B) (the only widely used p-type dopant) being a small light ion needs to be implanted at very low energies. As well as this, implant channelling (deeper penetration of the dopant atoms into the Si substrate) needs to be eliminated as this gives a greater $X_j$. An example of channelling can be seen in Figure 0-1.

![Figure 0-1 Schematic representation of implant channeling](image-url)
To avoid B channelling into crystalline silicon (c-Si) a technique known as pre-amorphisation is used. This involves amorphising a layer of the Si with Si⁺ or Ge⁺ ions prior to B doping, so that the B is implanted into amorphous Si (a-Si) and so cannot channel (see Figure 0-1). A process known as Solid Phase Epitaxial Re-growth (SPER) is used to re-crystallise the amorphous layer, using low temperature thermal annealing (shown in section 1.3.1). It also has the advantage of improving the electrical activation of the B atoms [4], as explained in more detail in section 1.3.

The major problem with pre-amorphisation is that during annealing of the damage created during the implantation process, a band of End-of-Range (EOR) defects form (made of Si interstitials). These are situated in the damaged but non-amorphised region below the former amorphous / crystalline interface. During annealing at larger thermal budgets these EOR defects undergo a series of transformations during which they release Si interstitials. These interstitials then migrate to the nearest available sink such as silicon / silicon dioxide (Si/SiO₂) interfaces, for bulk Si this is the Si surface where the B is situated.

During the course of this migration they interact with B atoms, causing it to electrically deactivate resulting in an increase in $R_s$. This occurs by clustering of the Si interstitials with the B to form Boron Interstitial Clusters (BICs). The interstitials also give rise to enhanced B diffusion known as Transient Enhanced Diffusion (TED) which is responsible for increasing $X_j$. Both of these effects are undesired [5].

A variety of techniques have been reported in the literature in order to overcome these problems of deactivation and diffusion, some of these include: laser or ‘flash’ thermal processing, vacancy engineering, co-implantation and use of alternative substrates. Sometimes two or more of these techniques are combined to maximise their effect.

One possible method to stop the interstitials from interacting with the B atoms is to provide an alternative sink for the Si interstitials (for example another Si/SiO₂ interface), away from the B implant. Silicon-On-Insulator (SOI) substrates appears to fit this criteria since they are composed of three layers, (1) a thin layer of top Si, (2) a buried oxide (BOX) layer and (3) the remainder of the bulk of the substrate (shown in Figure 0-2). The presence of the buried layer provides an alternative Si/SiO₂ interface between the Si top layer and its BOX layer (away from the B implant), in addition to the interface at the top Si surface.
It is also important that the use of the pre-amorphisation technique in SOI is compatible with current processing techniques in order for it to be the future starting substrate for CMOS devices, predicted by the ITRS to take place from 2008 [3].

This thesis studies the use of the pre-amorphisation technique between bulk Si and SOI substrates and its implication for future CMOS devices!

OBJECTIVES

The objectives of this research are:

(1) Annealing temperature consistency between bulk Si and SOI wafers:

The temperature experienced by bulk Si and SOI wafers when annealed together may not be the same. It is important when comparing between the two material types and for industrial CMOS processing that the true temperature experienced by SOI wafers is determined.

(2) The buried interface as a potential sink for interstitials and resulting effects:

It is postulated that the buried interface in SOI may act as a sink for interstitials. With such a sink, diffusing interstitials traversing the B profile might be avoided and could lead to less B deactivation and enhanced diffusion.

(3) Optimisation of the technique in SOI:

Understanding the effects introduced by the buried interface in SOI can allow the process to be optimised and meet challenges set out by the ITRS. As well as being able to integrate into current manufacturing processes for CMOS devices.
THESIS STRUCTURE
This thesis is organised into the following chapters:

Publications
This lists all of my publications, including collaborative work.

Introduction
The historical background to the work as well as a brief summary of the topic is contained in this section. It also indicates the objectives for the work as well as an overview of the structure and a synopsis of the novelty of this research.

Chapter 1 – Literature Survey
This chapter is a review of the published literature for this subject and covers an introductory background, current issues with B as a dopant as well as discussing possible solutions. It focuses on the literature that supports the approach used in this work, the pre-amorphisation technique and the substrate material used, SOI and ends with a summary.

Chapter 2 – Experimental Techniques
The various experimental techniques used in this work as well as their background theory are detailed and discussed in this chapter. It explains the process steps undertaken and their associated errors.

Chapter 3 – Results I: Amorphisation and SPER
The first set of experiments, investigating SPER in Si and SOI wafers is used to determine whether the anneal temperature experienced by the both substrate types is the same.

Chapter 4 – Results II: The Buried Interface
The experimental design for studying the electrical and structural effects in Si and SOI is described in this chapter. It reports the experimental results and also discusses the influence of the pre-amorphisation energy. From these results a theory is postulated about the behaviour of the EOR defects in SOI wafers.
Chapter 5 – Results III: Optimisation

This chapter uses the results from the previous chapter to optimise the structure in Si and SOI wafers. It discusses a second effect of using SOI substrates. It also extends the research to encompass some modelling of the results in order to quantify the relative contribution of the sinking effect in SOI material. This model is also used to verify and qualify the theory outlined in Chapter 4.

Conclusion

Here a summary of the research is presented, showing how the objectives for this work have been met and stating the main results. It also, discusses areas for future work.

References

This is a list of all the references used.

Appendix

This section contains additional information.

NOVELTY OF WORK

The novel factor for this research is the use of the pre-amorphisation technique in SOI and the exploitation of the benefits of the upper BOX interface in SOI as a tool for improving dopant behaviour (activation and diffusion). This occurs via accelerating the dissolution of EOR defects compared to bulk Si. This research concentrates on the electrical properties as well as studying the diffusive properties thus providing a direct input into the technology roadmap. Furthermore the modelling studies provide a test of the theories postulated in this work with supporting quantative results.

Finally this research shows the processes involved in the formation of ultra-shallow junctions in SOI are easily transferable to current processes lines, meeting requirements specified by the International Technology Roadmap for Semiconductors.
CHAPTER 1  LITERATURE SURVEY

1.1 INTRODUCTION

This chapter is a literature review focusing on B as a dopant for CMOS devices since all the work in this thesis is carried out using this dopant. It is partitioned into several areas, covering the objectives for downscaling of devices, problems resulting from this and discusses possible solutions. It finally extends to a review of current research in the field using the main technique in this work – pre-amorphisation and continues to explain how this research evolves from there.

1.2 MINITURISATION

To keep up with the constant demand in the modern world for smaller, faster and cheaper electronic products the number of transistors on an IC must be increased. In order to accomplish this, the physical dimensions of CMOS devices have to be downscaled achieving advantages such as faster, cheaper and less power hungry integrated circuits.

![Figure 1-1 Number of transistors per chip on Intel's processors](image)

A paper published in 1965 by Gordon Moore [7]; co-founder of Intel predicted that the number of transistors on an IC would double every couple of years. This was based on
evidence of the rate of integration since 1959. The trend predicted by Moore in 1965 still holds true of today and according to the current predictions of the ITRS is expected to carry on for at least the next 10 years. Figure 1-1 shows the actual trend in transistor count as a function of year, based on Intel’s microprocessor progress.

1.2.1 Source / Drain Engineering

In the digital world a CMOS device is made up of a complementary pair of n-type and p-type Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). Figure 1-2 is a schematic representation of this device. An important factor when shrinking transistor size is the gate length ($L_g$) since reduction in this results in faster switching times for the transistor [8]. However when scaling, all dimensions must be reduced in proportion, in order to minimise problems known as short channel effects – which for example is exhibited as leakage current.

Figure 1-2 Simplified schematic of a MOSFET

To avoid these negative effects reduction in the dimensions of the source and drain junction depth is necessary, more specifically the depth of the s/d extension region ($X_d$), labelled in Figure 1-2. With the junction profile (that is lateral abruptness) being as steep as possible. Another requirement is the reduction in the resistance of these regions, addressed in this thesis as sheet resistance ($R_s$).

Predictions made by the ITRS for p-type s/d extension regions are summarised in Figure 1-3. Important features are twofold, (1) present transistor technology is at the 65 nm node, however Intel have advertised that their newest 45 nm node processor is due to start production this year [2], which is predicted by the ITRS for 2010. Also significant, (2) it is suggested that the starting substrate will change from bulk Si to SOI in 2008.
SOI is a bulk Si wafer with a buried insulating layer of SiO$_2$ beneath the region where active devices are fabricated. Beneath this buried layer is the bulk of the single crystal Si substrate. A schematic of this is shown in Figure 0-2. The attractive quality about this material for CMOS transistors is improved device performance for the same device dimensions as in bulk Si substrates. As a consequence it is seen to be a future substrate of choice by the ITRS roadmap [3], [9].

1.2.2 Junction Formation

Knowing the requirements for downscaling with respect to the s/d extension regions, the next step is to look into how to form these junctions. Implantation is the primary method used (see section 2.3) for doping a material to form a junction, due to its reproducibility, precise control of dopant implant depth and dose. However a downside of implantation is the damage introduced into the substrate by the process through the displacement of the host lattice atoms. A thermal anneal is thus required to re-order the lattice to a crystalline structure and also to electrically activate the implanted dopant atoms.
There are three main steps to this process ramp-up, dwell period and ramp-down (see Figure 1-4). The dwell period is set for the pre-determined temperature and time. The ramp-up and down is the time it takes to reach the desired temperature, with the option to control the ramp rate.

![Diagram of an anneal cycle](image)

**Figure 1-4 Schematic representation of an anneal cycle (1) ramp-up, (2) dwell period and (3) ramp-down**

For p-type Metal Oxide Semiconductors (PMOS) B is the most popular dopant due to its relatively high equilibrium solid solubility ($1.2 \times 10^{20}$ cm$^{-3}$ at 1000 °C) [10] and low ionisation energy in Si (0.045 eV) [8]. However during implantation this dopant suffers from an effect known as channelling, which results in the B penetrating deeper into the substrate. In order to overcome this, a technique known as pre-amorphisation is used.

### 1.3 PRE-AMORPHISATION TECHNIQUE

Crystal silicon has a regular atomic structure with a tetrahedral configuration (diamond type structure). However Si in an amorphous state has no lattice configuration and can be described to be formed by an accumulation of damage. In this situation there is no way to predict atomic positions at distances far from a given atom; hence the arrangement of atoms is often loosely described as a “random”. Even though atoms clearly ‘avoid’ each other, they tend towards tetragonal bonding and have interatomic distances similar to those in c-Si.

One method to amorphise single c-Si wafers is by the implantation of heavy ions (such as Ge) where the depth of amorphous layer depends on the implant energy, mass and dose. This phase change starts with the creation of point defects or local amorphous regions until these regions accumulate as successive cascades are implanted and then the highly damaged c-Si becomes unstable and transforms into a-Si [11]. In order to re-
crystallise this amorphous layer, heat treatment is necessary, this process is known as solid phase epitaxial re-growth (SPER).

One of the advantages of amorphisation prior to B implantation is that it avoids B channelling. Channelling is a process whereby the incident ion beam is directed along a “channel” in the crystal lattice, as viewed in Figure 1-5. This allows the implanted ions to penetrate deep into the Si wafer due to there not being atoms to block its path. However in a-Si, there are no channels due to the damage of the lattice and consequently the implanted ion (e.g. B) does not penetrate as deep into the sample for the same implant dose / energy as in c-Si.

![Figure 1-5 Si crystal lattice viewed from channelling directions <100> and <110> [12]](image)

The effect of pre-amorphisation for avoiding channelling compared to c-Si is shown in Figure 1-6. Here B has been implanted into either c-Si or Ge pre-amorphised wafers to different depths. The graphs show that for a B implant into c-Si a channelling tail (green circle) is observed. When using a 2 keV Ge pre-amorphising implant (PAI) the B implant extends beyond the amorphous layer and a channelling tail is still observed. For the 5 keV PAI a small amount of channelling is observed indicating that the tail of the B distribution extends beyond the a-Si layer. For the highest PAI energy, 20 keV, the entire distribution is within the amorphous layer and therefore minimal channelling is seen. This shows that by careful selection of PAI conditions an $X_J$ (taken at $1 \times 10^{16}$ cm$^{-3}$ B) can be reduced by $\sim 18$ nm. Also junction abruptness increases for B implants into a-Si layers.
The benefits of using Ge (rather than Si) for amorphising a Si wafer are that, since it has a relatively heavy mass, (a) a relatively small dose can be used to amorphise the Si, (b) there is less implant straggle, so the amorphous / crystalline (a/c) interface is sharper and consequently the amorphous layer re-grows more cleanly than one produced by a lower mass ion [14].

Another benefit of pre-amorphisation is an increase in B activation as a result of the SPER process [15]. Since dopant atoms are incorporated onto lattice sites during the re-growth of the a-Si into c-Si during annealing and therefore can activate at lower temperatures than similar implants into c-Si only [16], [17].

### 1.3.1 Solid Phase Epitaxial Re-growth (SPER)

Re-ordering (or re-growth) of an amorphous layer of Si on top of a crystal layer was first reported in 1968 by Mayer et al. [18], it involved the heating of an amorphised Si wafer at a temperature of ∼570 °C.

Upon annealing the atoms in the amorphous layer re-order them selves following the structure of the crystal layer, which acts as a seed, the direction of re-growth moving from the a/c interface towards the surface. This is shown in Figure 1-7 as a series of
Cross-sectional Transmission Electron Microscopy (XTEM) images (see section 2.9). The rate of re-growth is temperature dependent and at a given temperature the amount re-grown is proportional to anneal time.

![Annealing time diagram](image)

**Figure 1-7 XTEM micrographs of SPER isothermally annealed at 600 °C [5]**

The temperature at which this re-growth occurs in intrinsic Si varies in different publications, but is generally reported to start between 550 °C – 570 °C [18], [19] and even shown to occur as low as 500 °C [20].

Csepregi *et al.* [19] reported the intrinsic re-growth activation energy of 2.3 eV for Si and also noted that the re-growth rate was linear with time. However later work showed that it was higher 2.68 – 2.85 eV [21], [22], [23], [24]. Olson *et al.* [22] noted that the re-growth rate was independent of amorphisation energy. Csepregi *et al.* [25] was the first to show in 1977 that impurity atoms can affect the SPER rate, where phosphorus (P), Arsenic and B doping impurities enhance SPER in Si with B resulting in the largest effect. This has also been shown by [20], [21], [22], [23] and that this rate is further enhanced by increasing B dose.

### 1.3.2 Implantation Damage

A drawback of the pre-amorphisation technique is the formation of EOR defects (due to a supersaturation of interstitials) below the former a/c interface after SPER [15]. In order to understand this process, the case for non-amorphising implants is described and depicted in Figure 1-8a-c and then follows to describe the case for amorphising implants (Figure 1-8d-f) [26].

When ions are ion implanted into Si they lose energy due to electronic and nuclear interactions with the host atoms (discussed in more detail in section 2.3.2). If the energy transferred during nuclear stopping from the incident ion to the lattice is sufficient a Si
atom will be ejected from its lattice location and become a Si interstitial leaving behind a Si vacancy. This Si interstitial will carry on producing a cascade of further collisions in the material, creating more interstitials until it stops due to loss of energy. Therefore one interstitial and one vacancy are created during each recoil. This defect pair is known as a “Frenkel pair” [4], [27].

The interstitial distribution after implantation is slightly deeper than the vacancy distribution. Since the momentum transfer of the incident ion is in the forward direction (interstitial moves deeper into the substrate), resulting in a spatial separation of the two profiles. This is shown schematically for non amorphising implants in Figure 1-8a.

![Non Amorphising Implant](image1)

**Figure 1-8 Schematic representation of (a)-(c) non amorphising and (d)-(f) amorphising implants into Si, shown as time sequences during annealing [26]**

Since the Si lattice is disordered, thermal annealing is used to repair the damage, during this process the Frenkel pairs recombine and the dopant atoms activate by taking substitutional positions in the lattice. This process leaves one extra Si interstitial for each
implanted ion and is known as the "plus-one model" [4], [28], [29] – shown in Figure 1-8b. Further annealing allows these interstitials to evolve into extended defects (see section 1.4), situated within the implant profile (Figure 1-8c). The separation of the defect distributions is dependent on implanted ion mass and energy.

For a PAI, an ion of higher mass (e.g. Ge) implanted at higher energies (keV) compared with a non-amorphising implant is used to form a layer of a-Si (Figure 1-8d). During annealing (Figure 1-8e) SPER takes place, using the single crystal Si below the amorphous layer as a seed. This allows the a-Si layer to re-grow and become single c-Si again. A band of excess interstitials remains just below the former a/c interface. During SPER these interstitials (Figure 1-8f) agglomerate into a band of extended defects (see section 1.4) termed End-of Range (EOR) defects (Figure 1-7). Since defect growth is faster than SPER and Si diffuses less in an amorphous state, defects remain below the former a/c interface [30].

This EOR band can be seen experimentally and was reported by de Mauduit et al. [31] in 1994. In their experiment Si wafers were amorphised with 150 keV 2x10^15 cm^-2 Ge, annealed at 1000 °C for 10 s, creating a band of defects 170 nm below the surface. This EOR band was created beneath the former a/c interface. They showed that defects were present within the EOR band and corresponded to the agglomeration of excess Si interstitial atoms produced from implantation and annealing.

1.4 EXTENDED DEFECTS

The excess interstitials caused by ion implantation and annealing eventually condense to form extended defects. These defects evolve through a series of transitions into different types (see section 1.4.3), until they subsequently dissolve through loss of free self interstitials to nearby sinks such as the Si surface [5], [29].

1.4.1 Defect Evolution

This evolution process is known as Ostwald ripening, a theory which was further developed by Lifshitz, Slezov and Wagner (LSW theory) [32]. It involves the growth of larger defects at the expense of smaller ones. Since larger defects are more energetically favoured as the thermal budget is increased. This is shown schematically in Figure 1-9a (assuming a closed system).
In a realistic (non-conservative) process there are other parameters, such as the silicon surface, the bulk of the wafer and the resultant concentration gradients. In this situation there are other paths (green dashed lines) for the free interstitials to follow. As well as exchanging of interstitials between the defects (Figure 1-9b). The probability of interstitials diffusing towards the surface is higher than them diffusing into the bulk of the wafer, due to the relatively short distance of the surface from the defect band. The resultant (blue line in Figure 1-9b) shows a reduction in the Si interstitial supersaturation towards the surface due to surface recombination of Si interstitials.

![Figure 1-9 Schematic representation of an Ostwald ripening process (a) conservative and (b) non-conservative ripening [26]](image)

### 1.4.2 Role of the Surface

Omri et al. [33] in 1996 suggested that after complete SPER the surface could act as a sink for interstitials. This was later shown by Cowern et al. [34] in 1999 studying the diffusion of B after the re-growth of a-Si, which was known to be enhanced by the presence of Si interstitials [35] (see section 1.5.2). In their experiments [34] Si wafers were implanted with Ge at 150 keV to a dose $2 \times 10^{15}$ cm$^{-2}$ and then etched to leave different distances from the EOR band to the surface (175 nm, 125 nm and 80 nm). The samples were then subsequently implanted with 3 keV $1 \times 10^{14}$ cm$^{-2}$ B and annealed for 1s at 900 °C. Secondary Ion Mass Spectrometry (SIMS) (see section 2.8) showed that B diffusion was greater the closer the EOR defect band was to the surface. The
experimental results were compared with simulations of the interstitial flux toward the surface. It was shown that the closer the EOR band was to the surface, the higher the concentration gradient for interstitial diffusion. This evidence led to the conclusion that the surface acted as a sink for the Si interstitials with a higher flux for an EOR defect band closer to the surface. This conclusion was confirmed by Giles et al. [36] and Venezia et al. [37].

In 2003 Lamrani et al. [38] showed direct evidence of the recombination of Si interstitial atoms at the Si surface. They grew four B marker layers at distances 0.1 µm, 0.4 µm, 0.7 µm and 1 µm from the surface within a Si substrate. The wafer was then implanted with Si 100 keV 2x10^{14} cm^{-2} to form a layer of extended defects between the first and second marker layers from the surface, at 0.2 µm. The samples were then annealed at 850 °C for times ranging from 15 s to 300 s and SIMS was used to monitor the subsequent enhancement of B diffusion in the marker layers. The results are shown in Figure 1-10a. They show that as the anneal time is increased there is an enhancement of B diffusion, with least diffusion near the surface. Observed by the wider profiles for the 300 s than the 200 s anneal and also wider distributions for deeper B marker layers, respectively.

![Figure 1-10](image)

**Figure 1-10** Diffusivity enhancement of B (a) for annealed SIMS distributions and (b) measurements related to the Si interstitial supersaturation gradient [38]

From their data, they measured values for the diffusivity enhancement of the B marker layers. This was then related to the Si interstitial supersaturation with respect to distance from the surface (Figure 1-10b). The results showed a gradient of the supersaturation of Si interstitials towards the surface as a result of the surface recombination of Si interstitial atoms that escaped the defect region. Also for increasing anneal time 15 s to 300 s the gradient reduces, resulting from a lower supersaturation of interstitials due to their recombination at the surface.
1.4.3 Types of defects

There are four types of extended defects shown in Figure 1-11, using Transmission Electron Microscopy (TEM) images. These are clusters, \{113\}'s, perfect dislocation loops (PDLs) and faulted dislocation loops (FDLs) [15]. They are all precipitates of self interstitials, and can only dissolve by emission of interstitials (or absorption of vacancies).

![Figure 1-11 Different types of defects formed during annealing (a) clusters, (b) \{113\}'s, (c) transformation from \{113\} into loops (d) PDLs and FDLs and finally (e) FDLs only [15]](image)

The types of extended defects that form are dependent on implantation and anneal conditions and evolve through a series of transitions from clusters, \{113\}, PDLs and FDLs. As the defects transform their formation energy decreases, which is the energy required to add one extra atom to the defect [39].

**Implantation Conditions**

Increasing the implantation dose increases the initial concentration of Si interstitial atoms present after implantation, which is related to the types of defects that are formed after annealing. For example, implanting a 40 keV 2x10^{13} \text{ cm}^{-2} \text{ Si implant into Si, defects are hardly visible by TEM after annealing for 15 s at 815 °C. However for the same conditions but incrementing only the Si dose to 5x10^{13} \text{ cm}^{-2} TEM shows \{113\} defects are formed. As the thermal budget is increased the \{113\} defects no longer dissolve but grow until transforming into dislocation loops [41]. For this situation as well as implantation dose, the surface now plays a role. By increasing the implantation energy, the defect region from the surface also increases resulting in a lower Si interstitial gradient towards the surface [34]. Therefore there is a higher concentration of Si...
interstitials in the damaged region, compared to a lower energy implant, which can evolve into higher forms of defects.

*Increasing Thermal Budget*

Anneal conditions are another factor in the evolution of these defects. Plan-view TEM (PTEM) images, in Figure 1-12, shows the evolution of defects with respect to thermal budget. These results were obtained by annealing pre-amorphised Si wafers implanted with $2 \times 10^{15}$ cm$^{-2}$ 150 keV Ge ions. It shows that by increasing the annealing time / temperature different types of defects are formed. From 10 s at 750 °C to 400 s at 1000 °C the types of defects evolve from clusters to {113} to PDLs and finally FDLs.

![Figure 1-12: Thermal evolution of EOR defects as a function of annealing conditions](image)

Following implantation and / or during the anneal ramp-up, most of the excess interstitials are accommodated in the form of di-interstitials [29]. Due to the Ostwald Ripening process, as the anneal budget increases these begin to cluster (Figure 1-11a).
It is thought that clusters of more than 20 atoms are similar, at least in terms of formation energy to {113} defects [29]. Increasing the thermal budget still further, results in "rod-like" defects being observed that lie on {113} planes and are elongated along the <110> direction [29] (Figure 1-11b). Once these rod-like defects are formed they grow in size and reduce their density, with continued annealing, to subsequently transform into dislocation loops.

There are two main types of dislocation loop, perfect (Figure 1-11d) and faulted (Figure 1-11e). They are reported to be either elongated, near circular or hexagonal objects and are more stable than {113} defects [15], [29]. For higher thermal budgets (Figure 1-12) only the FDLs survive [42].

The release of interstitials from these defects is the cause of anomalous diffusion and activation of B in Si, discussed in the following sections.

1.5 DIFFUSION

1.5.1 Mechanisms

Fick’s Law defines diffusion as the movement of atoms from regions of high concentration to regions of lower concentration in proportion to the diffusion coefficient of the diffusing ion (see Equation 1-1).

\[ \phi = (-D) \frac{dN}{dx} \]

Equation 1-1 Fick’s First Law [27]

Where;
- \( \phi \) is flux (mol/m²s)
- \( D \) is the diffusion coefficient (m²/s)
- \( N \) is the particle concentration (mol/m³)
- \( x \) is the depth (m)

The mechanisms involved for the diffusion of dopant atoms in Si are depicted in Figure 1-13. For a dopant atom 'X' diffusion is assisted by point defects (self-interstitials or vacancies) [43]. This happens via interactions of these point defects with the dopant atoms leading to the formation of defect pairs.
Figure 1-13 2D schematic representation of diffusion mechanisms for an impurity atom X (open circle) in a solid. ‘V’, ‘I’, ‘X’ and ‘Xs’ denote vacancies, self-interstitials, interstitial and substitutional positions of the foreign atoms respectively. XV and XI are defect pairs of the corresponding defects [43].

The defects pairs depicted in Figure 1-13 are listed below:

1. \( X_s + V \leftrightarrow XV \)  
   Vacancy Mechanism
2. \( X_s + I \leftrightarrow XI \)  
   Interstitialcy Mechanism
3. \( X_s + I \leftrightarrow X_i \)  
   Kick-out Mechanism
4. \( X_s \leftrightarrow X_i + V \)  
   Dissociative Mechanism

Where X represents a dopant atom, I a Si interstitial, V a vacancy, and subscripts ‘S’ and ‘I’ represent substitutional and interstitial positions respectively. [43], [27].

**Boron Diffusion in Si**

For the case of B, diffusion occurs by interactions with Si interstitials – mechanisms (2) and (3) (Figure 1-13) and is referred to as the interstitialcy mediated method. The notation is the same as in Figure 1-13, except the dopant atom is now labelled ‘B’ for boron. It starts with a diffusing Si interstitial kicking out a B substitutional atom. The Si interstitial incorporates itself into the lattice site and the B atom becomes an interstitial atom. This will then diffuse until it kicks back into a substitutional position and knocking out a Si interstitial which carries on diffusing into the Si lattice (see Figure 1-14) [27], [44], [45].
Annealing of B implanted into Si suffers from a thermal diffusive effect, which consequently increases $X_I$. However this diffusion effect can be enhanced by a phenomenon known as Transient Enhanced Diffusion (TED). This can occur even at relatively low temperatures (e.g. 600 °C), where thermal diffusion would not normally be significant.

### 1.5.2 Transient Enhanced Diffusion (TED)

In 1973 Hofker et al. [46] published a paper showing the diffusion of B in Si, for doses ranging from $1 \times 10^{14}$ cm$^{-2}$ to $1 \times 10^{16}$ cm$^{-2}$ at an energy of 70 keV the experiments covered a whole range of annealing recipes (700 °C to 1100 °C with times up to 21 hrs) in order to study the full diffusive effect. SIMS results showed broadening of the B distributions as a function of anneal temperature and time. Most of the diffusion happened during the initial stages of the thermal process and was best observed for isothermal anneals. It was suggested that the agent responsible was a large supersaturation of point defects, however which type of defect was not specified. They also noticed that there was a fraction at the peak of the B profile that was immobile during annealing and concluded that this immobile fraction consisted of B precipitates (assumed to be formed by B interstitials) created in the anneal process.

Michel et al. [47] were the first to show that: (1) the displacement of the B tail is larger at lower annealing temperatures, where (2) the diffusion is faster (but slows down as it approaches the saturation limit) and (3) the diffusion saturates faster at higher temperatures. That is the anomalous diffusion is a transient effect, from where the name
Transient Enhanced Diffusion is derived. The experimental results of Michel et al. (Figure 1-15) show conclusively the effect of increasing anneal time. They also noticed, like Hofker et al. [46], that there is an immobile fraction of the B profile, seen at the higher B concentrations and exhibited at the peak in the profile.

![Figure 1-15 Isothermal anneals of B in Si showing transient effect of TED [47]](image)

Before the work by Michel et al. it was already known that the Si interstitial was the cause of the TED, this was shown in 1978 by Claeys et al. [35]. They showed this by studying the phenomenon during the diffusion of B by creating stacking faults in Si by wet oxidation. Evidence for the observed results was based on two facts, (1) the growth kinetics of stacking faults in Si is generated by absorption of interstitials. (2) Anneals in oxygen ambient creates an excess of interstitials, whereas a nitrogen ambient produces excess vacancies [48]. After annealing in either ambient, the length of the stacking faults was measured and showed that the diffusing B atoms enhance the growth of the stacking faults under an oxygen ambient and retard their shrinkage under a nitrogen anneal. This evidence led them to conclude that the B diffusion was driven by Si interstitials.

**Role of Defects**

Eaglesham et al. [40], [49] showed that (113) defects are an important source of the interstitials in TED. They used a B delta-doped superlattice implanted with Si and showed that after annealing there was a broadening of the peaks, especially in the vicinity of the implant damage (Figure 1-16a).

A (113) defect was observed using TEM (Figure 1-16b) and they correlated the presence of the defect during the early stages of TED as a possible source of the interstitials. They
then used quantitative measurements of the evolution of the \{113\} defects and related the number of interstitials emitted by the defects with the flux of interstitials driving the TED. Their conclusion was that the \{113\} defects were the source of the interstitials which caused the TED.

\begin{figure}
\centering
\includegraphics[width=\textwidth]{figure1-16.png}
\caption{TED in a B delta-doped superlattice (a) showing enhanced broadening, particularly near the surface and (b) \{113\} defect after 15 s annealing at 815 °C [40]}
\end{figure}

Investigations by Zhang \textit{et al.} [50] showed that \{113\} defects are not the only source of interstitials responsible for TED and that there may be more than one source. This was evident from experiments which used a relatively low B dose of $1 \times 10^{14}$ cm$^{-2}$ at energy of 4 keV. Anneals were then performed between 700 °C to 850 °C for times of 2 min to 8 hr. Their results showed that although TED was observed, XTEM did not show the presence of \{113\} defects or extended defects – since these are below the detection limit for these techniques. They concluded from this indicating that there was more that one source of interstitials for TED. These results were confirmed by Liu \textit{et al.} [51] who went on to show that for B implant energies above 10 keV \{113\} defects are seen by TEM and enhance the already present B TED.

In 1999 Robertson \textit{et al.} [52] correlated EOR damage evolution with TED of B in regrown Si substrates. Si wafers were amorphised using Si implants at a dose of $1 \times 10^{15}$ cm$^{-2}$ with energies of 120 keV and then followed by a 30 keV Si implant to create a continuous amorphous layer 240 nm thick. The wafer was subsequently implanted with B at energy of 4 keV at a dose of $1 \times 10^{14}$ cm$^{-2}$ and annealed at 750 °C for times 15 min to 6 hr. The results in Figure 1-17a show junction shift with anneal time and is correlated with
the density of interstitials bound in EOR defects (Figure 1-17b) for the same time sequence – studied using TEM.

![Figure 1-17 TED of B (a) junction shift and (b) density of interstitials bound in EOR defects as a function of annealing time [52]](image)

The results show the presence of \{113\} defects and dislocation loops in the EOR band. As the anneal time is increased, there is a reduction in TED (Figure 1-17a) and in interstitials bound to the \{113\} defects, while interstitials bound to the loops increases (Figure 1-17b). They went on to say that the dislocation loops were not releasing interstitials but were growing in both density and interstitial content. Also the number of interstitials bound to the dislocation loops are increasing faster than the release of interstitials from the \{113\} defects. This suggests that there is another source for interstitials binding to the dislocation loops. They proposed that this source was sub-microscopic interstitial clusters and added that these interstitial clusters may be the principle source of the TED.

**Location of Defects**

In 1988 Ozturk *et al.* [53] showed the effects of Ge pre-amorphising energy on TED of B implanted at 10 keV at a dose of $1 \times 10^{15}$ cm$^{-2}$. An SPER anneal was carried out at 550 °C for 30 min and then a subsequent anneal at 1050 °C for 10s to study the diffusion of B. The results are shown in Figure 1-18a. Comparing a non-amorphising implant (profile X) to a 50 keV PAI (profile C), B diffusion is reduced after annealing. Increasing the PAI energy to 80 keV and 125 keV (profiles B and A respectively) shows a further decrease in diffusion. This is because increasing PAI energy increases the distance of the EOR defect band from the surface and thus from the B profile. This subsequently reduces the interstitial flux to the surface [34] and therefore fewer interstitials interact with the B
implant, resulting in less B diffusion. Ajmera et al. [54] showed similar results (Figure 1-18b) however they used simulations to study the impact of PAI energy of B diffusion.

![Graph showing the effect of pre-amorphising energy on B diffusion.](image)

**Figure 1-18 Effect of pre-amorphising energy on B diffusion (a) Ozturk et al. [53] and (b) Ajmera et al. [54]**

**Uphill Diffusion**

An interesting diffusive effect has been seen by various authors [55], [56], [57], where contrary to classical Fickian diffusion (see section 1.5.1) dopant profiles have diffused from low concentrations to high concentrations, this effect is known as “uphill diffusion”.

Quite recent results (2003) from Duffy et al. [57] are presented in Figure 1-19. They pre-amorphised wafers to different depths (5.5 nm, 13.7 nm and 29 nm) by varying the Ge implant energies (1.4keV, 5 keV and 15 keV respectively). The diffusion of B after annealing was then studied and compared to a non-amorphised sample. SIMS showed the presence of B uphill diffusion, but only in the case of the pre-amorphised samples. This was observed by a decrease in the depth of the B profile (at a concentration of $5 \times 10^{20}$ cm$^{-3}$) compared to the as-implanted condition. The largest shift of the B towards the surface was seen for the 1.4 keV Ge sample, resulting in 2.1 nm of uphill diffusion (Figure 1-19a).

The results showed that the uphill diffusion is more pronounced for lower energy PAIs, where the a-Si depth and therefore EOR damage are closer to the Si surface and the peak of the implanted B. They explained that this was due to a steeper Si interstitial
gradient towards the B profile as the EOR band approached the surface and is linked to a high concentration of boron-interstitial pairs.

Figure 1-19 Uphill diffusion of a 500 eV 1x10^{15} cm^{-2} B implant into pre-amorphised Si annealed at 700 °C for 2 hrs for (a) 1.4 keV PAI and (b) 15 keV PAI [57]

TED in the tail region of the B profile was seen for the higher energy (5 keV and 15 keV) PAIs (Figure 1-19b). In this situation the EOR defects are positioned within the tail of the B implant. Hence the Si interstitials released from the EOR defects play a larger role in the tail diffusion of the B implant. A small peak in the B profile corresponding to the position of the EOR defect band was also observed. This is caused by B trapping on EOR defects [58], [59] (Figure 1-19b).

The results from the work by Duffy et al. show that there are two competing diffusive processes. For lower PAI energies uphill diffusion near the surface dominates and for higher PAI energies TED in the tail of the B implant dominates.

1.6 ACTIVATION ANOMALIES

The diffusion experiments carried out by Hofker et al. in 1973 [46], were continued a year later [60]. The focus of these studies was the immobile peak originally observed in their earlier work (Figure 1-15). They compared SIMS B distributions with differential Hall measurements (Figure 1-20a) and discovered that the immobile peak was electrically inactive. Michel et al. [47] agreed with this conclusion, also showing that R_s reduced with increasing anneal temperature and anneal time, exhibiting a transient effect like the anomalous diffusion. For lower values of R_s the size of the immobile inactive fraction in the peak of the B profile also reduced. This fraction became increasingly mobile and able
to diffuse as the thermal budget increased. They concluded that this favoured a mechanism of dissolution of clusters of point defects.

Holland et al. [61] disagreed with Michel et al. explaining that the immobile peak was active substitutional B, but that the tail was interstitial B. Supporting the theory by Hodgson et al. [62] that the tail of the B profile diffused a lot faster than the peak close to the surface and was due to B atoms occupying interstitial positions.

In order to resolve the controversy Cowern et al. in 1990 [63] carried out experiments comparing spreading resistance profiling (SRP) measurements with SIMS. From this they proved that the static peak was composed of electrically inactive B, in agreement with the results from Hofker et al. [60] and are shown in Figure 1-20. The label ‘C_{enh}’ also referred to as the ‘kink’ (used in the results section of this thesis) is the critical concentration at which the profile begins to diffuse from the inactive region.

![Figure 1-20 Immobile and electrically inactive peak (shaded in red) resulting from TED, results from (a) Hofker et al. [60], (b) Cowern et al. [63]](image)

It was proposed by Cowern et al. that the diffused region was associated with electrically active substitutional B diffusing via a point defect assisted mechanism. However the immobile peak was associated with trapped non-substitutional B atoms resulting from the supersaturation of interstitials forming B defect complexes.

1.6.1 Boron Interstitial Clusters (BICs)

Boron interstitial clusters (BICs) consist of B combined with Si interstitial atoms. These are thought to be the cause of an immobile peak seen close to the Si surface at the peak of B profiles after annealing. Due to their small size it is hard to identify these clusters and the evidence for their existence comes from interpretation of the diffusion and electrical data.
However in 2003 Cristiano et al. [64] showed by TEM the presence of a defect in the \{100\} plane after high dose B implanted Si (Figure 1-21). This was presumed to be a large BIC since it was formed at the same depth as the immobile B peak.

![Figure 1-21 High resolution XTEM showing a defect ~2.5nm below Si surface, thought to be a BIC (for implanted 1x10^{15} B cm^{-2} at 500 eV annealed for 10 s at 650 °C) [64]](image)

Since the evolution of these defects cannot be seen experimentally, theoretical methods have been used to try to explain the evolution of these BICs. It is important to understand this as it helps to explain the relationship of the dopant-interstitial complex with dopant deactivation.

Pelaz et al. [65], [66] proposed a model where during the early stages of the anneal cycle, when there is a large supersaturation of Si interstitials, BICs are predominantly high in interstitial content (but less stable). Whereas during the latter part of the annealing process BICs emit Si interstitials leaving a higher B concentration behind, it is only after large thermal budgets (e.g. 790 °C for 10 hr [67]) that these more stable clusters will dissolve.

The results shown in Figure 1-22 describe the evolution of BICs. This uses the notation of $B_mI_n$, where 'm' is the number of B atoms and 'n' is the number of interstitial atoms (these can be either B or Si interstitials). The pathways are consistent with the immobile peak dissolving after TED ends and the defects have dissolved, allowing the B to re activate.
As a result of the evidence shown up to this point, B TED and deactivation have been shown to be caused by the release of Si interstitials from defects formed during implantation and annealing. This supersaturation of interstitials has a gradient towards the Si surface where they recombine, as the defects dissolve. When increasing the thermal budget, the effects of TED begin to saturate with electrical reactivation taking place.

**Pre-amorphisation and Dopant Electrical Deactivation**

In 2004 Pawlak *et al.* [68] showed evidence for the mechanism of B deactivation in Ge pre-amorphised Si. They carried out isochronal anneals on pre-amorphised bulk Si wafers, the Ge energies were 8, 12 and 25 keV with dose $1\times10^{15}$ cm$^{-2}$, resulting in a-Si layers of 14 nm, 22nm and 42 nm respectively. The wafers were subsequently implanted with B 1.5 keV to a dose $3\times10^{15}$ cm$^{-2}$.

The results (Figure 1-23a) show that while annealing there is an increase in $R_S$ driven by interstitials released from the EOR band, resulting in clustering of the B atoms (BIC formation). After reaching a peak, the $R_S$ then begins to decrease during further annealing and is attributed to the dissolution of BICs. It also shows that by increasing the
position of the EOR defect band from the surface (higher PAI energies), the temperature at peak deactivation increases. While the amount of deactivation, from 650 °C to the peak, decreases. This result is attributed to a smaller gradient of supersaturation of Si interstitials towards the surface, when the EOR band is positioned deeper into the substrate [34], [69]. Therefore requiring a larger thermal budget for the interstitials to reach the surface where they can then interact with the active B layer.

Cristiano et al. [70] observed similar deactivation results both isochronally and isothermally (Figure 1-23b) with B implanted at 500 eV \(1 \times 10^{15}\) cm\(^{-2}\) pre-amorphised with 30 keV \(1 \times 10^{15}\) cm\(^{-2}\) Ge. They concluded that the clustering was due to the release of interstitials from the EOR band. This was carried out by comparing simulations with experimental data on the evolution of the extended defects.

The literature has shown that during thermal treatment of B implanted into Si, TED occurs and BICs form. These manifest themselves in the form of increasing \(X_J\), due to diffusion of the B profile and electrical deactivation (resulting in an increase in \(R_S\)) due to BIC formation. It is the control of TED and BICs that allows Ultra Shallow Junctions (USJs) to be created. Conventional B implantation or B implantation with pre-amorphisation alone can no longer satisfy the targets set by the ITRS – however combined with alternative techniques this may be achievable.
1.7 MEETING ITRS REQUIREMENTS

1.7.1 Advanced Annealing

As discussed in section 1.3.1, in order to repair implantation damage and to activate dopant atoms, thermal annealing is required. The disadvantage is the formation of defects, which upon further annealing release interstitials that cause B deactivation and enhanced diffusion. Therefore tailoring of the annealing conditions (specifically ramp rate Figure 1-4) plays a role in the reduction of TED and BICs.

In 2001 Mannino et al. [72], used a Si wafer with B marker layers and implanted it with 6 keV $1\times10^{13}$ cm$^{-2}$ Si and subsequently annealed, using an rapid thermal annealer, up to 900 °C for 0.1 s, varying the ramp rate 0.1, 1, 10 and 100 °C/s. Results showed that by increasing the annealing ramp rate TED can be reduced. This was explained by a reduction in overall thermal budget, since TED is a transient effect reducing with increasing temperature. Similar results were seen by Agarwal et al. [71], who also showed an increase in dopant activation.

Due to these positive attributes (increase in B activation and reduction of diffusion), focus for the evolution of annealing schemes has been fast anneals with high ramp rates. This starts with the slowest furnace anneals to, RTA, spike, flash and finally laser annealing. For the 90 nm technology node spike annealing was the method of choice for junction formation; however for future technology generations other forms of annealing are being studied [16].

In a paper by Lindsay et al. [16] comparisons of different annealing techniques for improving junction characteristics were carried out. They showed SPER combined with flash annealing was one of the most promising solutions for reaching the 45 nm node requirements. More recently flash assisted annealing has shown how activation can be improved for PMOS applications [73] as well as diffusion requirements [74]. However this method currently has integration issues with manufacturing solutions due to wafer stresses caused by the anneal process [75].

Laser annealing both melt and non-melt has recently shown some very promising results for suppression of dopant deactivation and TED [76], [77]. Like flash annealing this method also suffers from integration issues due to the heating non uniformity of the laser scan over the whole of the wafer [78].
1.7.2 Co-implantation

One way of stopping the interaction of interstitials with B is to find a way to trap the interstitials before reaching the B distribution. One such method was investigated by Cowern et al. [79]. They showed that when implanting fluorine (F) in pre-amorphised wafers the co-implant acted as a trap for the interstitials. It was suggested that this was due to a fluorine-vacancy cluster mechanism created during SPER. $R_s$ results (Figure 1-24) showed suppression of B deactivation when the peak of the F distribution was between the B implant and the defect band or on top of the defect band. SIMS also showed that when the F distribution was situated between the EOR band and the B implant, TED was reduced creating steeper junctions. Similar improvements of F implants have been reported by other authors agreeing with the F-V model [80], [81], [82], [83], [84].

![Figure 1-24 F as a trap for interstitials from the EOR band [79]](image)

Pawlak et al. [85] used carbon (C) co-implantation to minimise B TED and deactivation. These results, in terms of diffusion, are summarised in Figure 1-25, and show that the high C dose ($2 \times 10^{15} \text{ cm}^{-2}$) with B gave the best results. However in terms of $R_s$ (not

```
0.9keV F
10keV F
22keV F
```

```
Ge 1x10^{15}\text{ cm}^{-2} 30keV + B 1x10^{15}\text{ cm}^{-2} 500eV
F 1x10^{15}\text{ cm}^{-2} at 0.9, 10 or 22 keV

(a) As-implanted F distributions showing depth relations with B profile and EOR band
(b) Isothermal anneal at 800 °C showing deactivation relation with position of F peak

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shown, see ref [85]) and $X_J$ the best results are achieved using pre-amorphisation combined with C at the lower dose ($1 \times 10^{15}$ cm$^{-2}$).

Pawlak et al. explained their results by referring to the conclusions proposed by Mirabella et al. [86]. Mirabella et al. explained that substitutional C atoms trap Si interstitials and form carbon-Si interstitial (C-Si$_i$) clusters in the ratio of $C_2$Si$_i$. Using this theory, Pawlak et al. proposed that there was a higher substitutional C fraction present in the re-grown pre-amorphised samples than in c-Si, resulting in less B diffusion. Therefore SPER of a-Si was more efficient at situating C onto substitutional sites during re-growth, than in standard c-Si.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure1-25.png}
\caption{C as a trap for Si interstitials [85]}
\end{figure}

Graoui et al. [87] has shown that C can reduce B diffusion more efficiently than F. They report a 27% improvement in $X_J$ when combined with Ge pre-amorphisation and after spike annealing at 1050 °C. Unfortunately C in Si increases device junction leakage [88], making F still an attractive co-implant. A combination of the two however has been investigated by Vanderpool et al. [89], who showed a reduction in diffusion over F alone. It is worth noting that they used a lower dose C ($1 \times 10^{15}$ cm$^{-2}$) when combined with F than would be needed if C was used alone ($2 \times 10^{15}$ cm$^{-2}$) [85].

The literature shows that the effects of co-implantation of F or C can suppress dopant-defect interactions. However this has been shown to work best when combined with pre-amorphisation.

1.7.3 Vacancy Engineering

In 1991 Raineri et al. [90] investigated the effects of a high energy Si implant after B implantation into Si wafers. They showed a reduction in the transient B tail diffusion and
suggested that it was due to secondary defects acting as interstitial sinks. However in 1999 Venezia et al. [91] proved that the real reason for the TED reduction was the production of an excess of vacancies by the Si implant in the near surface region. This was shown by using a 1 MeV Si implant into an SOI (section 1.2.1) substrate (Figure 1-26). The effect of this implant was to physically separate the vacancy rich region in the Si overlayer and the interstitial Si rich region below the BOX. As the diffusion of Si interstitials in SiO₂ is very small (~10⁻¹⁷ cm²/s at 1100 °C [92]) the BOX acts as a barrier for the Si interstitials and prevents them from reaching the B. This has the effect of preventing the deactivation process from occurring improving B dopant activation [93].

![Figure 1-26 Vacancy engineering using a 1 MeV 1x10¹⁶ cm⁻² Si into SOI with B marker layers. Defect distributions (a) as-implanted and (b) annealed showing the corresponding position of the BOX. The resultant B diffusion after annealing (c) no MeV implant or (d) with MeV implant, both (c) and (d) with or without an additional 40 keV Si implant [91]](image)

The benefits of vacancy engineering in SOI were further studied by Smith [94] in 2006. The novel factor in this work was the use of a much lower Si co-implant energy of 160 keV with dose 1.1x10¹⁵ cm⁻² and then doping with B at 500 eV 1x10¹⁵ cm⁻². This resulted in generating the equivalent vacancies than a high energy (MeV) implant. It should be noted that the SOI structure had a 55 nm Si top layer with a 145 nm BOX. After annealing (600 °C – 800 °C for times 10 s to 1000 s) produced a stable junction 17 nm deep with an Rₛ ~900 Ω/□.
As well as the use for SOI in vacancy engineering, the ITRS predicts its incorporation as a starting substrate in 2008 [3] research has been carried out to see if dopants behave in the same way in SOI as they do in bulk Si.

1.7.4 Silicon-On-Insulator (SOI)

An SOI wafer consists of a bulk substrate with a buried layer of SiO₂ (shown in Figure 0-2). There are many methods of producing SOI: two of them use ion implantation but with different species – these processes are called SIMOX (Separation by Implanted Oxygen) and Smart Cut™ (see section 2.2.1).

Advantages of SOI over bulk Si for the fabrication of future CMOS integrated circuits are improved device performance (i.e. reduced parasitic capacitance, elimination of latch-up, increased speed, and reduced power consumption) and as a consequence of this, SOI is seen as a candidate for the future replacement of bulk Si substrates [9].

So how does using SOI and more specifically the presence of the BOX interface, affect dopant diffusion, activation and defect evolution?

Effects on Dopants in SOI

There is controversy in the literature about the effects of SOI on dopant diffusion and activation. Crowder et al. [95] and Uchida et al. [96], [97], have shown that B diffusion is reduced in SOI compared to bulk Si wafers and is dependent on the Si/SiO₂ interface quality / roughness.

Uchida et al. [97] in 2002 studied B diffusion in bulk Si and SOI wafers by using a spin-on-glass source at 860 °C for 10 min in N₂ ambient. Four different types of SOI wafers were used produced by different types of fabrication methods, UNIBOND®, epitaxial layer transfer (ELTRAN) and SIMOX with and without internal-thermal oxidation (ITOX).

Their results (Figure 1-27) show that less B diffusion is seen for SOI wafers compared with bulk Si. Between the types of SOI from least to most reduction in B diffusion are, ELTRAN, UNIBOND®, SIMOX with ITOX and then without ITOX. They related the retardation of B diffusion to the quality of the BOX interface and postulated that the reduced diffusion was due to Si interstitials recombining at the BOX interface. Consequently acting as an alternative sink for interstitials and therefore competing with the surface sink.
Figure 1-27 B diffusion for wafers annealed at 860 °C for 10 min, comparing bulk Si with different types of SOI fabrication methods [97]

More recently Ottaviano et al. [98] in 2004 showed that $R_s$ in SOI is higher than that for bulk Si samples. Similar results have been shown by Saavedra et al. [99] who also noticed an increase in $R_s$ for B implanted UNIBOND® SOI wafers compared to bulk Si (Figure 1-28). The further away the B profile was from the Si/BOX interface the more $R_s$ reduced.

Figure 1-28 Position of Si/BOX interface, vertical solid black lines in (a), with respect to $R_s$ (b) for 1 keV $3 \times 10^{16}$ cm$^{-2}$ B, comparing with bulk Si [99]

As well as this a decrease in electrical activation and mobility in SOI samples with respect to bulk Si was seen, but above ~900 °C SOI values approached those observed for bulk Si. These results were attributed to an increase in BICs during the annealing of
SOI material. This theory was based on an assumption that the SOI BOX interface acts as a reflective boundary for interstitials, contrary to the conclusions of Uchida et al. [97].

So far there is a conflict in opinion in the literature as to whether the BOX interface acts as a sink or a reflector of Si interstitials. Since B electrical de-activation and TED are caused by Si interstitials it is important to understand the role of the BOX interface on the evolution of these defects. In 2002 Saavedra et al. [100], [101] observed that extended defects in SOI dissolved faster when they were situated close to or overlapped the BOX interface. Later in 2004 [102] they showed that {113} defects in SOI dissolve faster when compared to bulk Si. Similarly the {113} defects in SOI are less stable than those in bulk Si and favour the formation of dislocation loops as the surface Si layer is thinned. A possible mechanism to explain these results was that the BOX interface roughness in SOI allows Si interstitials to recombine there. Also, it is worth noting that throughout their studies they did not notice any real differences between SIMOX and SOITEC® wafers.

All of these previous results were carried out in crystalline Si; however Li et al. [103] in 2003 found that for Ge (5 keV 1x10^{15} cm^{-2}) pre-amorphised wafers more B (500 eV 1x10^{15} cm^{-2}) diffusion was seen in SOI (SIMOX) than in bulk Si (Figure 1-29).

It was explained that this enhancement was due to interstitial pile-up near the BOX interface in SOI. They used a low amorphisation energy, situating defects nearer the Si surface and the peak of the B distribution without fully taking advantage of another possible interface for interstitial recombination, the BOX interface.
1.8 SUMMARY

Smaller, faster, cheaper electronic products are the focus for next generation CMOS devices. To reach this goal device geometries must be scaled down, with s/d extension regions for B required having small $X_j$ and low $R_s$. To overcome the problems of channelling of B atoms during implantation, the pre-amorphisation technique is used. It also has the advantage of increasing B activation due to the SPER process. However it does have an associated problem, the formation of EOR defects below the former a/c interface. These arise due to the agglomeration of implant damage created excess interstitials.

These defects are responsible for TED and B de-activation in pre-amorphised wafers. During annealing, interstitials are released from these defects as they evolve, from clusters to (113) defects into dislocation loops. Electrical de-activation is caused due to the clustering of the B atoms with the interstitials. It is not until large thermal budgets that these defects and then eventually BICs completely dissolve to sinks like the Si surface. Tailoring of the implant and anneal conditions can reduce these effects by minimising the resultant gradient of Si interstitials from the EOR band to the surface – in order to reach the requirements set out by the ITRS.

With the incorporation of different materials for future technology generations, such as SOI, predicted by the ITRS to occur in 2008 it is important to be able to integrate current processes. With pre-amorphisation being the favoured technique, combined with advanced annealing strategies, for meeting the ITRS challenges it is natural to study its effect in SOI wafers.

Pre-amorphisation combined with SPER has a limitation in SOI, the necessity for a crystal seed to re-crystallise the amorphous layer (since the top Si layer in SOI has a restricted depth). There is however a big advantage, the ability to situate the EOR band anywhere within the top Si layer in SOI. This, coupled with the knowledge that the upper BOX interface in SOI is thought to capture Si interstitials, suggests that the additional sink could remove a portion of the Si interstitials that would normally contribute to B TED and deactivation.

The literature has also proposed a reflecting effect of Si interstitials with the BOX interface in SOI, in order to resolve this argument research into SOI wafers with pre-amorphisation should be investigated.
The evidence shown in the literature suggests several avenues for investigation of pre-amorphisation in SOI:

1. The true effect of the BOX interface in SOI (sink or reflector?), by comparing between bulk Si and SOI wafers.
2. Supposing a sink effect, the relation of the EOR defect band to the BOX interface, which can be achieved by varying Ge pre-amorphising implant energy.
3. Optimisation of the process by tailoring the implant conditions accordingly, taking care to study any additional observable effects.

The research carried out in this thesis is based upon these key points and uses them to minimise the two detrimental effects of B shown in this chapter (1) TED and (2) BICs.
CHAPTER 2 EXPERIMENTAL TECHNIQUES

2.1 INTRODUCTION

This chapter describes the theory and methodology behind the different experimental techniques used for obtaining the results used in this work. This covers material fabrication, ion implantation, RTA and a range of measurement techniques (Four point probe, Hall Effect, RBS, SIMS and TEM). It also includes a section for experimental errors for these techniques.

2.2 MATERIAL FABRICATION

Two types of wafers were used for the study in this thesis – bulk Si and SOI substrates. The method used for the growth of the bulk Si wafers in this thesis was by the Czochralski (Cz) process, named after the scientist who discovered the process Jan Czochralski. A seed crystal, mounted on a rod, is dipped into molten Si; this rod is pulled upwards and rotated at the same time – as this happens it is possible to extract a single-crystal, cylindrical ingot from the melt.

The fabrication method for the bulk Si wafers is standard however for SOI wafers this process is more complicated.

2.2.1 Silicon-On-Insulator (SOI)

There are various different techniques for the fabrication of SOI, however this work uses wafers from SOITEC© who use the Smart-cut process.

This process has the advantage that it is possible to reuse one of the Si wafers a few times, thus reducing the overall cost of the SOI wafer – it works using a combination of wafer bonding and splitting (Figure 2-1). Firstly an oxide is grown onto a “seed” wafer, which will be the BOX after bonding. Hydrogen ions are then implanted (typically \( >5 \times 10^{16} \) cm\(^{-2} \)) into the wafer through the oxide. The depth of this implant will determine the thickness of the Si overlayer [104].
Now both wafers are cleaned carefully so as to remove any surface contaminants and to make both of the surfaces hydrophilic, they are then aligned and contacted together so that they make a bond. Next the bonded wafers are split along the hydrogen implanted plane by annealing at a temperature of 400 – 600 °C. The “handle” wafer is used as a stiffener that redirects the pressure built inside the microcavities in a lateral direction. The “handle” wafer now becomes the SOI wafer and is polished to have the same surface roughness as a standard bulk Si wafer and the “seed” wafer can be reused for the same process [104].

The wafers used in this work were all obtained and subsequently implanted by Applied Materials (AMAT).

### 2.3 ION IMPLANTATION

Ion Implantation is the method used for doping the material used in this work. It is a very common technique used for doping, due to its reproducibility, precise control of dopant implant depth and dose. During ion-implantation, the dopant atoms are accelerated up to a particular energy (in this case B is implanted at 500 eV) and implanted into the Si substrate. They penetrate through the surface, colliding with many target atoms before...
losing all their energy and coming to rest. These collisions disturb the crystalline nature of Si and create disorder in the lattice in the form of point defects. Most of the implanted dopant atoms do not occupy substitutional sites in such a disordered state. In order to transfer the dopants to substitutional sites and activate them, the substrate is subjected to an annealing process [4].

2.3.1 Implanter Design

Figure 2-2 is a schematic of an AMAT xR80 Leap [14] high current implanter with its main components labelled. Although all of the implants carried out in this work were with an AMAT Quantum III, the principles are the same. For the general ion implanter case the main components are as in Figure 2-2, ion source, mass-analysing magnet, acceleration / deceleration lens and the target chamber.

![Figure 2-2 Schematic of an AMAT Quantum xR80 Leap high current ion implanter [14]](image)

The process starts at the ion source; here a filament is used to excite plasma from gaseous or solid vapour source material. A potential is then applied to extract and accelerate ions from the plasma to be mass selected. The mass analysing magnet lets the desired ions pass through for implantation; this is done by tuning the magnetic field so that only the desired ions are bent through 90°. Now that the beam is mono-energetic
it is either accelerated or decelerated to bring the ions to their desired final energy. For very low energy implants (like those carried in this work) deceleration is used.

The advantages of using an acceleration / deceleration setup are that space charge effects (where beam current is proportional to $V^{3/2}$ and hence decreases for low energy implants) are reduced due to the initial high acceleration [14]. However in this setup ions neutralised before or during the deceleration stage reach the wafer with a range of ion energies higher that the intended one. Therefore a short distance between mass analysis and deceleration is used in order to minimise this energy contamination. Generally a short beam line is used throughout in order to reduce beam blow-up (beam divergence) since this increases with distance from extraction.

The beam now reaches the target chamber, where either it is electrostatically scanned or in this case the wafer is mechanically scanned [105] through the beam to ensure a uniform dose over the whole of the wafer. An implant uniformity of <1% is achieved using the Applied Materials implanter.

Another effect of implantation is channelling of the ions deep into the substrate, unwanted since a shallow junction is required, although there are ways to avoid this by twisting and tilting the implant angles with respect to the major crystal lattice channels (see Figure 1-5). However in this work since pre-amorphisation is used, it has the advantage of avoiding channelling, therefore implantation is carried out with a 0° twist and 0° tilt.

2.3.2 Ion-Solid Interactions

As implanted ions enter the substrate they lose energy by interactions with the target atoms, there are two forms inelastic and elastic. Initially, inelastic collision occurs, by the ion exciting electrons in the substrate atoms (electronic stopping). The loss of kinetic energy here is smaller than the second type of collision. This second form, elastic collision, occurs by energy loss due to Coulombic forces (nuclear stopping).

Figure 2-3 shows a simulated B implant profile, using a program called SUSPRE a code developed by Webb [106] at the University of Surrey. Profiles of the energy loss of the implanted ions due to electronic and nuclear collisions are also shown (red curves). Integrating below those curves, gives the proportion of energy loss due to each type of collision, with the sum equivalent to the implanted energy.
The path the ion takes until it comes to rest is called the range, however a term known as "projected range" \((R_p)\) is used to describe the average depth of the implanted ions, shown by a blue line in Figure 2-3. The width of the ion distribution depend on factors like: implant energy, ion and target mass, implantation angle, substrate temperature, dose rate.

Due to the transfer of energy from the implanted ions, some target atoms are recoiled from their lattice positions. These recoils go on to move though the crystal creating their own path of damage, causing a collision cascade. During this process point defects, defect-clusters and in some cases amorphous pockets are formed. If further ions are implanted over the defected material damage accumulates and amorphous pockets overlap, causing the damaged region to become completely amorphous. The amount of damage is increased for larger ion masses, energies and doses. To form amorphous regions large ions such as Si or Ge are used, as discussed in section 1.3.2.
For this work having an amorphous layer is advantageous since it stops channelling of B in the Si substrate and is carried out using Ge as the amorphising ion. In order to remove the damage caused by the implanted ions and displaced target atoms a thermal anneal is required to return the crystalline structure to the material and to move the implanted ions from interstitial to substitutional positions, electrically activating the B (see section 1.3.1).

2.4 ANNEALING

To anneal the samples a Process Products Corporation (PPC) 18-lamp rapid thermal annealer was used, this is basically a tool that rapidly heats up samples to desired temperatures in a selected ambient – in this case N₂.

The equipment, Figure 2-4, consists of eighteen halogen lamps that are mounted inside a chamber with a gold plated reflector, 9 above and 9 below a support wafer. Samples are placed inside this chamber on top of a 5" (max size) Si support wafer (as this will not contaminate the samples). A supply of cooling water and compressed air runs around outside the anneal chamber and around the equipment so that the lamps, electronics and chamber do not overheat, these are also necessary during the anneal cycle cooling down period. To eliminate sample oxidation, nitrogen gas is constantly injected into the chamber and provides an inert ambient for the samples during the anneal cycle.

The temperature inside the chamber is measured using a K-type thermocouple which is connected underneath the wafer holder by ceramic cement. This data is constantly being monitored by the annealer controller, so that it can compensate for variation in measured temperature with programmed temperature and time.
The graph in Figure 2-5 shows a typical temperature versus time output graph, the first 2 minutes are for allowing the nitrogen gas to purge the annealing chamber. The next phase is a 1 minute hold time at 350 °C, having ramped from room temperature at 50 °C/s, this is set to allow the temperature within the annealer to stabilise. It can be seen that there is overshoot for 30 s at this stage, but this is not an issue since at this temperature it has been found that there are no measurable effects on the samples used in this work.

![Figure 2-5 Typical anneal cycle](image)

Using a ramp rate of 50 °C/s, the temperature required for annealing is reached (in this case 800 °C) and is held for 1 minute. At this stage there is no overshoot which would be undesirable, since the annealer is tuned for each annealing temperature so that there is minimal over / under shoot. The final stage is the cool down period which takes around 15 minutes for the sample to return to room temperature. A series of experiments and procedures have been undertaken to assess the errors involved during the thermal anneal cycle and are reported in section 2.11.2.

After the samples have been annealed and electrically activated they are ready to be characterised to see what effects the annealing has had on the samples.
2.5 ELECTRICAL CHARACTERISATION

In order to electrically characterise the samples, so as to find out how many dopant atoms are sitting in lattice sites, their resistivity and the mobility; two measurements techniques have been used, these are respectively four point probe (4pp) and the Van der Pauw technique.

2.5.1 Four Point Probe Measurements (4pp)

Initially the sample sheet resistance (R_s) is measured using a 4pp. This is a widely used technique as it is a quick and easy method of characterising the electrical properties of a conducting material.

It basically works by introducing a current and then measuring a voltage (all via four probes), the forward and reverse voltages are also measured to minimise errors.

Sheet Resistance (R_s)

The sheet resistance (R_s) of a sample is the resistance per unit square of that sample. Figure 2-6 shows a rectangular block of uniformly doped material with a resistance ‘R’. The resistance is determined by the resistivity of the material and the ratio of length to area, as defined in Equation 2-1. This equation also shows the derivation from resistance to R_s, which is dependant on width to length ratio.

\[ R = \frac{\rho \times L}{A} \]

- Since \( A = W \times t \) then \( R = \frac{\rho \times L}{W \times t} \)
- Since \( R_s = \frac{\rho}{t} \) then \( R = \frac{R_s \times L}{W} \)

Figure 2-6 Sheet Resistance Block

For this sample the resistance is \( R = \frac{\rho \times L}{A} \)
• Since $R = \frac{V}{I}$ then $R_s = \frac{R \times W}{L} = \frac{V}{I} \times \frac{W}{L}$

Equation 2-1 Sheet Resistance derivation (Ω/sq)

Where;

$R_s$ is the sheet resistance (Ω/□)
$R$ is resistance (Ω)
$\rho$ is the resistivity (Ω·cm)
$t$ is the thickness (Å)
$V$ is the voltage (V)
$I$ is the current (A)
$W$ is the width (cm)
$L$ is the length (cm)
$A$ is the area (cm²)

Description of equipment:

The $R_s$ is measured using a 4pp and is comprised of two components; a current source and a voltmeter. From the diagram in Figure 2-7 it can be seen that there are four pins that just penetrate the surface of the sample – the two outer pins (1 and 4) supply the current (I) and the two inner probes (2 and 3) measure the voltage (V).

![Figure 2-7 Diagram of 4pp measuring, where 'W', 'L', 't' and 's' represent sample width, length, thickness and probe spacing](image)

For an accurate reading the probe should be placed at the centre of the sample, having measured the voltage, the value for the $R_s$ can be found – using Equation 2-2.
Correction factors:

A geometric correction factor ‘CF’ is required to convert the voltage / current ratio measured by the 4pp into a $R_s$, due to the finite size of the sample. This correction factor accounts for the sample size (L / W ratio), shape, thickness and probe spacing. Therefore the $R_s$ measured by the probe is:

\[
R_s = \frac{\rho}{t} = \left(\frac{V}{I}\right) \times CF_1 \times CF_2
\]

Equation 2-2 Sheet Resistance including Correction Factors (Ω/sq)

Where;
CF$_1$ is correction factor one (L / W ratio)
CF$_2$ is correction factor two (t / s ratio)
The probe spacing (s) in this case 1 mm is constant, but the width and length of the samples vary (e.g. W = 7 mm and L = 14 mm → L / W = 2).

CF$_1$ varies depending on the sample, but is found from the width to length ratio and with the diameter (d) to the probe spacing ratio. CF$_2$ is a combination of thickness of the conducting layer and probe spacing. A table of these can be found in Appendix A – Four Point Probe Correction Factor Tables [107].

A disadvantage of this method is that as the probe heads penetrate the sample they may go in deeper that the thin USJ hence for example measuring the substrate. Therefore this method for finding $R_s$ has been used throughout this research for quick comparisons between samples. However the Van der Pauw technique was used for the results sections of this thesis since it is also possible to ascertain, as well as the $R_s$, carrier density and from these the mobility.

2.5.2 Van der Pauw Measurements

A technique developed by Van der Pauw showed a method of calculating the resistivity and Hall coefficient of a sample of arbitrary shape. Requirements for measurement are:
(1) four ohmic point contacts that can be placed at arbitrary positions, (2) at the periphery of the sample, (3) the sample is free of holes and (4) the thickness is uniform throughout [108].
Since it is difficult to physically contact the edge of small samples with point like
precision, meeting the Van der Pauw requirements, an alternative method was used in
this work. A clover leaf pattern as shown in Figure 2-8 is the method employed, since the
leaves provide a large area for contacts and are themselves edge contacts to the central
region [110]. Another advantage of this sample geometry was shown by Van Daal et al.
[111], who measured the errors caused by surface contacts on samples with and without
clover leaf patterns. They showed that the pattern can reduce the contact errors by up to
a factor of 10. Fabrication of this pattern is discussed in section 2.6.

![Clover leaf pattern used for Van der Pauw measurements](image)

**Sheet Resistance**

Using the sample as in Figure 2-8, the $R_S$ can be found by applying a current ($I$) to two of
the contacts and then a voltage ($V$) read across the other two (similar to the 4pp
method). This process is repeated following an anticlockwise rotation. E.g. introducing $I$
into 1 and out of 2 gives $I_{12}$ and subsequently the $V$ measured between 4 and 3 is found
$V_{43}$, from these the resistance $R_{12,43}$ can be found, similarly $R_{23,14}$ also, these are shown
by the following relations:

$$R_{12,43} = \frac{V_{43}}{I_{12}} \quad R_{23,14} = \frac{V_{14}}{I_{23}}$$

Equation 2-3 Clover Leaf Pattern Contact Resistances ($\Omega$) [108]

These relations are used in the equation established by Van der Pauw for $R_S$
calculations:

$$\exp\left(-\frac{\pi}{R_S} R_{12,43}\right) + \exp\left(-\frac{\pi}{R_S} R_{23,14}\right) = 1$$

Equation 2-4 Van der Pauw Sheet Resistance [108]
To simplify the equation, assuming there is a line of symmetry through contacts 1 and 3, then $R_{12,43} = R_{23,14}$ allowing $R_s$ to be solved as:

$$R_s = \frac{\pi}{\ln(2)} \times R_{12,43}$$

Equation 2-5 Symmetrical Case $R_s$ (Ω/sq) [108]

Generally $R_s$ can not be expressed as in Equation 2-5, however the solution can be written in the form:

$$R_s = \frac{\pi}{\ln(2)} \times \frac{R_{12,43} + R_{23,14}}{2} \times f$$

Equation 2-6 $R_s$ General Case (Ω/sq) [108]

Where, $f$ is a correction factor which is a function of the ratio $Q = \frac{R_{12,43}}{R_{23,14}}$ [108], [109]. For $Q > 1.5$ the result is unsuitable, indicating poor contacts or a non uniform layer. Using the same sample it is possible to not only measure the $R_s$, but also the carrier density by means of the Hall Effect.

**Hall Effect**

In 1879, Edwin H. Hall discovered that by applying a current through a metal strip in a magnetic field created a corresponding voltage perpendicularly across it [112]. This known as the Hall voltage ($V_H$) and is a direct method for calculating the carrier density of a material, as explained by the subsequent process.

It works on the principle of the Lorentz force. This describes how an electron moving along a direction perpendicular to an applied magnetic field will experience a force acting normal to both directions and it moves in response to this force [113] as expressed in Equation 2-7.

$$F = -q \nu_d \times B$$

Equation 2-7 Lorentz Force (N)

Where;

- $F$ is the Force (N)
- $q$ is the elementary charge ($1.602 \times 10^{-19}$ C)
- $\nu_d$ is the drift velocity (m/s)
- $B$ is the magnetic field (T)
This is shown schematically in Figure 2-9, where an n-type, bar-shaped semiconductor with width (W) and thickness (d) has carriers predominately electrons of bulk density \( N_s \). Applying a current (I) flowing in the positive x-axis through the bar, in the presence of a magnetic field (B) in the positive z-axis, will subject a force on the electrons from the current line toward the negative y-axis direction. This results in an excess surface electrical charge on the side of the sample. This charge results in the Hall voltage (\( V_H \)) a potential drop across the two sides of the sample, in the y-axis direction [8], [113]. (Note that the force on holes is toward the same side because of their opposite velocity and positive charge).

To measure the Hall voltage, a sample with a clover leaf pattern as in Figure 2-8 is used. A current (I) is forced through the opposing pair of contacts 1 and 3 and the Hall voltage \( V_H (= V_{24}) \) is measured across the remaining pair of contacts 2 and 4. Once the Hall voltage is acquired, the hall coefficient (\( R_{HS} \)) can be calculated:

\[
R_{HS} = \frac{V_H}{I \times B}
\]

Equation 2-8 Hall coefficient with respect to \( V_H \) (m\(^2\)C\(^{-1}\)) [108], [114]
Subsequently the carrier density \( N_s \) can be calculated using the relation:

\[
R_{HS} = \frac{r}{q \times N_s}
\]

Equation 2-9 Hall coefficient \( \text{m}^2 \text{C}^{-1} \) with respect to \( N_s \) [108], [114]

Where ‘r’ is the hall scattering factor and is due to scattering of carriers caused by the presence of the magnetic field. It is difficult to say what value of scattering factor to use because of the complicated scattering mechanisms involved. It has been reported to be \( \sim 0.8 \) for a B concentration of \( 5 \times 10^{17} \text{ cm}^{-3} \) [115], however for high B concentrations (\( >1 \times 10^{18} \text{ cm}^{-3} \)) it tends to approach 1 [116], [117] and its this value that has been used in this work. It is important to note that the scattering factor is not involved in measuring the \( R_s \).

Now that the \( R_s \) and \( N_s \) have been measured, the hall mobility can be calculated using the following expression:

\[
\mu_H = \frac{R_{HS}}{R_s}
\]

Equation 2-10 Hall mobility \( \text{cm}^2 \text{V}^{-1} \text{s}^{-1} \) [114]

The results obtained for resistivity and Hall measurements from a randomly selected sample used in this work were used to check the equations quoted in this section. This is summarised in a table in Appendix B – Hall Results from Theoretical Calculations, displayed in the fashion of a typical printout from the Hall system measurement software.

In order to carry out these measurements a series of processing steps were necessary for sample preparation, described in the next section.

2.6 PROCESS STEPS

2.6.1 Sample Preparation

Samples for this study were prepared from 8" (200 mm) wafers implanted at AMAT, using a Quantum III Implanter, with an implant orientation of 0° tilt and 0° twist.

The wafers were cleaved using a diamond scribe into 1 x 1 cm samples. Each sample was cleaned before any processing took place, to remove surface particles / organic impurities. The method used was a 3-stage clean and involved the use of 3 different
chemicals, Acetone ($\text{(CH}_3\text{)}_2\text{CO}$), Methanol ($\text{CH}_3\text{OH}$) and Isopropyl Alcohol (IPA) ($\text{(CH}_3\text{)}_2\text{CHOH}$). The steps used to accomplish this were as follows:

1. The samples were submerged in a Petri dish of boiling acetone (100°C) for around ~5 minutes.
2. Then transferred into a Petri dish of Methanol (100°C) for ~5 minutes.
3. IPA was used for the final stage, but this time at room temperature and for ~5 minutes.
4. Straight after removing them from the IPA they were washed in deionised (DI) water and each one was blown-dry with $\text{N}_2$.

After cleaning samples were annealed and then cleaned again before the photolithography process.

There are quite a few steps required to make a successful clover leaf pattern on a sample ready for Van der Pauw measurements. The individual steps for photolithography and etching of the samples are described in this section here.

### 2.6.2 Photolithography

Photolithography is the process of transferring geometric shapes from a mask on to the surface of a Si wafer. The steps involved in the photolithographic process are photo resist application, ultra violet (UV) exposure, pattern development, sample checking and sample baking. All of which will be described in detail here:

1. After the 3-stage clean, samples should be baked on a hotplate between 120 °C to 140 °C for desorption of $\text{H}_2\text{O}$ [118].
2. Next a sample is placed onto a spinner and then a positive photo resist s1828 is applied and should cover the sample. The spinner is turned on and set to ~5000 rpm for 1 minute; this gives a film thickness of about 2.8 $\mu\text{m}$ [119].
3. At the end of the spin cycle the sample is removed and soft baked at 100 °C for 70 seconds. This helps to avoid sample sticking / contamination of the mask by reducing the solvent content [118].
4. A Quinter 7000 series mask aligner was used in this work for exposure. The sample is placed on a tray in the mask aligner where a complete pattern is centred on the sample and then exposed to UV light for 15 seconds. This
converts the exposed regions of resist into an indene carboxylic acid which is soluble in a developer solution [118].

5. MF-319 developer has been formulated for use with the s1800 series resists and is desirable to avoid potential sources of metal ion contamination. Samples are submerged in this solution for around 40 s to 60 s until a clear clover leaf pattern can be seen [120]. The sample is then rinsed off with DI water and dried with N2.

6. The sample is checked under a microscope for any anomalies in the pattern. Once a good pattern has been achieved, the sample is hard baked on a hot plate at 100 °C for 30 minutes. This increases the thermal, chemical and physical stability of the resist for subsequent processes, in this case etching [118].

2.6.3 Etching

In order to make accurate Hall electrical measurements it is important that the B doped layer be completely electrically isolated from the substrate. This requires a uniform etched mesa structure deeper than the Xj or for SOI the BOX depth.

To accomplish this an isotropic wet chemical etch was carried out using a Hydrofluoric acid (HF), Nitric acid (HNO₃) and DI water (H₂O) mixture. It works by the HNO₃ oxidising the Si through a chemical reaction releasing hydrogen, then the HF etches this oxide releasing H₂O. Etch rate is dependant on the ratios of HF: HNO₃, solution temperature and dopant dose [118].

Two mixtures were created for etching the different materials:
- Bulk Si samples etch solution ratio: 21 [HNO₃] : 12.5 [H₂O] : 4 [HF 40%), removes ~1 μm in 35 s.

To measure the etch depth a Rank Taylor-Hobson Talystep was used, from this an etch rate could be calculated. Etching was carried out at room temperature, since the etch solution is sensitive to temperature variations. With each new solution a new etch rate was measured using dummy samples, equivalent to those to be studied.
Once the desired etch rate was achieved from the test samples the etching process could begin. The steps were, submersion of a sample in etch solution, then rinsing in DI water and drying with N$_2$. Finally the samples were 3-stage cleaned in order to remove the mask and were now ready for measuring.

2.6.4 Measurements

Before being able to measure the samples, contacts must be placed at the four corners of the pattern. This is done using a very fine paintbrush to paint a liquid metal called Indium Gallium Eutectic on the four corners of the pattern. The Hall equipment used was an HL5500 Accent Machine, shown in Figure 2-10.

![Figure 2-10 Pictures of the Hall equipment (left) HL5500 Accent Machine, and sample mounting compartment (right)](image)

Once the samples are ready, four tiny probes are delicately placed on the contacts, the lid is closed and the sample is now ready for being measured. An example of a typical results printout from the Hall software is shown in Appendix C – Typical Set of Hall Results.

Electrical results in this work were compared with structural analytical techniques, in order to gain a further understanding of the effects seen in the samples. To gather information on amorphous layer thicknesses the following technique was used.
2.7 RUTHERFORD BACKSCATTERING (RBS)

2.7.1 Theory

Rutherford Backscattering Spectrometry (RBS) analysis is performed by bombarding a sample target with a monoenergetic beam of high energy particles, typically Helium (He), with energy of a few MeV. A fraction of the incident atoms are backscattered by the target in the near surface region and are detected with a solid state detector which measures their energy. The energy of a backscattered particle is related to the depth and mass of the target atom while the number of backscattered particles detected from any given element is proportional to concentration. This relationship is used to generate a quantitative depth profile of the upper 1 to 2 μm of the sample. Alignment (channelling) of the ion beam with the crystallographic axes of a sample permits crystal damage and lattice locations of impurities to be quantitatively measured and depth profiled. The primary applications of RBS are the quantitative depth profiling of thin film structures, crystallinity, dopants, and impurities.

RBS attempts to find out sample composition, quantity and location in order to accomplish this a few concepts are used [121]:

1. **Kinematic factor**: the ratio of energy loss of a projectile (e.g. He) before and after colliding with a target atom (e.g. Si). The energy loss is dependent on the target atomic mass which is a factor in determining the type of atom, i.e. the composition.

2. **Scattering Cross Section**: a cross-sectional area that determines how frequently (in terms of probability) a scattering event will likely take place. Its magnitude is proportional to the square of the atomic number of the target atom, i.e. quantity of the atomic composition.

3. **Stopping Cross Section**: describes the measure of the rate of energy loss per distance of target that the ion travels through. This energy loss allows a depth distribution to be obtained.

4. **Energy Straggling**: a spreading in beam energy arising from statistical fluctuations in the energy lost in collisions along the ions' trajectory through the sample. This limits the energy resolution translating to a loss in resolution of depth and mass of the element being analysed.

In addition to elemental compositional information, RBS can also be used to study the structure of single crystal samples. When a sample is “channelled”, the rows of atoms in
the lattice are aligned parallel to the incident ($^4$He$^+$) ion beam. The bombarding He will backscatter from the first few monolayers of material at the same rate as a non-aligned sample, but backscattering from buried atoms in the lattice will be drastically reduced since these atoms are shielded from the incident particles by the atoms in the surface layers. For example, the backscattering signal from a single crystal Si sample which is in channelling alignment along the $<100>$ axis (see Figure 1-5) will be approximately 3% of the backscattering signal from a non-aligned crystal or amorphous Si. By measuring the reduction in backscattering when a sample is channelled, it is possible to quantitatively measure and profile the crystal perfection of a sample or determine its crystal orientation.

2.7.2 Channelling and Glancing Incidence

A channelled beam is where the ion beam is aligned parallel to the rows of atoms in the lattice. In this process lattice atoms "hide behind" the surface atoms and are therefore not scattering targets. Interstitial atoms (such as crystal damage) are scattering targets and therefore contribute to the backscattering yield. Therefore the interstitial fraction can be calculated using non-aligned (random) and aligned (channelled) data.

In order to achieve a better depth resolution the angle of incidence of the beam is changed by 45°, so it is now no longer normal to the sample, but still is in the channelled $<110>$ (see Figure 1-5) position. This means that the beam now comes in near the surface of the sample, it will travel longer through the sample and exit from the surface. Therefore having covered a larger distance and a better relationship of depth versus energy can be achieved.

2.7.3 Accelerator and RBS Chamber

The equipment used for carrying out the RBS was a 2 MV Tandetron accelerator from High Voltage Engineering Europe, at the University of Surrey Ion Beam Centre. RBS was carried out with ~1.5 MeV $^4$He$^+$ beam.

The depth profiling beamline (RBS) is equipped with a 6 movement goniometer from Arun Microelectronics Ltd. This instrument is capable of loading entire 100 mm wafers or single samples. The target chamber is cryopumped with a base vacuum below 1 nbar. It is possible to carry out channelling, random and glancing beam incidence measurements (higher depth resolution). Depth profiles are extracted automatically from RBS, spectra are analysed using the revolutionary Ion Beam Analysis (IBA) DataFurnace software developed at Surrey [122].
Two solid state detectors are used for collecting the backscattered particles with scattering angles of 147.7° (IBM), 166° (Cornell); solid angles 3.5 and 1.25 msr respectively.

2.7.4 Methodology

The accelerator is turned on and set to produce a beam energy of ~1557.5 keV $^4$He$^+$ (includes extraction and doubly accelerated voltage). Once a beam with a high enough beam current is produced, typically ~20 μA (higher the current, faster collection of data), a calibration sample is measured. This sample is made up of Au/Ni/SiO$_2$/Si and is used in order to find the channel number for those elements in order to set up a Geometry file (used by the Data Furnace).

To find the position of the axial channel the sample is moved with respect to the beam so that the beam is aligned (by moving the goniometer) along the <100> direction. This is observed by a decrease in the number of counts, exhibited by a trough with the optimum aligned position at the centre. Random spectra are collected ~7° away from the channelling direction. Glancing incidence channelling or random spectra are collected at 45° from the normal positions.

To analyse the spectra with the Data Furnace some information is required, the incident ion energy and the detector angles. A gain and offset value (fitting parameters) are extracted from the channel numbers measured from the calibration sample. This is carried out by the Dual Trace program (software developed for controlling the goniometer and data collection). Now one can proceed to analyse the data using the Data Furnace.

2.7.5 Data Furnace

The IBA Data Furnace fits the data to elemental depth profiles using a simulated annealing algorithm [122]. Figure 2-11 shows two typical RBS channelled spectra, the red spectrum is normal channel and the blue is glancing exit.
Figure 2-11 RBS spectra for bulk Si samples pre-amorphised with 42 keV $1 \times 10^{15}$ cm$^{-2}$ Ge, the red and blue spectra represent the normal and glancing channel respectively.

The data is plotted as counts versus channel number, in which the counts are proportional to the number of particles with a particular energy and the channel number is directly proportional to the energy of the backscattered He. This case is for bulk Si pre-amorphised with 42 keV $1 \times 10^{15}$ cm$^{-2}$ Ge. The peak at around channel number 480 is an electronic test signal; the next two peaks around channel number 190 are the a-Si peaks, the rest of the signal after that is the Si substrate.

Using the Data Furnace a fit can be made by suggesting layer thicknesses and atomic ratios, the simulation is then ran to get the best fit between experimental and simulated data. This is shown in Figure 2-12, where the symbols represent experimental data and the solid lines are the fits. It is important to get a good fit as possible in the area that is being investigated. Now the data has been fitted, the amorphous peaks can be integrated and translated into thin film units, which can then converted into a thickness (nm).
Figure 2-12 Data Furnace fitting, red and blue symbols represent the data and green and red curves are the fits.

Figure 2-13 is the best structure plot of the fitted data. The line shows the position of the a/c interface. The amorphous layer is ~64 nm thick.

Information about the B depth distribution is another requirement for this work. Unfortunately RBS is not very sensitive to light elements such as B, therefore an alternative technique is used for carrying out the B depth profiling.
2.8 SECONDARY ION MASS SPECTROMETRY (SIMS)

Secondary Ion Mass Spectrometry (SIMS) is a sensitive elemental technique that can carry out concentration depth profiling for a range of elements, including B. It basically works by bombarding a sample surface with a primary ion beam followed by mass spectrometry of the emitted secondary ions.

If a surface is bombarded with a primary beam of low energy ions, typically up to 20 keV. The energy transferred from these ions to the host atoms causes a fraction of them to become ionised and sputtered away from the surface. An example of this is shown in Figure 2-14. The incident ions are usually oxygen or caesium, since these elements are more likely to ionise the atoms emitted from the surface, enabling them to be detected. The sputtered ions are detected and analysed, using a mass spectrometer, to determine the sample composition. As well as calculating the concentration of all the impurities in the sample.

![Figure 2-14 Schematic of the sputtering of a sample](image)

The continual bombardment of a primary beam forms a crater in the sample with depth increasing with time. The secondary ion count rate is monitored with time in order to convert this into a depth scale. This is done by measuring the crater depth after experimentation using a profilometer. Crater depth divided by the total sputter time provides the average sputter rate [123]. To increase the accuracy of the depth measurement, which is important for shallow depth profiling, the sample can be rotated during analysis. This drastically reduces the roughness at the crater base when measuring the depth [124].
2.8.1 Methodology

All of the SIMS carried out in this work were made at the ‘Centro per la Ricerca Scientifica e Tecnologica’ (ITC-irst) in Italy. A CAMECA Wf SC-ULTRA was used with a 0.5 keV O₂ beam at 68 °C incidence angle. Oxygen flooding to the surface of the sample and the stage rotation during the analyses was used in order to avoid ripple formation. Under these conditions the degradation of depth resolution due to recoil mixing was expected to be ~2 nm/decade [124].

2.9 TRANSMISSION ELECTRON MICROSCOPY (TEM)

This is a technique used to visualise and analyse nanostructures, in this work it is used for cross sectional and plan view visualisation of samples.

TEM can provide information such as:

- Morphology (size, shape and arrangement of particles that make up the sample)
- Crystallographic Information (sample atomic arrangement, detection of defects in the sample)

A Transmission Electron Microscope works similar to a slide projector. Where a projector shines (transmits) a beam of light through the slide, as the light passes through it is affected by the structures and objects on the slide. These effects result in only certain parts of the light beam being transmitted through certain parts of the slide. This transmitted beam is then projected onto the viewing screen, forming an enlarged image of the slide. In TEM the microscope passes a beam of electrons through a thinned sample, where part of it is transmitted and after magnification is projected onto a phosphor screen for the user to see [125].

Figure 2-15 is a schematic representation of a transmission electron microscope, the virtual source at the top represents an electron gun. The condenser lenses and aperture focus and restrict the beam, after which it impinges on the sample at high energy with some of the electrons transmitted through the specimen. The transmitted portion is focused by the objective lens into an image and at the focal plane of the lens, a diffraction pattern is created. Below the lower focal plane, an inverted image of the specimen is formed. These images are magnified by the lenses below the specimen. The selected image is made visible when the electrons impinge on the fluorescent screen at the base of the microscope, and this is recorded by a digital camera [125].
2.9.1 Methodology

TEM was carried out at ‘CNR-IMM Sezione di Bologna’ in Italy. Cross-sectional TEM (XTEM), high resolution XTEM (HREM) and plan-view (PTEM) observations were carried out in Weak Beam (WB) mode, using a F.E.I. Tecnai F20 electron microscope operating at 200 kV. The depth scale on the samples have a ±3 nm error.

2.10 SIMULATIONS

Simulation software has been used throughout this thesis to help plan experiments and also to help the understanding of some of the results.

2.10.1 Re-growth Program

To predict the amount of SPER that would occur for the amorphised samples in this work a program using activation energies from Olson et al. [22] and Haynes et al. [24] was used. This re-growth process has been discussed in detail in section 1.3.1. It was written by Cowern in the programming code FORTRAN for other applications, however has found itself useful with this work also. A copy of this code can be found in Appendix D – Thermal Budget SPER Program.
It is based on an Arrhenius-type expression:

\[ \nu = \nu_0 \exp \left( -\frac{E_a}{k_B T} \right) \]

\textit{Equation 2-11 SPER velocity (m/s) [22]}

Where:
'\(\nu\)' is the solid phase epitaxial growth velocity (m/s),
'\(E_a\)' is the activation energy (eV),
'\(k_B\)' is Boltzmann's constant of (8.617343 \times 10^{-5} \) eV/K,
'\(T\)' is the temperature (K)

The program requires the user to create an input file with a temperature-time profile at 0.1 s intervals. When it is ran it calculates the amount of re-growth using Equation 2-11 at each time interval. As mentioned it uses two different activation energies and averages the result for a final value of re-growth.

These values for activation energy are for intrinsic Si, most of the samples used in this work were doped with B and this has been taken into account when comparing the expected with the experimental amount of re-growth.

The input file used was adapted from real temperature-time profiles that are outputted from the annealer software. It is worth noting that the program was originally written with a temperature correction of +2 °C and was taken into account when carry out the simulations.

These simulations were carried not only to predict re-growth but also to check any error of the annealer temperature by using un-doped Si samples, as discussed in section 2.11.2.

\textbf{2.10.2 Cascade}

To estimate the defect distributions (vacancy and interstitials) after Ge implantation into Si and SOI wafers two simulation codes were used. The first Monte Carlo (MC) program, called "Cascade" was developed by Webb [126]. Although there are other MC programs, most commonly TRIM (Transport of Ions in Matter) [127], Cascade is able to run on high powered severs with a simple user interface, hence reducing computational time.
The formulation for this program is out of the scope of this thesis; however its main assumptions are as follows [94], [128]:

1. The target substrate is assumed to be amorphous
2. Interactions between the incident ion and the individual target atoms are treated as a binary collision, ignoring the influence of neighbouring atoms.
3. Ziegler, Biersack and Littmark (ZBL) stopping powers are used [129].
4. In each binary collision one atom is assumed to be initially stationary.
5. The implant is equivalent to one at absolute zero, and therefore no dynamic annealing or damage evolution takes place.

As stated in the first assumption, this simulation program assumes the target material is amorphous. However this is not the case in this work, where single crystalline Si wafers are used that are then amorphised with Ge. And it is the implant distribution of Ge in the original c-Si and the corresponding damage distribution that is of interest in this work. Therefore another simulation program was used, to compare with this one.

2.10.3 KING

The MC simulation program called "KING" was developed by Lulli [130] at CNR–Instituto LAMEL. Its main difference with Cascade is that it can simulate implants into crystalline Si. Like Cascade simulations can also be carried out in multilayer structures, such as SOI. This is particularly important for simulating the implant tail of the implant species in Si, which would be shorter in an amorphous material since channelling is reduced.

Another side benefit of this program is that it can also output the amorphous fraction in the material as a function of depth [131], which is quite useful to compare with experimental data.

This chapter has described many experimental techniques, processing, electrical, structural and simulative. However in order to have confidence in the results an understanding and measurement of the uncertainties involved is necessary.
2.11 MINIMISING ERRORS

Never is the case that an experiment is error free and this is why the accuracy of the results in this report must be considered, especially since several different process steps and measuring equipment have been used.

2.11.1 Implantation

All implants were carried out at Applied Materials and are stated to have uniformity of <1%.

2.11.2 Annealing

There are a few variables when annealing, temperature, ramp rate, hold time, overshoot and undershoot. Desired temperature, time and ramp rate are set by the user, although over / under shoot can only be minimised by optimising the PID (Proportional Band, Integral, Derivative) settings for each anneal temperature (trial and error is usually the only solution to find these optimum settings).

Once the anneal cycle has been optimised, the next issue is to achieve a uniform anneal temperature over all of the samples and to check the accuracy of anneal temperature reading.

Uniformity test

Ways of optimising the temperature uniformity across the whole of the 5" wafer holder during any one anneal are: balancing of the lamp powers, adjusting the flow of the nitrogen over the wafer and minimising the cement used to mount the thermocouple to the underside of the wafer (since the cement can act as a localised heat sink).

Work was carried out to minimise the errors involved in the annealing uniformity. The first step was to anneal a test wafer (bulk Si implanted with 2 keV B) and to map the $R_S$ over the whole wafer. From this it was possible to determine the areas on the wafer that had temperature variations, shown in Figure 2-16a. This gave a variation in $R_S$ from front to back of 8.5%. It was speculated that the reason the $R_S$ was higher at the front (at the flat) of the wafer, was because the temperature was cooler. Possibly due to the flow of the cold N$_2$ which is introduced into the front of the chamber.
The lamp setup of the annealer is 3 sets of 3 lamps above and below the support wafer, distributed in a straight line. To compensate for this temperature gradient the power to the lamps was staggered so the front lamps were hotter than the rear lamps.

After this tuning another identical wafer was remapped, Figure 2-16b, now the variation across the wafer from front to back was 0.9%. Although there was still a large $R_S$ drop (2.6% from the mean) on the left hand side of the wafer.

The next test was to use a set of nine 1 x 1 cm samples that were more relevant to this work. Bulk Si amorphised with 20 keV $1 \times 10^{15}$ cm$^{-2}$ Ge and subsequently implanted with 500 eV $2 \times 10^{15}$ cm$^{-2}$ B. These were annealed at 950 °C, a high temperature where a larger temperature variation is expected. These were spread across the support wafer as shown in Figure 2-17. Assuming the centre sample is the most accurate due to the close proximity of the thermocouple, the outer most samples showed a difference in $R_S$ of: top = -1.87%, bottom = +4.84%, left = -3.20%, right = +1.28%.
It is clear from these results and the wafer maps in Figure 2-16 that the right hand side of the wafer appears to have better uniformity and a smaller error from the centre. Therefore an area was selected on this side of the wafer, shown by a blue dotted rectangle in Figure 2-17. This area was used to test a further set of eight identical samples, occupying the space within the rectangle.

Again this set was annealed and measured by 4pp; however they now showed a standard deviation of ±1%. Therefore it was within this area where all samples used in this research were placed for all anneals.

**Absolute temperature**

Now that the anneal cycle and anneal uniformity had been optimised, it was necessary to determine the absolute temperature experienced by the samples. That is the difference between the temperature readings from the thermocouple with the actual sample temperature. The method used to achieve this was to carry out re-growth measurements on bulk Si and SOI samples. Then compare the experimentally measured amount of regrowth with that predicted by simulation (described earlier in section 2.10.1).
Bulk Si and SOI samples, pre-amorphised with 20 keV 1x10^{15} \text{ cm}^{-2} \text{ Ge only, were annealed at 570 °C for 54 s. The as-implanted amorphous thickness was 38 nm (determined by RBS). Simulations predicted that for this anneal budget there would be a 50% re-growth, therefore 19 nm of re-growth.}

First a check between the re-growth in bulk Si and SOI samples showed that there was no difference between the two types of material, both re-grew by equal amounts. The next check was to see whether the amount of re-growth simulated was the same as the actual experimental value. It is known that B enhances re-growth [22], therefore only samples without B implants were compared.

The results showed that the remaining amorphous layer thickness after annealing was larger than expected (less re-growth than expected occurred). Re-simulating the re-growth at lower temperatures (where SPER is slower) for the same times found a difference of ~7 °C. Therefore the re-growth annealing temperature from the simulations that agrees with the experimental data for the same anneal times is 563 °C. These results show a 7 °C difference between simulated temperature and that measured experimentally, which is in the order of ~1% for this temperature range. Also this is consistent with the thermocouple error which is known to be around ±7 °C.

**Repeatability**

Throughout the course of this PhD many samples have been annealed at different points in time. In order to be able to compare between samples annealed at the same temperature but during a different anneal cycle it is important to be sure that the anneal cycles were reproducible, shown in Figure 2-18.

Data acquisition of the temperature profile is carried out in real time using a program that interfaces with the PPC annealer controller, designed by Benson et al. [132]. This is then easily transferred to a graphing tool.

The anneal profiles in Figure 2-18 are for anneals that have been taken place over a period of two years. Only a selected region is shown, since this is the main area of importance when comparing between anneal cycles – the set temperature. The dotted black line is the programmed profile; comparing it with all the other profiles it is clear that there is a shift in time and temperature. These offsets are intentional in order to produce the required anneal budget of 60 s at 800 °C.
Figure 2-18 Repeatability of an anneal cycle (800 °C for 60 s) during a period of 2 years

For the initial few seconds the temperature over and undershoots by a maximum of ±5 °C, this is not expected to make a significant difference in results for subsequent measurements. For the majority of the anneal cycle the temperature is stable at 800 °C. There is a good agreement between the anneal cycles over the period of two years, providing a good confidence when comparing samples annealed separately but for the same thermal budget.

A comparison using SIMS between measurements made two years apart is described in section 5.3.2. However to summarise little difference was seen in the B depth distributions for samples (implanted with 8 keV 1x10^{15} cm^{-2} Ge plus 500 eV 2x10^{15} cm^{-2} B) annealed at 850 °C for 60 s.

2.11.3 Rutherford Backscattering (RBS)

To be able to assess the uncertainties involved in the RBS measurements an uncertainty budget needs to be prepared and is described in detail by various authors [133], [134]. More recently Jeynes et al. [135], using the RBS equipment from the University of Surrey and the Data Furnace code for sample analysis, determined a combined uncertainty for their samples of ±2.07%.
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Chapter 2 - Experimental Techniques

The values relevant for this work are based on those by Jeynes et al. [135], however the counting statistics have been determined using a range of glancing exit channelled samples from this work. These are summarised in Table 2-1. This table includes a breakdown of the different forms of uncertainties expressed as a percentage standard deviation.

<table>
<thead>
<tr>
<th>Uncertainty Components</th>
<th>IBM detector (%)</th>
<th>Cornell detector (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Counting Statistics, a-Si signal</td>
<td>0.94</td>
<td>2.89</td>
</tr>
<tr>
<td>Scattering angle</td>
<td>0.28</td>
<td>0.07</td>
</tr>
<tr>
<td>Electronic gain</td>
<td>0.5</td>
<td>0.5</td>
</tr>
<tr>
<td>Relative uncertainty</td>
<td>1.10</td>
<td>2.93</td>
</tr>
<tr>
<td>Relative uncertainty of average of two detectors</td>
<td>1.57</td>
<td></td>
</tr>
<tr>
<td>Beam Energy</td>
<td>0.20</td>
<td></td>
</tr>
<tr>
<td>Rutherford cross-section</td>
<td>0.16</td>
<td></td>
</tr>
<tr>
<td>Si stopping power</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td><strong>Total combined standard uncertainty</strong></td>
<td><strong>2.55</strong></td>
<td></td>
</tr>
</tbody>
</table>

Table 2-1 RBS Uncertainty Budget, based on [135], with counting statistics values attained from this work

In summary the total combined standard uncertainty is ±2.55% for the RBS data, this can be directly applied to the amorphous depth thicknesses.

### 2.11.4 Electrical

The measurement of the Hall voltage using the Accent 5500 can include several spurious voltages. These can be eliminated by field or current reversal. Also a misalignment voltage exists, since even when there is a zero magnet field a voltage can appear between two contacts. This also can be eliminated, by carry out measurements with and without a magnetic field. These methods of eliminating the spurious voltages are automatically carried out by the Hall software when running a sample.

To check for electrical measurement errors comparisons were made between samples masked and measured at UNIS with those by Hebras at LAAS-CNRS [136]. All of these samples (UNIS and Toulouse set) were annealed (at Mattson) with the same annealer under the same conditions.

The difference in preparation techniques was that at Toulouse gold contacts were evaporated onto the samples and also patterning was not used, instead samples were cleaved into a square and contacts placed in all four corners. Whereas at UNIS samples are masked with a clover leaf pattern (described in section 2.6) and used a conducting
liquid called Indium Gallium Eutectic for the contacts. It was found that by using a paintbrush to apply the contacts a variation in $R_s$ of ±0.5% was achieved from results from Toulouse.

Smith [94] found that the errors involved in the electrical measurements for samples with low sensitivity to anneal temperature fluctuations resulted in an $R_s$, $N_s$ and $\mu$ error of 4%, 4% and 8% respectively.

### 2.11.5 Summary

Based on the above analysis, reasonable estimates for the total uncertainty for the electrical measurements, adding implant uniformity, anneal uniformity and hall accuracy values; result in an $R_s$, $N_s$ and $\mu$ uncertainty of 6%, 6% and 10% respectively.

It is important to consider the wide spectrum of experimental techniques, that have been used in the results section to cross analyse. This support of different techniques adds further validity to the results.
CHAPTER 3  RESULTS I: AMORPHISATION AND SPER

3.1 INTRODUCTION

This chapter and the subsequent chapters discuss the results from this work, with the goal of studying the effects of using SOI as an alternative substrate to bulk Si. In particular to study the effects of different PAI energies with the aim of optimising the PAI conditions to give the maximum benefits and thus form highly activated USJs to meet the requirements of the ITRS.

Si and SOI wafers were pre-amorphised to different depths using Ge ions. Ultra low energy B was then implanted and the samples annealed using RTA at different temperatures. Details of these experimental conditions can be found in Table 3-1. Subsequent to implantation and annealing the samples were analysed using Hall Effect measurements to determine carrier density, Hall mobility and Rs. RBS and ion channelling was used to evaluate the amorphous depth prior to annealing and its subsequent re-growth during annealing. SIMS was used to determine the depth distribution of the dopant atoms after implantation and how they diffused and clustered during annealing. The presence and structure of extended defects was investigated by XTEM in order to better understand their role in the micro-structural and electrical properties of the samples.

3.2 IMPLANT MATRIX

To find the optimum implantation matrix, it was necessary to consider any constraints so that an appropriate selection of implant conditions could be made. The SOI wafers used had a 55 nm top Si layer; therefore it was necessary to choose Ge energies that did not amorphise this entire layer (otherwise no SPER would take place).

Three batches of implants were made during the course of this project; the first set was used to carry out amorphous thickness measurements. This enabled the design for the second set of experiments to be accomplished allowing electrical and micro-structural measurements. The third was used for optimisation based on the results from the previous experiments.
In all cases two types of substrates were used:

- Bulk Si wafers of n-type <100> Cz Si, with a resistivity of ~10-25 Ωcm
- SOI wafers which have a 145 nm-thick BOX and a 55 nm-thick p-type Si overlayer

The first batch of implants (Implant Batch 1) was carried out on four bulk Si wafers and one SOI wafer (Table 3-1), using different energies for the PAI. The energies were chosen to amorphise the wafers to different depths which varied from around ~10 – 70 nm. Figure 3-1 shows a plot of amorphous layer thickness Vs PAI energy. Samples from these wafers were then used to carry out SPER studies of the material, to determine the time needed to fully re-grow the amorphous layer. Table 3-1 summarises the implantation details for the first batch of wafers, it lists the material type, the amorphising Ge energy and dose.

<table>
<thead>
<tr>
<th>Material</th>
<th>Ge energy</th>
<th>Ge dose</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk Si</td>
<td>4 keV</td>
<td>1x10^{15} cm^{-2}</td>
</tr>
<tr>
<td>Bulk Si</td>
<td>12 keV</td>
<td>1x10^{15} cm^{-2}</td>
</tr>
<tr>
<td>Bulk Si</td>
<td>20 keV</td>
<td>1x10^{15} cm^{-2}</td>
</tr>
<tr>
<td>SOI</td>
<td>20 keV</td>
<td>1x10^{15} cm^{-2}</td>
</tr>
<tr>
<td>Bulk Si</td>
<td>42 keV</td>
<td>1x10^{15} cm^{-2}</td>
</tr>
</tbody>
</table>

Table 3-1 Implant details for Implant Batch 1

3.3 AMORPHOUS LAYER RE-GROWTH

As previously described in the literature review (Chapter 1), when Ge is implanted to a high dose into crystalline Si it amorphises it, to a depth determined predominantly by the implant energy but also by the dose. PAIs are used to minimise B channelling, however to activate the B atoms the wafer must be heat treated, this has the effect of re-growing the c-Si and eliminating the amorphous material. Since the Si top layer in the SOI material is 55 nm thick, amorphous depths need to be chosen within this thickness, in order to have a seed for re-crystallisation.

From previous data (provided by Applied Materials) amorphisation conditions were chosen using a Ge dose of 1x10^{15} cm^{-2} and energies of 4, 12, 20 and 42 keV for bulk Si wafers and 20 keV for SOI, as a comparison with the bulk. RBS was used in order to determine the amorphisation depths – the results of which can be seen in Figure 3-1.
The graph shows amorphisation depth versus implant energy, results from this work are bulk Si (red) and SOI (black). The difference seen between the SOI and bulk is small and within experimental error. Data from AMAT (blue) used Medium Energy Ion Scattering (MEIS), to measure the thickness of the amorphous layer. There are differences between the RBS data and that obtained by MEIS and is likely due to the way in which the depth information is determined from the two measurement methods. With MEIS the depth is calculated by measuring the thickness of the amorphous peak with a ruler, whereas the RBS measurements used a sophisticated data analysis programme (Data Furnace [122]) and integrated the counts in the amorphous peak and converted this in to a depth scale. Subsequent SIMS and XTEM analysis confirmed the RBS findings. A summary of the results are shown in Table 3-2.

<table>
<thead>
<tr>
<th>Material</th>
<th>Ge energy</th>
<th>Ge dose</th>
<th>Amorphous Depth</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk Si</td>
<td>4 keV</td>
<td>$1 \times 10^{15} \text{ cm}^{-2}$</td>
<td>12 nm</td>
</tr>
<tr>
<td>Bulk Si</td>
<td>12 keV</td>
<td>$1 \times 10^{15} \text{ cm}^{-2}$</td>
<td>25 nm</td>
</tr>
<tr>
<td>Bulk Si</td>
<td>20 keV</td>
<td>$1 \times 10^{15} \text{ cm}^{-2}$</td>
<td>38 nm</td>
</tr>
<tr>
<td>SOI</td>
<td>20 keV</td>
<td>$1 \times 10^{15} \text{ cm}^{-2}$</td>
<td>37 nm</td>
</tr>
<tr>
<td>Bulk Si</td>
<td>42 keV</td>
<td>$1 \times 10^{15} \text{ cm}^{-2}$</td>
<td>64 nm</td>
</tr>
</tbody>
</table>

Table 3-2 Summary of amorphous depths for Implant Batch 1
From this depth / energy data two amorphisation depths were selected for further study, \( \sim 19 \) nm and \( \sim 38 \) nm (confirmed by RBS), these correspond to PAI energies of 8 keV and 20 keV Ge respectively. The lower PAI (8 keV) places the EOR defects between the Si surface and the BOX interface in SOI. The other (20 keV) places the EOR defects quite close to the BOX interface and further away from the Si surface. A more detailed explanation and reasoning for this is described in section 4.1, however it is important to mention this here since these PAI energies were used for the re-growth study described in the following section.

### 3.3.1 Re-growth Comparisons

The SPER process was performed at a temperature of 570 °C, since re-growth is observable at this temperature but is much slower than at higher temperatures and consequently it allows changes due to be observed. This makes it easier to partially re-grow thin layers and also for consistency with previous studies [22], [23], [24], [137]. The anneal times chosen ranged from 30 s to 150 s, depending on the amorphous thickness, this respectively re-grew \( \sim 50\% \) and 100% for all of the samples. Glancing-exit RBS was used to monitor the re-growth of the a-Si. The amorphous depth was measured using a 1.5 MeV He beam at a glancing angle of 45° to the sample, and the resulting spectra were analysed using the IBA Data Furnace.

In order to determine the re-growth anneal times for an anneal temperature of 570 °C simulations were made using activation energies from Olson et al. [22] and Haynes et al. [24], which were incorporated into the small program described earlier in section 2.10.1. The plan was to re-grow half the amorphous layer and then to fully re-grow it, in order to determine their re-growth velocities and to make comparisons between bulk Si and SOI. The latter was to ascertain whether the re-growth velocity was the same for the two types of material. There was concern about whether the SOI substrates would vary in temperature during RTA annealing because of the presence of the BOX [138]. Comparisons between the different B doses were also made, to see whether the B influences the re-growth rate.

The anneal conditions were as follows:
- 8 keV PAI samples: 30 s for half and 60 s for full re-growth at 570 °C
- 20 keV PAI samples: 65 s for half and 135 s for full re-growth at 570 °C
The first comparison, Figure 3-2 shows the dependency of time on the re-growth.

Figure 3-2 (a) RBS spectra of the re-growth of bulk Si implanted with B at dose $2 \times 10^{15}$ cm$^{-2}$ and pre-amorphised with 20 keV Ge, before and after annealing. Inset (b) is a section of the channel number range where the amorphous peaks lie. All spectra are normalised and are normal incidence channelled except for the black as-implanted random.
In terms of the number of counts, an amorphous material is similar to that of a random spectrum since this represents the backscattered particles impinging on the surface of the sample and an amorphous material is highly disordered and therefore not allowing any channelling to occur. This is why the peak in Figure 3-2 (a) for the as-implanted channelled (red) is so high and reaches the height of the random (black) spectrum, giving an indication that the as-implanted sample is amorphous. It is also evident that the peak in terms of channel number starts together with the random sample, indicating that the amorphous layer begins from the surface.

As the samples are annealed SPER occurs which subsequently reduces the thickness of the amorphous layer and is why the amorphous peaks after 65 s (blue) and 135 s (pink) anneal times are reduced compared to the original as-implanted. This can be seen in clearer detail in the inset, Figure 3-2 (b). These results visibly show that for an increasing anneal time there is an increase in the amount of re-growth.

An extra feature of these spectra is the peak around channel number 360 which represents the Ge signal. It is at a higher channel number that the Si, due to its larger mass, giving more energy for the backscattering particles.

Having shown that increasing the anneal time increases the amount of re-growth, it is important to know what effect the presence of B has on the re-growth rate. Figure 3-3 (a) shows the amorphous peaks of the normalised spectra for bulk Si pre-amorphised with 20 keV Ge without and with B subsequently implanted to a dose of $2 \times 10^{15}$ cm$^{-2}$. The random (black) spectrum for the as-implanted sample is also shown to check that the samples have been amorphised; it is apparent that this is true for all samples and is seen more clearly in Figure 3-3 (b).

After annealing for 45 s at 570 °C the sample implanted without B is compared to that with B. Both samples exhibit a certain amount of re-growth, for the sample with B there is an increase in re-growth compared to that without B. This increase in re-growth rate is expected [20], [22], [25].

Another feature of the spectra is the small oxide peak at around channel number 125; this is the signal from the surface oxide, since in this case oxygen is lighter than Si its signal is shown to be within the Si substrate.
Figure 3-3 (a) RBS spectra of the re-growth of bulk Si implanted without / with B at a dose $2 \times 10^{15}$ cm$^{-2}$ and pre-amorphised with 20 keV Ge, annealed at 570 °C for 54 s. Inset (b) is a section of the channel number range where the amorphous peaks lie. All spectra are normalised and are normal incidence channelled except for the black as-implanted random.
Figure 3-4 (a) shows glancing exit channelled spectra for bulk Si and SOI samples implanted with B at a dose $2 \times 10^{15}$ cm$^{-2}$ and pre-amorphised with 8 keV Ge before and after annealing for 30 s at 570 °C. Three features of SOI wafers compared to bulk Si are clearly seen, (1) the oxide peak around channel number 150 which corresponds to the surface oxide, (2) the oxide peak around channel number 100 which corresponds to the BOX and (3) the dip in the spectra, just after the amorphous peak around channel number 230 is caused by the loss of Si counts in SiO$_2$ (with respect to the Si overlayer); this dip corresponds to the upper BOX interface. The spectra seem stretched compared to normal incidence channelled spectra, as in the case of Figure 3-2, since the angle of incidence of the ion beam has changed by 45° therefore increasing the penetration distance through the sample.

Comparing the amorphous peaks in Figure 3-4 (b) between SOI annealed (blue) and SOI as-implanted (red); there is a noticeable amount of re-growth. Now comparing between the SOI (blue) and bulk Si (pink) annealed samples, there is no significant difference between the two. The Data Furnace was used to calculate the amount of re-growth in both cases and the numbers showed that there was negligible difference between SOI and bulk Si wafers in terms re-growth. This serves as proof that the difference between the anneal temperatures for the bulk Si and SOI wafers are negligible. According to Mannino et al. [138] SOI experiences a lower temperature compared to bulk Si when annealed in a lamp annealer (as is the case in this work), this is due to an increased reflectivity of the incoming radiation during the anneal because of the BOX interface in SOI. However their RTA setup had lamps located only on top of the wafers, results showed that when samples were annealed facing downwards with the lamps heating from the bottom of the SOI samples, no distinguishable differences in anneal temperature between materials was noticed. This was explained by the fact that in this case the radiation is absorbed by the thick Si back layer and then travels through the whole of the wafer by a heat transport mechanism. Since in this work the RTA setup is such that lamps are above and below the samples it is reasonable to conclude that the reason that there is no noticeable difference in temperature difference between bulk Si and SOI during annealing is because of the lamp array setup below the samples.
Figure 3-4 (a) RBS spectra of bulk Si & SOI implanted with B at a dose $2 \times 10^{15}$ cm$^{-2}$ and pre-amorphised with 8 keV Ge, before and after annealing for 30 s at 570 °C. Inset (b) is a section of the channel number range where the amorphous peaks lie. All spectra are normalised and are glancing exit channelled except for the black as-implanted random, also all samples are SOI except for the pink bulk Si sample.
After carrying out all of these comparisons, a check between the simulated and actual experimentally determined re-growth was carried out. This is explained in more detail in section 2.11.2. However in summary the results showed that the samples experienced ~7 °C lower anneal temperature than expected and is consistent with the thermocouple error which is known to be around ±7 °C.

3.3.2 Re-growth Rates

Table 3-3 summarises the data collected (re-growth rate nm/sec) from the re-growth study. This data was obtained by comparing the amorphous layer thickness of half re-grown samples, with their as-implanted counterparts. The difference in thicknesses was calculated as a ratio of the anneal time, which gave the rate of re-growth at the anneal temperature of 570 °C.

Comparisons are made between PAI energies, wafer material and increasing B dose. From Table 3-3 it can be seen that the only factor influencing the re-growth rate is the dose of B. The PAI energy and substrate type have a negligible effect.

<table>
<thead>
<tr>
<th>B dose incr.</th>
<th>8keV Ge Bulk</th>
<th>8keV Ge SOI</th>
<th>20keV Ge Bulk</th>
<th>20keV Ge SOI</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>N/A</td>
<td>N/A</td>
<td>0.27</td>
<td>0.26</td>
</tr>
<tr>
<td>2x10^13cm^-2</td>
<td>0.35</td>
<td>0.37</td>
<td>0.37</td>
<td>0.39</td>
</tr>
<tr>
<td>2x10^14cm^-2</td>
<td>0.40</td>
<td>0.42</td>
<td>0.40</td>
<td>0.44</td>
</tr>
<tr>
<td>2x10^15cm^-2</td>
<td>0.52</td>
<td>0.48</td>
<td>0.52</td>
<td>0.50</td>
</tr>
</tbody>
</table>

Table 3-3 Re-growth rates for increasing B dose, comparing between PAI energy and wafer material (±0.03 nm/sec) [139]

The re-growth rates for intrinsic Si are in agreement with the literature, reported to be ~0.29 nm/s at 570 °C [22]. Also B dopant as a re-growth rate enhancer (and with increasing B dose), has also been reported in the literature [20], [22], [25].
CHAPTER 4 RESULTS II: THE BURIED INTERFACE

4.1 INTRODUCTION

In this chapter a study of the effects of the upper BOX interface in pre-amorphised SOI on behaviour of implanted B during annealing is undertaken. Various characterisation techniques (Van der Pauw, Hall Effect, SIMS and TEM) were used in order to determine the electrical and structural properties of these B implants in pre-amorphised bulk Si and SOI.

The question asked in this chapter, is whether the upper buried interface in SOI acts as a sink for interstitials released from the EOR band during annealing?

Using the results from the previous chapter, two amorphisation energies were chosen in order to study any effects of the buried interface and the importance of the position of the EOR defect band in relation to the BOX interface. This was achieved by placing the EOR defect band a) near the surface or b) near the BOX interface. The corresponding energies selected were 8 and 20 keV Ge these gave amorphisation depths of ~19 nm and ~38 nm respectively, as shown in Figure 4-1.

![Figure 4-1 Schematic representation of EOR band in SOI for an 8 and 20 keV Ge PAI](image-url)
After amorphisation both bulk Si and SOI wafers were then implanted with B to doses of $2 \times 10^{14}$ cm$^{-2}$ and $2 \times 10^{15}$ cm$^{-2}$ with energy of 500 eV. Samples from these wafers were then annealed isochronally in order to carry out activation and diffusion studies. Table 4-1 is a summary of the implantation details for this second batch (Implant Batch 2) of implants.

<table>
<thead>
<tr>
<th>Material</th>
<th>Ge energy</th>
<th>Ge dose</th>
<th>Amorphous Depth</th>
<th>B energy</th>
<th>B dose</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk Si</td>
<td>8 keV</td>
<td>$1 \times 10^{15}$ cm$^{-2}$</td>
<td>19 nm</td>
<td>500 eV</td>
<td>$2 \times 10^{14}$ cm$^{-2}$</td>
</tr>
<tr>
<td>SOI</td>
<td>8 keV</td>
<td>$1 \times 10^{15}$ cm$^{-2}$</td>
<td>19 nm</td>
<td>500 eV</td>
<td>$2 \times 10^{14}$ cm$^{-2}$</td>
</tr>
<tr>
<td>Bulk Si</td>
<td>8 keV</td>
<td>$1 \times 10^{15}$ cm$^{-2}$</td>
<td>19 nm</td>
<td>500 eV</td>
<td>$2 \times 10^{15}$ cm$^{-2}$</td>
</tr>
<tr>
<td>SOI</td>
<td>8 keV</td>
<td>$1 \times 10^{15}$ cm$^{-2}$</td>
<td>19 nm</td>
<td>500 eV</td>
<td>$2 \times 10^{15}$ cm$^{-2}$</td>
</tr>
<tr>
<td>Bulk Si</td>
<td>20 keV</td>
<td>$1 \times 10^{15}$ cm$^{-2}$</td>
<td>38 nm</td>
<td>500 eV</td>
<td>$2 \times 10^{15}$ cm$^{-2}$</td>
</tr>
<tr>
<td>SOI</td>
<td>20 keV</td>
<td>$1 \times 10^{15}$ cm$^{-2}$</td>
<td>38 nm</td>
<td>500 eV</td>
<td>$2 \times 10^{14}$ cm$^{-2}$</td>
</tr>
<tr>
<td>Bulk Si</td>
<td>20 keV</td>
<td>$1 \times 10^{15}$ cm$^{-2}$</td>
<td>38 nm</td>
<td>500 eV</td>
<td>$2 \times 10^{15}$ cm$^{-2}$</td>
</tr>
<tr>
<td>SOI</td>
<td>20 keV</td>
<td>$1 \times 10^{15}$ cm$^{-2}$</td>
<td>38 nm</td>
<td>500 eV</td>
<td>$2 \times 10^{15}$ cm$^{-2}$</td>
</tr>
</tbody>
</table>

Table 4-1 Implant details for Implant Batch 2

4.2 PROCESS STEPS

The wafers were cleaved into samples of 1 x 1 cm then annealed to see the effects of temperature on the electrical and structural properties of the samples. Since annealing is used for other processes during the fabrication steps of CMOS devices and it is necessary to have stable electrical and structural properties for a range of anneal temperatures and times. As it is a highly undesirable effect for the $R_s$ (as an example) to increase during later steps in the fabrication process. Therefore it is necessary to study these properties for a range of annealing budgets.

The temperature range here was chosen in order to reveal the deactivation and reactivation of B in bulk Si and SOI. This was 700 – 1000 °C in steps of 50 °C for times of 60 s, that is, one sample at 700 °C for 60 s and another at 750 °C for 60 s etc.

In order to measure the electrical properties of the samples, a 4pp was employed, to gather some preliminary data. Next the Van Der Pauw technique was used in order to find $R_s$, carrier density and from these the mobility. SIMS was used to study the diffusion of the B implant with increasing annealing temperature. In order to study the evolution of the defects, TEM was carried out.
Figure 4-2 (a-d) is a schematic of the evolution of the structure in the bulk Si samples during the processes steps involved in their fabrication. Figure 4-2 (e) shows the case for SOI at a point equivalent to (d) in bulk Si.

(a) Implant Germanium

(b) Implant Boron

(c) Anneal Boron in a-Si

(d) Result Boron in c-Si

(e) SOI wafer

Figure 4-2 Schematic representation of wafer implant and anneal steps for both bulk Si & SOI
(a) A bulk Si wafer is implanted with Ge to a dose of $1 \times 10^{15}$ cm$^{-2}$ with an energy of either 8 keV or 20 keV.

(b) An amorphous layer is now formed (green), the thickness of which depends on the implant energy. B is now implanted, in this case with energy of 500 eV to a dose of $2 \times 10^{15}$ cm$^{-2}$.

(c) The top layer of the wafer now contains B inside a-Si (blue on green pattern); below this is the remainder of the amorphous layer. At the interface between amorphous and crystalline Si are excess interstitials. Samples are now annealed for 60 s from 700 °C to 1000 °C.

(d) During annealing the amorphous layer re-grows as c-Si and no amorphous material remains. There is still a B rich layer close to the surface (blue on grey pattern). The agglomeration of the excess interstitials causes a band of defects to form (red layer), just below the position of the former amorphous / crystalline interface, these are called EOR defects. Below the EOR defects is the single crystal Si substrate i.e. the rest of the bulk of the wafer (grey block). Also after annealing BICs form near the peak of the B profile, which leads to dopant deactivation.

(e) In SOI the same processes occur, however now there is a BOX is the (yellow layer). The thickness of the amorphous layer is carefully controlled so that it stays within the top Si layer and does not reach the BOX interface.

Once annealed the samples undergo a 3-stage clean, and are then prepared to be masked by means of photolithography (see section 2.6.1). The Van der Pauw patterns are then developed and the mask checked for any damage. Once all the samples have been masked they are etched and rinsed in an Acetone solution, to remove the photo resist and are now ready to be measured using the Van der Pauw technique, as described in section 2.5.2.

### 4.3 ISOCHRONAL ANNEAL STUDY

#### 4.3.1 Electrical Measurements

In this section the electrical results are shown and discussed in terms of a comparison between SOI and bulk Si, as well as the effect of Ge PAI energy and of B dose.
Sheet resistance

Figure 4-3 shows a graph of $R_s$ versus annealing temperature for samples implanted with 8 keV Ge and $2 \times 10^{15}$ cm$^{-2}$ B in bulk Si and SOI. Looking initially at the bulk case there is one main feature that is apparent, an increase in $R_s$ with anneal temperature (700 °C – 800 °C), where it peaks, followed by a subsequent decrease in $R_s$ (800 °C – 1000 °C).

The rise in $R_s$ (deactivation) corresponds to the ripening of EOR defects and the release of self interstitials from the EOR defect band which diffuse towards the surface, driving clustering (in the form of BICs) and surface segregation of the B [5]. The decrease in $R_s$ after the peak (reactivation) arises from the subsequent dissolution of the BICs to nearby sinks such as Si/SiO$_2$ interfaces (in the case of SOI) and the Si surface (for both bulk Si and SOI) [5]. The red line shows the results for the SOI sample, where the trend is almost the same as for the bulk case. The SOI material starts with a slightly higher $R_s$ value than the bulk (by $\sim 100$ Ω/sq) but ends with a very similar value. Interestingly the values of $R_s$ between 775 °C – 800 °C for SOI are slightly lower than those for bulk Si (although this can be argued to be within experimental error ±6%). The $R_s$ results also correspond to a higher level of activation for SOI.

So could the BOX interface be having an effect on the defect evolution?
In the case of the samples pre-amorphised with 20 keV Ge and subsequently implanted with B $2 \times 10^{15} \text{ cm}^{-2}$ in bulk Si and SOI similar trends are found. Figure 4-4 shows the results for bulk Si and SOI, in both cases there is an increase in $R_s$ (700 °C – 850 °C), where it peaks and subsequently decreases (850 °C – 1000 °C). Again the $R_s$ values for SOI at 700 °C are higher than those for bulk Si (≈100 Ω/cm) and only after annealing at 1000 °C do they reach similar values. The value of the $R_s$ in SOI is lower than that for bulk Si between 775 °C to 850 °C and is outside the range that would be attributed to experimental error (this again corresponds to a higher level of activation for the SOI).

Comparing the two PAI conditions similar trends are seen (a) there is a deactivation / reactivation process, which is shown by an increase and then decrease in $R_s$, (b) SOI material starts with a slightly higher $R_s$ value than for bulk Si, but ends (at 1000 °C) with similar values (c) reactivation (shown by a decrease in $R_s$) for the 8 keV samples begins 50 °C earlier than for the 20 keV PAI (d) for the 8 keV samples there is less deactivation in SOI (when compared to bulk Si) and this trend is much more pronounced for the 20 keV PAI.

To explain these observations (a) is the well known ‘reverse annealing’ effect [5], (b) the difference in $R_s$ at 700 °C and 750 °C could be attributed to a difference in the two
materials. This fits with previously published observations of a lower level of B activation in SOI at 750 °C [140].

(c) The shift in the temperature for peak deactivation, between the 8 and 20 keV PAIs, is well known and is caused by a reduction in the concentration gradient of interstitials towards the B-doped region when the EOR band is located deeper into the material [5], [68], increasing the thermal budget required for them to reach the surface.

(d) This difference in the level of deactivation between SOI and bulk Si suggests that there is more electrically active B in the SOI and could be explained by arguing that the BOX interface acts as a sink for interstitials, removing some of the self interstitials that would otherwise have contributed to BIC formation closer to the surface [97].

**Activation**

Figure 4-5 is a graph showing the electrically active B dose ‘Ns’ versus annealing temperature for the two PAI conditions and two material types. As expected these results correlate with the Rs measurements.

![Graph showing electrically active B dose versus annealing temperature](image)

**Figure 4-5** Electrically active B dose after 60 s isochronal anneals (700 °C – 1000 °C) [2x10^{15} cm^{-2} B]
Upon annealing the level of activation drops in bulk Si by a factor of ~3.5 at 800 °C for the 8 keV Ge PAI and by ~3 at 850 °C for the 20 keV Ge PAI. In SOI this deactivation is less with a factor of ~2.5 for 8 keV and ~2 for 20 keV. After these trough values the samples re-activate and reach ~43% activation for bulk Si at 1000 °C and ~38% activation for SOI samples. This deactivation / reactivation process is due to the defect evolution and dissolution discussed previously for the $R_s$ results.

The differences observed in the level of activation, during the deactivation phase, between SOI and bulk Si wafers are due to the same reasons as discussed in the $R_s$ section earlier. The BOX interface appears to act as a sink for interstitials reducing BIC formation.

**Mobility**

Equation 2-9 and Equation 2-10 show that the mobility is inversely proportional to $R_s$ and carrier density. This relation is used to help explain what is happening in Figure 4-6.

![Figure 4-6 Mobility after 60 s isochronal anneals (700 °C – 1000 °C) [2x10^{15} cm^{-2} B]](image)

Using the same graph key as before, the first feature is that the 20 keV Ge samples at 700 °C have a higher mobility value than those for the 8 keV Ge PAI. The mobility
increases rapidly from 750 °C to 850 °C for the 8 keV Ge samples and then begins to saturate. For the 20 keV Ge PAI samples the mobility decreases from 750 °C to 800 °C and then increases up to 1000 °C.

Since ionised impurity scattering is dominant at room temperature and affects mobility, when more dopant atoms become substitutional the mobility is reduced. For the samples discussed here between 750 °C and 850 °C the mobility is increasing and this corresponds with a decrease in carrier density. The rate at which the mobility increases up to ~850 °C corresponds to the decrease in the number of active dopants. Above 850 °C the mobility continues to rise but at a slower rate. This corresponds to the diffusion and reactivation of the dopants, where the number of ionised dopants is increased (hence more scattering centres). Also noticeable is that the SOI samples generally have a lower mobility than the bulk Si; this was also seen by Saavedra et al. [99].

In 2004 Pawlak et al. [68] carried out isochronal anneals on pre-amorphised bulk Si wafers, Ge energies were 8, 12 & 25 keV with a dose $1 \times 10^{15}$ cm$^{-2}$ and subsequently implanted with B at 1.5 keV to a dose $3 \times 10^{15}$ cm$^{-2}$. The trends observed by Pawlak et al. show similar features to those in this work. There is an increase and subsequent decrease in $R_s$, which corresponds to the deactivation / reactivation process. Also comparing the 8 keV and 25 keV Ge PAI conditions the $R_s$ peak shifts by ~50 °C for the higher Ge energy; this is also noticeable in this study.

Saavedra et al. [99], carried out similar experiments - except there was no pre-amorphisation, the SOI overlayer thicknesses varied and implant conditions were different. Their results show that B implants into SOI produces significantly lower levels of activation and mobility as well as a higher $R_s$ compared with bulk Si. These results appear to contradict those of this study (apart from the mobility results) until it is remembered that Saavedra et al. did not use PAI. Consequently the defects they produced are spread throughout the SOI top film, and the beneficial effects of the BOX interface in removing Si self interstitials will essentially be lost.

So far only the results for the higher B dose $2 \times 10^{15}$ cm$^{-2}$ have been considered, what differences if any will be seen for a lower B dose $2 \times 10^{14}$ cm$^{-2}$?
Lower B dose

Figure 4-7 shows the $R_S$ versus annealing temperature for PAI, Si and SOI samples implanted with 8 or 20 keV Ge and $2 \times 10^{14}$ cm$^{-2}$ B. Comparing this dose ($2 \times 10^{14}$ cm$^{-2}$) with that discussed previously ($2 \times 10^{15}$ cm$^{-2}$) it is observed not surprisingly that the $R_S$ are higher in the lower dose case. For these lower dose samples a similar electrical deactivation / reactivation phase is observed, with less deactivation in the case of deeper 20 keV Ge PAI.

![Graph showing Rs versus annealing temperature for different substrate types and energies.](image)

Figure 4-7 Van der Pauw resistivity after 60 s isochronal anneals (700 °C – 1000 °C) [2x10$^{14}$ cm$^{-2}$ B]

Two things are noticeable here. First, for the 8 keV PAI the deactivation peaks at a different temperature for bulk Si (775 °C) and SOI (800 °C), this is due to either (a) errors in determining the absolute value of the anneal temperature (difference of 25 °C) or (b) the true peak in $R_S$ for both materials is somewhere between 775 °C and 800 °C.

Secondly, the effects in reduction of deactivation are much more pronounced at this lower dose for both PAI energies. Normalizing the curves at their 700 °C values then calculating the percentage difference between the $R_S$ peaks for both substrate types with respect to the bulk Si samples for both energies and comparing between the two doses results in the table below (Table 4-2).
Table 4-2 Percentage $R_s$ reduction in deactivation peaks between bulk Si and SOI as a function of Ge energy and B dose

<table>
<thead>
<tr>
<th>Ge Energy</th>
<th>B Dose 2x10^14 cm^-2</th>
<th>B Dose 2x10^15 cm^-2</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 keV Ge</td>
<td>24%</td>
<td>17%</td>
</tr>
<tr>
<td>20 keV Ge</td>
<td>60%</td>
<td>36%</td>
</tr>
</tbody>
</table>

Clearly this table shows that the effect the BOX has in SOI on B deactivation is largest for a lower B dose, in fact for the 20 keV PAI the amount of reduction in $R_s$ for a B dose of 2x10^14 cm^-2 is 60%. This may be a consequence of the fact that the B concentrations are now largely below the Si solid solubility limit. In this case, deactivation becomes a purely kinetic excess-interstitial driven phenomenon, rather than a more complex process as the equilibrium solubility of B in Si is approached.

As in the case of the higher B dose, the electrically active dose for the 2x10^14 cm^-2 B dose mirrors the $R_s$ results, shown in Figure 4-8.

![Figure 4-8 Electrically active B dose after 60 s isochronal anneals (700 °C – 1000 °C) [2x10^14 cm^-2 B]](image)

Again as shown earlier there is a small amount of deactivation for the 8 keV PAI but for the 20 keV there is a vast improvement in electrical deactivation.
Finally for the $2 \times 10^{14} \text{ cm}^{-2}$ B dose, the mobility values are compared across the annealing temperature range, this is shown in Figure 4-9. Like the results discussed earlier for the higher B dose wafers, SOI generally has a lower mobility than that observed in bulk Si, this is clearly evident for the lower B dose and the difference is even more pronounced for this lower B dose situation.

![Figure 4-9 Mobility after 60 s isochronal anneals (700 °C – 1000 °C) [2x10^{14} \text{ cm}^{-2} \text{ B}]](image)

The peak in the mobility curves is directly correlated with the increase in carrier density, as mentioned before as the active dose increases, so does the ionised impurity scattering, which is what drives mobility degradation. Here the troughs and peaks between the $N_s$ and mobility are directly related, with the decrease in $N_s$ giving rise to an increase in mobility. As the samples begin to reanimate after 850 °C for 20 keV PAI, the mobility decreases.

To summarise what has been observed so far, it has been shown that there are differences and similarities between the two B doses ($2 \times 10^{14} \text{ cm}^{-2}$) and ($2 \times 10^{15} \text{ cm}^{-2}$). (a) There is a deactivation / reactivation process occurring for both doses, which are shown by an increase and then decrease in $R_s$ and mobility, mirrored by a decrease / increase in $N_s$. (b) The effect of the BOX interface in SOI on dopant activation is much more pronounced in the lower B case, especially at 20 keV Ge PAI.

Now, what happens to the B profile during annealing?
4.3.2 SIMS

To investigate further the B behaviour, its interaction with interstitials from the EOR defects, and the role of the BOX interface, a series of SIMS measurements were carried out on selected samples.

Figure 4-10 shows SIMS profiles for 8 and 20 keV Ge PAI conditions in bulk and SOI after an 800 °C for 60 s anneal. Starting with the 8 keV Ge case (left), there is a small peak in the tail of the B profile at a depth of about 20 nm, corresponding to the former a/c interface position (confirmed by RBS) and thus the location of the EOR defect band. The peak is formed due to the decoration of B on the EOR defects [57], [58], [59] and is virtually the same size for both substrate types, suggesting that there are an equal number of defects present, resulting in the same amount of trapped B. What is also interesting is the uphill diffusion effect [57] seen for both annealed profiles compared with the as-implanted profile – evidenced by a narrower surface peak in the annealed profile.

Figure 4-10 (right) is the 20 keV PAI case a similar peak can be seen but this now occurs at ~40 nm, where the EOR defect band is expected to be (confirmed by RBS). However for this PAI condition the peak is smaller in the SOI case, this suggests that there are a smaller number of defects in the SOI material and therefore less B trapping. Also there is a ‘kink’ in the profile at a concentration of 1x10²⁰ cm⁻³ for SOI and at a lower concentration (~6.5x10¹⁹ cm⁻³) in bulk Si. This ‘kink’ occurs where B has diffused out from the initial implant distribution. This kink concentration reflects the electrically active B concentration, since active B is substitutional and able to diffuse, while clustered B is immobile. So the peak to the left hand side of the ‘kink’ is thought to be composed of
electrically inactive B in the form of BICs. The difference in 'kink' concentration levels in SOI and bulk Si therefore suggests that less deactivation has taken place in the SOI. Looking back at the $R_S$ measurements for this time (see Figure 4-4), one can see that the results show a lower $R_S$ value for SOI, confirming this inference from the SIMS profiles. Another feature common to both SIMS profiles in Figure 4-10 is a peak ~55 nm, this corresponds to B pile-up at the BOX interface [141], [142]. The peak also increases with anneal temperature, due to diffusion of the B to the BOX interface.

For a higher thermal budget, 850 °C for 60s (Figure 4-11), the 8 keV Ge PAI case no longer shows any peak at the EOR location for either substrate type, this suggests that the defects have all dissolved. Interestingly for the 20 keV Ge PAI condition the EOR peak for the bulk sample has decreased in area and the peak in the SOI material is no longer visible.

This would suggest that the EOR defects have mainly dissolved in SOI; while in the bulk material some defects and trapped B are still present. So for the same thermal budget, the defects in the SOI have annealed out while some are still present in the bulk Si. Once again, this confirms the tentative suggestion, already made and based on the $R_S$ data, that the EOR defects dissolve faster in SOI because the interstitials are removed rapidly by the nearby BOX interface sink [97].

For the 20 keV Ge case the 'kink' where B out diffusion is observed occurs at concentration of ~4x10^{19} B cm^{-3} for SOI, and at ~2x10^{19} B cm^{-3} in bulk Si. Again, this difference suggests a higher level of electrical activation in SOI, which correlates with the
lower $R_S$ value seen in the Hall data. A further interesting feature of the SIMS data is that TED which can be seen in the tail region of the profile persists throughout the time that EOR defects are present. In SOI the TED is strongly reduced as can clearly be seen from a comparison of the SIMS profile tail regions in SOI and bulk.

The 8 keV Ge PAI results do not show much difference (Si and SOI) in terms of their electrical characteristics. Also there seems to be a similar number of B atoms trapped at the EOR peak (seen in the SIMS profile) suggesting a similar number of EOR defects in SOI and bulk Si for the same thermal budgets. Therefore the presence of the BOX interface does not appear to have much effect on the EOR defects for the 8 keV PAI.

For the 20 keV Ge PAI condition the results are quite different, they show that the BOX interface is having an effect on the electrical and structural properties of the samples. This is evidenced by a reduction in $R_S$ for SOI samples compared to bulk Si during the deactivation / reactivation phase. These results are mirrored by a higher level of activation for the SOI samples. This suggests that the EOR defects dissolve faster in the SOI samples than in the bulk Si. The SIMS results support this hypothesis since there is a reduction in B trapping (this is an indirect method of estimating the number of defects) for the SOI samples compared to bulk. At higher temperatures (850 °C) the defects appear to have completely dissolved in the SOI case but not in bulk Si - therefore the SIMS results are in agreement with the electrical results.

So do defects dissolve faster in SOI that bulk Si?

4.3.3 TEM

To investigate the defect structure in more detail, bulk Si and SOI samples annealed at 800 and 850°C were examined by XTEM and PTEM. Figure 4-12 and Figure 4-13 show WB XTEM micrographs for 20 keV Ge PAI in bulk Si and SOI annealed at 800 °C and 850 °C for 60 s respectively. Selected area parallel electron energy loss spectroscopy (PEELS) spectra obtained in both cases with the electron beam positioned onto the defect band, are superimposed on the corresponding XTEM micrographs to show the close equivalence of the thickness of the TEM samples.

For this Ge PAI energy (20 keV) the EOR defects lie at ~40 nm below the surface as indicated by the arrow in Figure 4-12. For an anneal temperature of 800 °C, the defects are clearly evident in the bulk Si sample and some are visible in the SOI sample.
(however the number of defects in SOI appear to be smaller). Increasing the anneal temperature to 850 °C, where no B trapping peak was visibly observed in the SIMS for SOI, it can be seen from the TEM (Figure 4-13) that very few defects are present.

Figure 4-12 XTEM micrographs of 20 keV Ge SOI (a) and bulk Si samples (b) annealed at 800 °C for 60 s

These results confirm the conclusion from the SIMS measurements, discussed earlier, that most of the EOR defects in the SOI sample have dissolved during the 850 °C anneal. This is strong evidence in support of the hypothesis that the upper BOX interface becomes the predominant interstitial sink when the EOR band is located close to it in SOI samples.

Figure 4-13 XTEM micrographs of 20 keV Ge SOI (a) and bulk Si samples (b) annealed at 850 °C for 60 s

Similar results are seen in PTEM micrographs for the same samples conditions (Figure 4-14). It is immediately clear that for the samples annealed at 800 °C Figure 4-14a and b, the defect density in the bulk Si (b) appears to be higher than in the SOI (a) sample.
Annealing at 850 °C (Figure 4-14c and d) however shows not only a significant reduction in the visible quantity of defects compared to the 800 °C micrographs, but also for SOI (c) the defect density is lower than for the bulk Si (d) sample. This is clear evidence as suggested in the SIMS and the XTEM micrographs of a faster dissolution of EOR defects in SOI. These micrographs were taken in regions whose thickness largely exceeded that of the EOR defect band (~40 nm).

To conclude from the results in this chapter, the differences between B activation and TED in SOITEC® SOI and bulk Si have been shown, these have been directly correlated with SIMS and XTEM data and show an accelerated dissolution of EOR defects in SOI material. B de-activation, TED, and the density of EOR defects all decrease as the EOR
band is brought closer to the upper BOX interface in the Si overlayer. This result is interpreted as evidence that a substantial portion of the interstitials contained in the EOR defects are absorbed at the upper BOX interface, which appears to act as an efficient sink for interstitials [143].

4.3.4 Theory

A clear and simple explanation of this sinking effect is that there are two interstitial fluxes emerging from the EOR band, one towards the surface and another towards the upper BOX interface. For the 20 keV Ge PAI the EOR defect band is relatively close BOX interface, this accelerates the dissolution of the EOR defects, leading to a reduced fluence of interstitials, integrated over time, in the direction of the Si surface where the dopant is located.

A schematic representation of the competition for interstitials between the Si surface and the upper BOX interface in SOI is shown in Figure 4-15, for the case of the 20 keV Ge implant. For the 8 keV Ge PAI the effect is less marked as the EOR defect band is further from the BOX interface.

In the first case in Figure 4-15, bulk Si (top), there is an interstitial gradient towards the surface from the EOR defect band, during annealing. However, as shown in the lower representation (SOI), the BOX interface also has an interstitial flux towards it, reducing...
the number of interstitials available to reach the surface. The effect of the BOX is strongest when the defect band is placed closer to it, which could explain why there is no noticeable difference in $R_S$ between bulk Si and SOI in the 8 keV Ge case. Also the flux towards the surface for the 8 keV Ge implant is steeper than for the 20 keV Ge case, which is why the defects dissolve faster for the lower energy PAI [144].

All of the results in this chapter – the electrical data, the decrease in the EOR peak and the TED – confirm that the deactivation and diffusion of B are reduced in SOI, and the EOR defects preferentially dissolved, in the case where they are located close to a BOX. This suggests that the upper BOX interface in SOI acts as a sink for Si interstitials.

To further study and to fully take advantage of this effect an optimisation study was carried out, as discussed in the next chapter.
CHAPTER 5 RESULTS III: OPTIMISATION

5.1 INTRODUCTION

In this chapter the implants are tailored to maximise the effects described in the previous Chapter 4, in order to minimise dopant deactivation and diffusion. This was accomplished using the characterisation techniques described previously and also using Monte Carlo (MC) simulation software in order to gain a better understanding of the effect of the buried interface on the EOR defects.

The question that requires being answered in this chapter is how to optimise the improvements seen in SOI and what are the effects involved?

Again using results from the two previous chapters, four more amorphisation energies were chosen in order to optimise the effects of the BOX interface in SOI. This was achieved by placing the EOR defect band as close as possible to the interface while still allowing SPER to take place. As was carried out in Chapter 3, RBS was used to determine, (1) the amorphous depths of this new batch of implants and (2) whether or not they had all re-grown epitaxially. The energies for the PAI were 24, 28, 32 and 36 keV Ge which gave amorphisation depths of ~45, 50, 55 and ~60 nm respectively; this is shown schematically in Figure 5-1.

For this final implant batch (Implant Batch 3), B was implanted after amorphisation into both bulk Si and SOI wafers, this time only one B dose of \(2 \times 10^{15} \text{ cm}^{-2}\) with energy of 500 eV was implanted. Samples from these wafers were then annealed isochronally in order to carry out activation and diffusion studies. Table 5-1 is a summary of the implantation conditions for Implant Batch 3.

This B dose was chosen to continue the study since it gave lower \(R_S\) values (shown in Chapter 4) which are closer to achieving the requirements of the ITRS [3], which is one of the aims of this work.
Figure 5-1 Schematic representation of EOR band in SOI for 24, 28, 32 and 36 keV Ge PAIs

<table>
<thead>
<tr>
<th>Material</th>
<th>Ge energy</th>
<th>Ge dose</th>
<th>B energy</th>
<th>B dose</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bulk Si</td>
<td>24 keV</td>
<td>1x10^{15} cm^{-2}</td>
<td>500 keV</td>
<td>2x10^{15} cm^{-2}</td>
</tr>
<tr>
<td>SOI</td>
<td>24 keV</td>
<td>1x10^{15} cm^{-2}</td>
<td>500 keV</td>
<td>2x10^{15} cm^{-2}</td>
</tr>
<tr>
<td>Bulk Si</td>
<td>28 keV</td>
<td>1x10^{15} cm^{-2}</td>
<td>500 keV</td>
<td>2x10^{15} cm^{-2}</td>
</tr>
<tr>
<td>SOI</td>
<td>28 keV</td>
<td>1x10^{15} cm^{-2}</td>
<td>500 keV</td>
<td>2x10^{15} cm^{-2}</td>
</tr>
<tr>
<td>Bulk Si</td>
<td>32 keV</td>
<td>1x10^{15} cm^{-2}</td>
<td>500 keV</td>
<td>2x10^{15} cm^{-2}</td>
</tr>
<tr>
<td>SOI</td>
<td>32 keV</td>
<td>1x10^{15} cm^{-2}</td>
<td>500 keV</td>
<td>2x10^{15} cm^{-2}</td>
</tr>
<tr>
<td>Bulk Si</td>
<td>36 keV</td>
<td>1x10^{15} cm^{-2}</td>
<td>500 keV</td>
<td>2x10^{15} cm^{-2}</td>
</tr>
<tr>
<td>SOI</td>
<td>36 keV</td>
<td>1x10^{15} cm^{-2}</td>
<td>500 keV</td>
<td>2x10^{15} cm^{-2}</td>
</tr>
</tbody>
</table>

Table 5-1 Implant details for Implant Batch 3
5.2 AMORPHISATION, RE-GROWTH AND EOR DEFECTS

New amorphous layer thicknesses from Implant Batch 3 and the data from Chapter 3 were used to give an updated version of amorphisation depth as a function of implant energy, plotted in red in Figure 5-2. Also plotted are two depths measured by Sharp [145] (blue), these were carried out at Surrey and serve as a further comparison of the data reported here. One difference is that the depths measured by Sharp include the surface oxide thickness of ~1 nm, removing this oxide thickness brings both set of data in line with each other. Subsequent SIMS, XTEM and simulation results confirmed the RBS findings from this work. These results are for bulk Si samples; however those for SOI are within the experimental error for the bulk Si samples.

![Figure 5-2 Amorphous depth Vs Ge implant energy, determined by RBS for all Implant batches](image)

After measuring the amorphous layer depths, a set of samples were then annealed (700 °C for 60 s) in order to find out in which samples SPER would occur in SOI. For Ge implant energies up to and including 32 keV the samples did re-grow epitaxially, however for the 36 keV PAI condition this did not happen. This was to be expected since the amorphisation depth was 60 nm, which engulfs the Si overlayer (55 nm) in SOI and overlaps the BOX, there is no single crystal Si remaining to seed the re-growth.
5.2.1 Re-growth

Random (red) and channelled (blue and black) RBS spectra for the 36 keV PAI in SOI are shown in Figure 5-3. Spectra are shown for as-implanted samples and after annealing at 570 °C for 180 s. Comparing the as-implanted channelled spectrum with its corresponding random spectrum, the amorphous peaks match in both height and width, indicating that the as-implanted sample has an amorphous layer. However when annealed, usually SPER would take place, but for this PAI condition it does not. This is deduced from the fact that the annealed sample still has an amorphous peak of equal magnitude to the as-implanted sample.

What about the 32 keV PAI condition?

RBS and TEM have been carried out on this sample in order to find out whether there is any single crystal Si seed remaining after amorphisation, and if so how thick it is and is there enough to facilitate re-growth of the amorphous layer into single crystal Si.
Analysis was initially carried out using RBS, again as before both as-implanted random, channelled and annealed channelled spectra were obtained and the amorphous peaks compared to the random condition in order to determine the crystallinity of the samples (Figure 5-4).

For the 32 keV PAI two things are clear, the as-implanted channelled spectrum shows an amorphous layer, by comparing with the random spectrum (as described earlier). However the annealed (570 °C for 180 s) spectrum reveals that SPER has occurred and no longer shows an amorphous layer. Examining the annealed spectrum reveals that the Si overlayer is now composed of high quality single crystal Si. Analysis carried out using the Data Furnace, indicates that the amorphous depth for the equivalent bulk Si sample is ~55 nm, however since SPER has taken place in SOI this indicates that there is still enough single crystal Si layer to seed the re-growth, this is because either the original amorphous layer is slightly less than 55 nm or the SOI BOX interface is slightly deeper that anticipated (it is expected to be at a depth of ~55 nm).

![Figure 5-4 RBS spectra for 32 keV PAI in SOI, red, blue and black spectrum represent the as-implanted normal incidence random, channelled and annealed conditions respectively. The inset shows the amorphous peak area only](image)
To investigate the amorphous layer thickness further and to check the crystal quality of the re-grown layer for the 32 keV PAI in SOI, XTEM was carried out on both as-implanted and annealed samples.

Figure 5-5 shows an XTEM micrograph for the as-implanted condition, measurements show that the top amorphous layer is \( \approx 58 \) nm thick; this value is \( \approx 3 \) nm thicker than expected, however it is within the TEM measurement error margins (±3 nm).

![XTEM micrograph of a 32 keV Ge PAI B as-implanted SOI sample](image)

From Figure 5-5 it is clear that between the amorphous and BOX layers there is a thin single crystal Si seed layer. In order to determine the thickness of this layer more accurately HREM was carried out at two different locations on the same sample (Figure 5-6). What appear to be darker patches are single crystal Si islands that lie between the a-Si and the amorphous SiO₂ layers. These islands are what remain as the seed for SPER; their thickness varies across the width of the sample and ranges from 0 – 4 nm.
Figure 5-6 HREM micrographs of the bottom of the Si overlayer in the case of the as-implanted 32 keV PAI in SOI (a) and (b) are different locations from the same sample.

Figure 5-7 HREM micrographs of the bottom of the Si overlayer in the case of the 32 keV PAI in SOI annealed at 500 °C for 15 s, (a) and (b) are different locations from the same sample.
During annealing these islands seed laterally as well as vertically to re-grow the a-Si layer. To show this, another 32 keV PAI sample in SOI was annealed at 500 °C for 15 s, with the purpose of re-growing a small portion of the Si overlayer; the anneal conditions were simulated using the same re-growth program as described in section 2.10.1. Figure 5-7 shows the resulting HREM micrograph for this sample, again taken at two locations on the same sample. It is clear that the c-Si islands in the as-implanted sample condition have now re-grown into a thicker more uniform layer - this is clear evidence of lateral as well as vertical re-growth. Also there are no observable twins, stacking faults, threading dislocations or extended defects which tend to suggest that the layer is single crystal Si. Evidently the attachment of the crystal islands to the SOI BOX keeps them close enough to their locations on the original single crystal lattice (prior to PAI) that they can re-grow together without forming defects or polycrystalline structures.

It has been ascertained from the HREM that the surviving single crystal Si seed layer is <4 nm thick (average ~2 nm), suggesting that the BOX is at a depth of ~60 nm. This is 5 nm deeper than expected for these SOI samples but SIMS, TEM and RBS have already shown that the Si overlayer thickness in these SOI samples varies between 55 - 60 nm.

What does this mean in terms of the position of the EOR defect band?

5.2.2 EOR Defects

XTEM was carried out on annealed (700 °C for 60 s) samples, in order to see if full re-crystalisation had occurred and to find the position of the EOR band. Figure 5-8 are XTEM micrographs for annealed implants in SOI and bulk Si. Looking at (a) the SOI sample, initial observations are that the amorphous layer is no longer visible and the re-grown region consists of single-crystal Si (confirming RBS results).

In micrograph (b) bulk Si, a band of EOR defects is visible at a depth of ~60 nm below the sample surface, but in SOI (a) no significant defect accumulation is found. High-resolution imaging (Figure 5-9) detects only a small number of isolated {113} defects close to the BOX interface. A plausible explanation for this effect is that part of the reservoir of excess interstitials that nucleate into EOR defects in the bulk case, is absent in the SOI case.
Figure 5-8 XTEM micrographs of 32 keV Ge PAI B implanted samples annealed at 700 °C for 60 s in (a) SOI and (b) bulk Si.

Figure 5-9 HREM micrograph of a defect lying close to a {113} plane observed near the bottom of the Si overlayer in a 32 keV PAI SOI sample annealed at 700 °C for 60 s.
The excess atom density generated by the Ge implant in the SOI remains trapped in the BOX. As the diffusivity of Si in SiO₂ is negligible at the temperatures used in this study [92], only the excess interstitials created in the thin crystalline region between the a/c interface and the BOX interface are available to nucleate into EOR defects, and of these an unknown proportion may be consumed in interface reactions [146].

The {113} defect seen in Figure 5-9 is shallower (further away from the BOX interface) than expected, this is possibly due to the non-uniform nature of the initial as-implanted amorphous / crystalline interface. At this particular location, perhaps the crystal seed was slightly thicker than the average across the width of the sample. Knowing this combined with the fact that EOR defects form just below the a/c interface could explain the position of this particular {113} defect.

What happens electrically for these now optimised implants?

5.3 ISOCHRONAL ANNEAL STUDY

5.3.1 Electrical Measurements

Samples from all wafers were isochronally annealed from 700 °C – 1000 °C for 60 s in steps of 50 °C, this allowed a study of the electrical response of the B dopants.

Is there still any electrical deactivation?

Sheet resistance

Firstly the bulk Si only case is considered (Figure 5-10), the graph shows $R_s$ versus annealing temperature for samples implanted with 8 – 36 keV Ge and $2 \times 10^{15}$ cm⁻² 500 eV B in bulk Si. Three features are immediately apparent; firstly (1) as explained in Chapter 4 the well known reverse annealing effect [5] is observed for all PAI conditions. This is evidenced by an increase in $R_s$ with anneal temperature until it peaks and then followed by a subsequent decrease in $R_s$.

(2) The results indicate that the peak deactivation varies with PAI condition, for 8 keV it is at ~800 °C. For the remaining PAI conditions the peak varies between ~800 – 850 °C and is very likely that the true peak lies somewhere between these two temperatures. As described in Chapter 4, determining the exact location of the deactivation peak is also due to errors in determining the absolute value of the anneal temperature.
The final feature observed in Figure 5-10 is, (3) as the PAI energy is increased (i.e. EOR distance from the Si surface is increased) then the change in deactivation $\Delta R_S$ (700 °C – peak) decreases. This is due to the increased deactivation efficiency when the EOR defects are closer to the Si surface [68].

![Graph showing Van der Pauw resistivity after 60 s isochronal anneals (700 °C – 1000 °C) for 8 – 36 keV Ge PAI in bulk Si only [2x10$^{15}$ cm$^{-2}$ B].]

Now, to investigate the effects in SOI; Chapter 4 explained that SOI showed an improvement in terms of B deactivation due to the BOX interface acting as a sink for some of the interstitials released from the EOR band, that would normally help to deactivate the B. It also concluded that this effect was larger the closer the EOR was to the BOX interface. In this set of implants (batch 3), the EOR is placed even closer to the buried interface and for the 32 keV PAI a sizeable portion of the excess interstitials that would normally contribute to EOR formation are locked inside the BOX.

Figure 5-11 shows the $R_S$ results for samples implanted with 8 – 32 keV Ge and 2x10$^{15}$ cm$^{-2}$ 500 eV B in SOI. The 36 keV PAI condition has been omitted in SOI since SPER did not take place, therefore the Si overlayer does not re-crystallise and dopant activation does not take place.

Again the typical deactivation / reactivation phase occurs, however for the new implants (24 – 32 keV) the $\Delta R_S$ are much smaller than for the 8 and 20 keV PAI implants. This is
attributed to the proximity of the EOR defect band to the BOX interface and also possibly to another effect, the cutting of the initial excess interstitial distribution with the BOX.

![Graph showing Van der Pauw resistivity after 60 s isochronal anneals (700 °C – 1000 °C) for 8 – 32 keV Ge PAI in SOI only [2x10^15 cm^-2 B]](image)

Figure 5-11 Van der Pauw resistivity after 60 s isochronal anneals (700 °C – 1000 °C) for 8 – 32 keV Ge PAI in SOI only [2x10^15 cm^-2 B]

The results in Figure 5-11 show that least deactivation is observed for the 32 keV Ge PAI in SOI where an increase of only ~80 Ω/□ in observed in Rs between 700 °C to 850 °C this is compared to ~480 Ω/□ for the same implant in bulk Si, that represents an 6x improvement in ΔRs for SOI.

To put these improvements of ΔRs into context, using the 8 keV as a reference (since very little difference was seen between the bulk and SOI scenarios), calculating the ΔRs (700 °C to the peak) for each energy and then expressing the difference from the 8 keV as a percentage \([\frac{\Delta R_s^{8\text{keV}} - \Delta R_s^{x\text{keV}}}{\Delta R_s^{8\text{keV}}} \times 100]\) gives the data in Table 5-2.

<table>
<thead>
<tr>
<th>Energy</th>
<th>Improvement (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 → 20keV Ge</td>
<td>46%</td>
</tr>
<tr>
<td>8 → 24keV Ge</td>
<td>84%</td>
</tr>
<tr>
<td>8 → 28keV Ge</td>
<td>91%</td>
</tr>
<tr>
<td>8 → 32keV Ge</td>
<td>92%</td>
</tr>
</tbody>
</table>

Table 5-2 Improvement in ΔRs for each PAI energy with respect to the value for 8 keV
This table clearly shows how tailoring the PAI energy can yield a significant improvement in $R_s$ deactivation, 92% is seen for the highest PAI energy, with 100% representing no deactivation at all.

Comparing bulk Si and SOI similar trends are seen (1) there is a deactivation / reactivation process, which is shown by an increase and then decrease in $R_s$, (2) SOI material starts with a slightly higher $R_s$ value than for bulk, but ends with similar values to bulk Si, (3) peak deactivation occurs at higher temperatures for larger PAI energies, for 8 keV it is at $\sim800 \, ^\circ C$, however for the remaining PAI conditions the peak varies between $\sim800 - 850 \, ^\circ C$ (4) as the PAI energy increases the $\Delta R_s$ decreases, this difference is much more pronounced with the SOI samples than bulk Si.

To explain these observations (1) is the well known 'reverse annealing' effect [5], (2) the difference in $R_s$ at 700 °C could be attributed to a difference in the two materials. This fits with previously published observations of a lower level of B activation in SOI [140].

(3) The shift in the temperature for peak deactivation, between the different PAIs, is well known and is caused by a reduction in the concentration gradient of interstitials towards the B-doped region when the EOR band is located deeper into the material [5], [68]. However for the 20 – 36 keV PAI implants this peak seems to vary between 800 °C and 850 °C and is very likely that the true peak lies somewhere between these two temperatures. The true peak position is further investigated at the end of this section.

(4) As has been shown in Chapter 4, the difference between the SOI and bulk Si means there is more electrically active B in SOI, this is due to (i) the BOX interface acting as a sink for interstitials, removing some of the self interstitials that would otherwise have contributed to BIC formation closer to the surface [143]. There is also another effect that is possibly contributing to the removal of interstitials; (ii) the "cutting" of the initial excess interstitial distribution by the BOX, further investigation into these two effects will be discussed later in this chapter.

In order to find the true $R_s$ peak position for all the PAI energies, bulk Si samples were annealed as before, but this time in steps of 25 °C ranging from 700 – 850 °C, 4pp measurements were made to monitor the variations in $R_s$. These results are summarised in a graph in Figure 5-12.
The results clearly show that for the 8 keV Ge PAI the peak deactivation is ~775 °C, however the difference in $R_S$ between this temperature and that at 800 °C is ~36 Ω/□ and well within the error bars of the measurement. Perhaps the real peak is again somewhere between these two temperatures, however determining this could be argued to be in the error boundaries of determining the absolute value of the anneal temperatures used.

Now for the remaining PAIs, in Chapter 4 it was determined that the peak for the 20 keV PAI was ~850 °C, it can be seen from the data in Figure 5-12 that the peak actually lies at ~825 °C. The same trend is observed for Ge energies 24 – 36 keV, the true peak is closer to ~825 °C than either 800 °C or 850 °C, this is why discrepancies were observed earlier in Figure 5-10 for determining the $R_S$ peak. It is worth noting that the separation in peaks between 8 keV Ge PAI and the remaining higher energies is still ~50 °C.

*Are the observed improvements in $R_S$ reduction also reflected in sheet carrier measurements?*
**Activation**

Figure 5-13 is a graph showing the electrically active B dose $N_s$ versus annealing temperature for all PAI conditions and for both materials. These results correlate with and mirror the $R_s$ measurements, which is as expected.

![Graph showing electrically active B dose versus annealing temperature](image)

**Figure 5-13 Electrically active B dose after 60 s isochronal anneals (700 °C – 1000 °C) in (a) bulk Si and (b) SOI materials [2x10^{15} \text{ cm}^{-2} \text{ B}]**
There are many similar features between Figure 5-13a and Figure 5-13b. (1) It is clear that from this data that the "reverse annealing" effect is taking place, with a trough at 800 °C for 8 keV Ge and 850 °C for the remaining Ge energies. This deactivation (decrease in $N_S$) / reactivation (increase in $N_S$) process is due to defect evolution and dissolution as mentioned earlier when discussing the $R_S$ results.

(2) As the PAI energy goes up the $\Delta N_S$ (700 °C to trough) goes down, for SOI this effect is much more pronounced. A table summarising the $\Delta R_S$ and $\Delta N_S$ expressed as a percentage with respect to their starting 700 °C values is shown in Table 5-3.

<table>
<thead>
<tr>
<th>Bulk Si</th>
<th>$\Delta R_S$ w.r.t. 700°C</th>
<th>$\Delta N_S$ w.r.t. 700°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 keV Ge</td>
<td>133%</td>
<td>72%</td>
</tr>
<tr>
<td>20 keV Ge</td>
<td>108%</td>
<td>65%</td>
</tr>
<tr>
<td>24 keV Ge</td>
<td>101%</td>
<td>64%</td>
</tr>
<tr>
<td>28 keV Ge</td>
<td>93%</td>
<td>64%</td>
</tr>
<tr>
<td>32 keV Ge</td>
<td>66%</td>
<td>61%</td>
</tr>
<tr>
<td>36 keV Ge</td>
<td>64%</td>
<td>57%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>SOI</th>
<th>$\Delta R_S$ w.r.t. 700°C</th>
<th>$\Delta N_S$ w.r.t. 700°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 keV Ge</td>
<td>100%</td>
<td>59%</td>
</tr>
<tr>
<td>20 keV Ge</td>
<td>61%</td>
<td>43%</td>
</tr>
<tr>
<td>24 keV Ge</td>
<td>19%</td>
<td>28%</td>
</tr>
<tr>
<td>28 keV Ge</td>
<td>11%</td>
<td>25%</td>
</tr>
<tr>
<td>32 keV Ge</td>
<td>10%</td>
<td>22%</td>
</tr>
</tbody>
</table>

Table 5-3 Deactivation, $\Delta R_S$ and $\Delta N_S$ for each PAI energy with respect to their 700 °C value.

Comparing initially the $\Delta R_S$ values for 32 keV in bulk Si, there is a ~2x improvement compared to the 8 keV values, whereas for the same PAIs in SOI the improvement is ~10 times. Now observing the differences in $\Delta N_S$, for bulk Si improvement between PAIs is small slightly over 1, however for SOI between 8 keV and 32 keV there is ~2.5x improvement in deactivation. Comparing between bulk Si and SOI, for a PAI of 32 keV the improvement in $\Delta R_S$ is ~6x, whereas for $\Delta N_S$ the factor is ~2.5x.

These results show that after optimisation of the PAI the junction is much more stable in terms of its electrical properties for SOI. It is likely in SOI that most of the interstitials released from the EOR band are absorbed by the upper BOX interface, as explained in Chapter 4 and shown in published work by Hamilton et al. [143].
**Mobility**

It is not only important to understand the effects on $R_S$ and $N_S$ but also what happens to the mobility during annealing (see Figure 5-14).

![Graph showing mobility after 60 s isochronal anneals (700 °C – 1000 °C) in (a) bulk Si and (b) SOI materials [2x10^{15} cm^2 B].](image-url)
As noted in Chapter 4, as the PAI energy increases so do the starting mobility values (700 °C to the temperature positions of the Ns troughs), this is observed both for the (a) bulk Si and (b) SOI. This can be directly correlated with a lower Rs for the higher PAIs, due to the fact that there are fewer interstitials travelling towards the surface as the PAI energy is increased. In addition, higher mobility can be correlated to a decrease in the density of scattering centres. This can occur with diffusing B profiles, as well as, wider Ge distributions for higher PAIs, since Ge ions could also be possible scattering centres.

After further annealing from the troughs in the Ns up to 1000 °C, dopant atoms start to reactivate which causes Rs to continue to reduce due to there being more active dopants. However, more scattering centres are created due to the increase in substitutional B atoms, which is why the mobility appears to saturate at higher temperatures.

In Figure 5-14 (b) for the 36 keV PAI the mobility is very low; ~50% less than the other PAIs throughout the entire annealing temperature range. As discussed earlier for this PAI SPER did not take place, therefore the observed reduction in mobility is due to the Si overlayer being in a polycrystalline state. This confirms that the 36 keV PAI in 55 nm thick SOI is not a candidate for this study.

To summarise, as the electrical measurements have shown that between bulk Si and SOI ARs and ANS are reduced in SOI and this effect increases with increasing the PAI energy. It is suggested that these observations are due to two effects (i) the BOX interface acting as an interstitial sink [143] and (ii) the BOX acting as a cutting mechanism, reducing the initial quantity of interstitials within the Si overlayer [146]. In order to confirm these hypotheses further studies were carried out.

5.3.2 SIMS

The previous chapter showed how SOI appeared to have superior properties in terms of reduced TED and higher dopant activation.

In order to be fully confident with the repeatability of the annealing temperature, a further study was carried out before annealing the new (batch 3) set of implants for SIMS. Two samples from batch 2 implants were annealed again and then compared with previous measurements made by SIMS. The first (old set) of SIMS used in Chapter 4 were measured in 2004 and the second (new set) were measured in 2006. The anneal
temperature chosen was 850 °C for 60 s, since for the majority of the samples this seems to be a key temperature with respect to the deactivation peaks. The results are shown in Figure 5-15.

![Figure 5-15 SIMS profiles of annealed old (2004) Vs new (2006) 8 keV Ge PAI in (a) bulk Si and (b) SOI [2x10^{15} cm^{-2} B]](image)

In both cases comparing between new and old annealed samples at 850 °C (green and red curves respectively), there are only small variations in the profiles and these are attributed to (1) small temperature difference during annealing and to a lesser extent (2) SIMS error. However for the SOI (Figure 5-15b) one factor which does stand out is the difference in the position of the peaks, caused by B segregation at the BOX interface. For the old sample it is ~54 nm and for the new sample it is ~57 nm, this is largely explained by (1) variations in the Si overlayer thickness in the SOI material (also observed in XTEM shown earlier in this chapter) and again (2) SIMS error.

The old profiles annealed at 800 and 900 °C (black and blue curves respectively) have also been included to help to visualise how small the variations are between the old and new SIMS samples annealed at 850 °C.

Now that it has been ascertained that the annealing and SIMS errors involved are very small, a valid comparison can be made between the samples from batch 3 and those from batch 2. Selected samples were annealed and analysed in order to compare between PAIs and between bulk Si and SOI, in order to understand the improvements seen in the electrical measurements for the 32 keV PAI in SOI.
The first comparison is made between the PAI energies. The results show similar features to those seen in the previous SIMS profiles. Three main effects are highlighted by green circles in Figure 5-16.

![SIMS profiles for SOI as-implanted and annealed 850 °C for 60 s, for 8, 20 and 32 keV Ge PAI conditions [2x10^15 cm^-2 B]](image)

Figure 5-16 SIMS profiles for SOI as-implanted and annealed 850 °C for 60 s, for 8, 20 and 32 keV Ge PAI conditions [2x10^15 cm^-2 B]

It is evident from (1) that the 'kink' concentration where the B diffuses out from the initial implant distribution is higher for the 32keV PAI indicating a higher level of B activation. Looking back at the electrical data for this temperature (see Figure 5-11 and Figure 5-13b); one can see that the results show an increasing level of activation and a corresponding reduction in $R_s$, as PAI energy is increased, confirming what is seen in the SIMS profiles. The kink level in the SOI ($\sim$8x10^{19} B cm^{-3}) is above the equilibrium solubility limit for B in c-Si at this temperature ($\sim$5x10^{19} B cm^{-3} [10]). Junction abruptness and TED in the tail (2) are again reduced as the PAI energy increases. Decoration of the EOR defects (3) is not observed in this case and is concluded that few EOR defects remain at this temperature. The peaks in (4) represent B segregation at the BOX interface, unfortunately due to variations in the SOI overlayer thickness (and maybe SIMS error) the observed peaks do not overlap as they should. Instead they sit within the range $\sim$55 – 59 nm.
The SIMS in Figure 5-17 was carried out to investigate three effects: (1) differences between the 32 keV Ge PAI in SOI compared to bulk Si. (2) To investigate the possibility of an overlapping of the initial excess interstitial profile with the BOX. (3) To confirm the theory that the combination of the overlapping effect and that of the BOX acting as a sink, causes the EOR formation in the 32 keV Ge PAI in SOI to be hindered (as explained in the TEM section of this chapter, section 5.2.2).

![Figure 5-17 SIMS profiles of 32 keV Ge PAI conditions annealed at (a) 800 °C and (b) 850 °C for 60 s [2x10^{15} \text{cm}^{-2} \text{B}]]

Both temperatures shown in Figure 5-17 show similar results, but there are also some distinct differences, (1) comparing between bulk Si and SOI, it is clear that the ‘kink’ concentration is higher for SOI indicating a higher level of activation. This is confirmed by the electrical data (see Figure 5-13). At 800 °C the difference in ‘kink’ level is not as large as that at 850 °C where the difference is quite significant. At 850°C the B ‘kink’ concentration is \(\sim 7.5 \times 10^{19} \text{cm}^3\) for SOI and \(\sim 1.5 \times 10^{19} \text{cm}^3\) for bulk Si, this represents an increase of 5x for SOI. Also (2) the junction in SOI is much more abrupt and there is far less TED, as shown by the longer tail in the SIMS profile for bulk Si. For a B concentration of \(1 \times 10^{18} \text{cm}^3\) the \(X_j\) for SOI is \(\sim 27.5 \text{nm}\) and for bulk Si \(\sim 42.5 \text{nm}\) at 850 °C, this represents a reduction of 1.5x in SOI. Next (3) is the peak in the bulk Si at \(\sim 60 \text{nm}\) observed at both 800 °C and 850 °C, this is thought to represent B decoration of the EOR defect band. This is supported by evidence of a defect band at a similar depth in the XTEM micrographs in Figure 5-8. Also as the anneal temperature increases beyond 850 °C the peak is no longer observed, this is attributed to the dissolution of the defect band at higher temperatures and is also observed in the SIMS in Chapter 3. Finally (4) the peak in the SOI, observed for both temperatures (and is also seen at higher temperatures) represents B segregation at the BOX interface \(\sim 55 \text{nm}\).
What is interesting about this peak at the SOI interface is that it is shallower than the EOR peak in bulk Si; this would infer that the a/c interface in SOI after pre-amorphisation is situated within the BOX and would also at first sight suggest that SPER could not take place. However it is known experimentally (RBS and TEM seen earlier in this chapter) that the SPER does take place. Taking this into account the SIMS profiles in Figure 5-17 help to support the hypothesis that a significant proportion of the excess interstitials are trapped within the BOX. To investigate this further quantitative analysis was carried out using MC simulations.

5.3.3 Simulations

At this point, the question arises as to whether, contrary to previously published arguments concerning interface recombination [101], all of these results might be explained in terms of the locking of the excess interstitial distribution within the BOX. To test this hypothesis, an estimate of the dose of excess interstitials implanted in the residual crystalline portion of the Si overlayer as a function of PAI energy was made, using MC implant simulation techniques.

Care was taken in simulating the Ge implant distribution correctly, and is the reason why two implant simulators were used; (1) Cascade and (2) KING, both of which are described in more detail in section 2.10. The main difference between them is that (1) assumes an amorphous substrate whereas (2) uses crystalline material. Since Ge implantation was made into crystalline Si, it was expected that (2) should reveal more accurate results; however (1) was also used for comparison and to understand the differences between the two.

However before carrying out any simulations, initial assumptions must be made, these are listed here:

1. **Surviving crystal seed thickness for 32 keV Ge in SOI [2 nm]:** For this PAI, HREM has shown (Figure 5-6) that the thickness of the residual crystalline layer after Ge amorphisation varies from 0 - 4 nm and suggests that it may not be perfectly continuous; averaging this depth range gives a thickness of ~2 nm.

2. **BOX interface depth [57 nm]:** RBS values gives an a/c interface depth of 55 nm for the 32 keV Ge PAI and then adding the 2 nm residual crystalline
thickness (obtained from HREM) after amorphisation gives a BOX interface depth of ~57 nm, this is assumed for all SOI simulations.

Of course the absolute depth values in these thin layers have significant uncertainties and these are taken into consideration when carrying out the simulations.

Now that the assumptions had been defined, it was possible to proceed with the simulation. MC simulated implanted Ge distributions were compared with measured SIMS data, those shown in Figure 5-18.

![Figure 5-18 MC simulations Vs SIMS data for 8 keV Ge implants into bulk Si and SOI](image)

Examine the SIMS data first, bulk Si (black) and SOI (red) both distributions sit on top of each other, apart from in SOI where the Ge distribution reaches the BOX interface, observed by a peak in the profile. The observed peak is a combination of two factors (1) Ge pileup at the interface and (2) an artefact of the SIMS, due to a change in substrate (Si to SiO$_2$) material. Comparing between the KING simulations for bulk Si (blue) and SOI (green), again these distributions sit on top of each other. For SOI there is also a peak at the BOX interface (~57 nm) and is due to a change in material from c-Si to amorphous SiO$_2$. No channelling will occur in the SiO$_2$ as it is amorphous.

Comparing between the SIMS for SOI (red) and the KING simulations for SOI (green), it is clear that there is excellent agreement between the peaks in profile up to the
channelling tail. The same is also true for the two bulk Si samples. However comparing the Cascade simulation in SOI (pink) with the SIMS SOI (red) there is a major difference; there is no tail in the profile for the Cascade simulation. This is because the Cascade simulation package assumes an amorphous target and hence one would not expect to see a channelling tail as implants do not channel in amorphous material.

The excellent agreement between the simulated KING distributions and the actual experimental SIMS results provide a degree of confidence that this is the correct simulation package to use in this case. Thus all the following simulations were carried out using the KING simulator code (which assumes a crystalline material).

An added benefit of using the KING simulations is that one of its output files gives the amorphous fraction of the Si layer after implantation. This is useful as it provides a further comparison between the simulations and the measured amorphous depths obtained using RBS. These results are summarised in Figure 5-19.

![Figure 5-19 Amorphous depth Vs Ge PAI energy for RBS and KING simulations, where the red dashed line represents the depth of the BOX interface](image)

Again comparing the simulated and experimental data gives an excellent agreement. It is also important since the a/c interface depths used in the following simulations are calculations and can be used with a high degree of confidence as the experimental and simulated results match.
The next step is to calculate the as-implanted defect distribution. The standard way for calculating this is by subtracting the interstitial distribution from the vacancy distribution. This is because local recombination of interstitials and vacancies occurs upon annealing, leaving a net excess of interstitials near the projected range of the implant and an excess of vacancies in the near surface region. This has already been explained in more detail in section 1.3.2. Since SOI consists of two elements, the top overlayer of Si and the BOX layer (SiO\textsubscript{2}). Thus Si and O recoil as Ge ions are implanted. The true defect distribution can therefore be calculated taking all four resulting distributions into account and can be expressed by the following equation:

\[
D_D = S_i - [S_{iv} - (O_i - O_v)]
\]

Equation 5-1 Defect Distribution (cm\textsuperscript{3})

Where;

'D\textsubscript{D}' is the defect distribution (cm\textsuperscript{3}),
'S\textsubscript{i}' is the Silicon interstitial distribution (cm\textsuperscript{3}),
'S\textsubscript{iv}' is the Silicon vacancy distribution (cm\textsuperscript{3}),
'O\textsubscript{i}' is the Oxygen interstitial distribution (cm\textsuperscript{3}),
'O\textsubscript{v}' is the Oxygen vacancy distribution (cm\textsuperscript{3})

Figure 5-20 illustrates the theoretical defect distributions for the different PAI energies as a function of depth, using the formula in Equation 5-1. The red dashed line represents the position of the BOX interface (57 nm).

Where the profiles are above the origin of the plot, in Figure 5-20, represents a net excess of interstitials whereas when they are below the origin, this represents a net excess of vacancies. As the PAI energy is increased the depth and width of the distribution is increased. The small peak observed at 57 nm (circled in pink) is a consequence of recoiled atoms at the BOX interface, the peak increases with PAI energy since the implant is going in deeper.

The important part of these defect distributions, with respect to calculating the dose of interstitials responsible for EOR formation and consequently BIC formation and TED, is between the a/c interface and the BOX interface (location of the surviving c-Si seed layer after amorphisation). This is why it was very important to be able to simulate the tail of the Ge distribution correctly, in order to have the most accurate tail for the defect distribution.
The excess interstitial (defect) distributions for the as-implanted SOI samples were integrated between the amorphous / crystalline interface and the BOX interface to give the dose of excess interstitials remaining within the overlayer after amorphisation. The same calculation for bulk Si, where the BOX is absent, gave a correspondingly larger dose of excess interstitials. This is because for SOI a portion of the interstitials are implanted into the BOX and increases with PAI energy. Comparison of this calculated dose with experimental measurements of the number of interstitials in the EOR band in bulk Si [29] then allowed normalization of the calculations for SOI to give the number of excess interstitials, ‘Nc’ in the EOR band for each Ge implant energy in SOI.

To support the hypothesis that the BOX interface is an effective sink for interstitials, Nc must be multiplied by a factor that allows for a recombination length of a Si interstitial with the BOX interface to be best matched with B deactivation. In order to quantify this, the following simplified model was used.

The EOR band is treated as a simple ‘plane’ at depth ‘x’, placed at the centroid of the excess interstitial depth distribution in the region beyond the a/c interface. This approximation enables a simple calculation of the interstitial fluxes towards the top and
bottom interfaces of the Si overlayer during annealing, shown in Equation 5-2. A representation of these fluxes and distances are shown in Figure 5-21.

\[
\varphi_1 = \frac{D_i \times C_{\text{LEOR}}}{x + L_1}, \quad \varphi_2 = \frac{D_i \times C_{\text{LEOR}}}{d - x + L_2}
\]

Equation 5-2 Interstitial Fluxes \( (\text{cm}^2 \text{s}^{-1}) \)

Where;
‘\( D_i \)’ is the interstitial diffusivity at a given temperature \( (\text{cm}^2 \text{s}^{-1}) \)
‘\( C_{\text{LEOR}} \)’ is the interstitial concentration at the EOR depth \( (\text{cm}^3) \),
‘\( d \)’ is the thickness of the Si overlayer \( (\text{nm}) \),
‘\( L_1, L_2 \)’ are the recombination lengths for interstitials at its upper and lower interfaces, respectively \( (\text{nm}) \)

Figure 5-21 Schematic representation of the fluxes and distances involved in the model used in the simulations

As is well known \[34\], the recombination length at the surface, \( L_1 \), is less than a few nm during TED and can certainly be neglected in comparison to the thickness \( d \). There is now as a good approximation for the fraction of interstitials ‘\( F_1 \)’ flowing to the surface, given by Equation 5-3.

\[
F_1 = \frac{d - x + L_2}{d + L_2}
\]

Equation 5-3 Interstitial Fraction \( (\%\) )

This quantity, multiplied by the dose, \( N_c \), is then plotted as a family of curves in Figure 5-22, for cases, \( L_2 = (0, 10, 30, 100, \infty)\) nm. When \( L_2 \) tends to \( \infty \), \( F_1 \) tends to 1, and the
BOX interface can be modelled as a reflecting boundary for interstitials, whereas when \( L_2 = 0 \) the BOX interface becomes a perfect sink.

These curves are plotted as a function of the remaining crystal layer thickness after amorphisation. This was done to emphasise the fact that the true variable for increasing the sinking efficiency of the BOX interface is not the Ge PAI energy or amorphous layer thickness, but the distance of the resulting EOR band from the BOX. This is represented as the distance from the a/c interface to the BOX or the thickness of the surviving single crystal seed after amorphisation.

Figure 5-22 also shows the amount of B deactivation caused by the migration of interstitials from the EOR band. Expressed as the difference, \( \delta N_B(E) \), between the number of carriers at 700 °C and that at the maximum measured deactivation (corresponding to the peaks in \( R_s \) in Figure 5-11) for each PAI energy.

Further assumptions made are as follows:

3. **Amorphous thickness:** As discussed for Figure 5-19, the a/c interface depths used in the following simulations are those resulting from the simulated values, which as stated previously agree with that measured by RBS. The exception being the 32 keV PAI, where the amorphous layer depth used in the simulations is assumed to be at 55 nm (obtained from RBS absolute value and agrees with XTEM within error margins)

4. No significant BIC dissolution occurs simultaneously to the EOR dissolution

5. During the deactivation phase a high percentage (100%) of the interstitials in the EOR defects are released.

The deactivation data are presented in the form \( \delta N_B(E) - \delta N_B(32 \text{ keV}) \). This serves to eliminate the effects of the small amount of ‘equilibrium’ B deactivation that occurs in the 32 keV case. This is because B is more soluble in the amorphous phase than it is in the crystalline and thus after SPER a smaller proportion of B is soluble in the c-Si resulting in a slight deactivation. This effect is unrelated to the presence of excess interstitials, occurring even in Si that has been treated with an excess of vacancies [147].

Figure 5-22 shows that, as the thickness of the remaining crystalline layer is reduced, B deactivation decreases much more rapidly than the number of available interstitials. This
is explained by the fact that, as the EOR band approaches the interface with the BOX, an increasing proportion of interstitials are absorbed there instead of migrating to the near surface region, where they can deactivate the B.

![Diagram showing dose of excess Si interstitials and deactivated B dose as a function of remaining crystal layer thickness.](image)

Figure 5-22 Dose of excess Si interstitials that flow toward the surface driving B deactivation for various values of recombination length \(L_2 = 0, 10, 30, 100, \infty\) (left Y-axis), plotted together with relative deactivated B dose (right Y-axis). Results are expressed as a function of the remaining crystal layer thickness after amorphisation.

By treating the number of B atoms deactivated by one Si interstitial, 'n', as a free parameter in a fit of \(F_1N_e\) to the deactivation data, it is found that the best fit is for the case \(L_2 = 0\). There is a significant increase in the \(\chi^2\) value for the \(L_2 > 10\). Moreover, the fitted value of n is \(~2\) for the case \(L_2 = 0\), but becomes unrealistically small (n < 1) for larger \(L_2\) values. These chi-squared values are summarised in Table 5-4.

<table>
<thead>
<tr>
<th>(L_2 =)</th>
<th>0</th>
<th>10</th>
<th>30</th>
<th>100</th>
<th>(\infty)</th>
</tr>
</thead>
<tbody>
<tr>
<td>n</td>
<td>1.7</td>
<td>0.7</td>
<td>0.4</td>
<td>0.24</td>
<td>0.16</td>
</tr>
<tr>
<td>8</td>
<td>2</td>
<td>74</td>
<td>133</td>
<td>172</td>
<td>194</td>
</tr>
<tr>
<td>20</td>
<td>31</td>
<td>102</td>
<td>130</td>
<td>148</td>
<td>158</td>
</tr>
<tr>
<td>24</td>
<td>2</td>
<td>8</td>
<td>16</td>
<td>23</td>
<td>27</td>
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<tr>
<td>28</td>
<td>1</td>
<td>26</td>
<td>43</td>
<td>49</td>
<td>51</td>
</tr>
<tr>
<td>32</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Table 5-4 Chi-squared \(\chi^2\) values for parameter 'n' in a fit of \(F_1N_e\)
Vertical scales differing by a factor of two were chosen in Figure 5-22, to compare the number of interstitials reaching the surface with the measured deactivation (pink curve), based on the assumption:

6. **B deactivation \( B_{\text{B}} \):** Two B atoms are assumed to be deactivated by one interstitial [5], [68].

This curve follows the \( L_2 = 0 \) curve for all data points except the first (remaining crystal thickness 37 nm) for which the EOR band slightly overlapped the B implant distribution. The slightly low value for this point could be a result of direct deactivation by implanted interstitials prior to annealing. The shape of the actual deactivation curve is clearly best matched by a value of \( L_2 = 0 \), indicating that the BOX interface is an efficient sink and plays an important role in the control of defects, deactivation and TED in SOI layers. Recent quantitative TEM data [148] shows a similar trend, with a strong dependence on distance between EOR and BOX.

### 5.3.4 Theory

Returning to the explanation in Chapter 3, for SOI there are two interstitials fluxes emerging from the EOR band, one towards the surface and another towards the upper BOX interface. The closer the EOR is to the BOX interface the steeper the flux of interstitials. This in turn causes acceleration in the dissolution of the EOR defects, leading to a reduced fluence of interstitials, integrated over time, in the direction of the Si surface where the dopant is located. In addition for the 32 keV PAI, part of the excess interstitial distribution is cut by the BOX interface. This means that a proportion of the excess Si interstitials remain effectively trapped within the BOX and so do not contribute to the B deactivation.

An updated schematic representation of the competition between the front and back SOI interfaces as sinks for interstitials is shown in Figure 5-23, for the case of the 20 and 32 keV Ge PAI. They are shown as a sequence of captions for increasing thermal budget.
Figure 5-23 Schematic representation of the interstitial fluxes for (a) 20 keV Ge PAI in bulk Si and (b) SOI compared with a (c) 32 keV PAI in SOI, for increasing thermal budget.

In the first case, 20 keV PAI bulk Si (top) from left to right, there is an interstitial gradient towards the surface from the EOR defect band, during annealing. As the thermal budget is increased the concentration of interstitials in the EOR band reduces due to dissolution of defects and therefore the gradient becomes less steep. For the 20keV PAI in SOI (middle) there is also an interstitial flux towards the BOX interface. This reduces the
number of interstitials that are available to reach the surface. Comparing this with the bulk Si case, for the same thermal budgets, in SOI the EOR dissolution is greater.

For the 32 keV PAI in SOI (bottom), first the EOR band has a lower concentration of interstitials in it to begin with compared with 20 keV PAI in SOI, as some are trapped within the BOX. Also the defect band is much closer to the BOX interface, thus the gradient of interstitials towards the back interface is steeper, allowing a faster dissolution of defects in the EOR band for the same thermal budget when compared to either the 20 keV PAI in SOI or in bulk Si.

The results presented in this chapter have demonstrated and explained an optimal approach for pre-amorphisation in SOI. Two phenomena are involved; (i) the SOI BOX interface acting as an efficient sink for Si self interstitials and (ii) the overlap of the interstitial profile with the BOX interface reducing the initial number of interstitials within the Si overlayer as some become effectively trapped within the BOX. The consequent reduction in the number of interstitials driving BIC formation in the near surface region leads to more stable electrical activation, less TED, and a more abrupt junction. The optimum result is achieved by tailoring the Ge PAI to ensure that the amorphous / crystalline interface is placed as close as possible to the BOX, while still maintaining a single-crystal Si layer adjacent to the upper BOX interface for reliable SPER.
Demand for more powerful electronic devices has led to the miniaturisation of transistor dimensions in order to improve CMOS device performance. The requirements for p-type s/d extension regions are ultrashallow junctions with a low sheet resistance. For the 2007 technology generation these are $X_j = 7.5$ nm and $R_s = 1368\, \Omega /\square$, specified by the ITRS.

One of the main problems for creating these junctions is the channelling of B atoms during implantation. This gives rise to a B channelling tail and increases the junction depth and degrades its steepness. To overcome this problem pre-amorphisation is used. This technique also has the benefit of increasing B activation, since dopant atoms are incorporated onto lattice sites during the subsequent SPER of the amorphous layer. The main problem associated with the pre-amorphising implant is the generation of damage in the form of Si interstitials and vacancies. During annealing the vacancies and interstitials recombine, leaving behind excess interstitials which then agglomerate into a band of EOR defects which are situated just below the former a/c interface.

Upon further annealing these extended defects transform from clusters to \{113\} defects and then into dislocation loops. During this process they release self-interstitials that migrate towards the nearest available sink, in bulk Si this is the top Si surface where the B implant is situated. As they approach the surface they interact with B atoms causing TED and complex with the B atoms to form BICs. TED is manifested by an increase in $X_j$, while BIC formation is evidenced by a rise in $R_s$ due to deactivation of dopant atoms.

In SOI it had been postulated that the BOX interface may also act as a sink and so cause interstitial migration away from the B distribution towards the BOX. It is important to study the effects of SOI on dopant activation and diffusion in terms of integration, as SOI is predicted to be the starting substrate of choice by the ITRS from 2008 [3].

In order to evaluate this hypothesis the objectives were set out (1) to ascertain the annealing temperature consistency between bulk Si and SOI wafers, (2) if the buried interface can be a potential sink for interstitials and (3) to optimise the technique with the premise of meeting the requirements of the ITRS.

To carry this out these objectives a range of pre-amorphisation conditions (Ge energies 8 keV to 36 keV with a dose $1 \times 10^{15} \, \text{Ge cm}^{-2}$) have been studied for low energy B implants (500 eV $2 \times 10^{15} \, \text{B cm}^{-2}$). The implants were carried out and compared between bulk Si
and SOI wafers, with a 55 nm top Si overlayer. Isochronal (60 s) annealing at temperatures ranging from 700 °C to 1000 °C were performed in order to reveal the electrical activation / de-activation cycle and to study the diffusion of the B profile. An array of analytical techniques were used, Van der Pauw resistivity combined with Hall Effect, SIMS and TEM. Further to this MC simulations were used to model the efficiency of the buried interface for capturing interstitials and comparisons were made between the simulated and electrical data. Conclusions from the main results are presented here:

**Annealing of Bulk Si and SOI Wafers**

It has been suggested in the literature whether the temperature experienced by SOI wafers during annealing was the same as that experienced by bulk Si wafers for the same set of processing conditions. This is not only important in the research environment, but also in industrial processing. In order to make realistic comparisons between both substrate types, SPER velocities were measured after a range of PAIs in bulk Si and SOI. The results showed that the re-growth velocity was the same for both materials. As the SPER velocity is a temperature dependant process, the fact that it was the same for both substrate types indicates that they both experienced the same annealing temperature. It was also determined that the re-growth velocity was not affected by the PAI energy. The presence of B at high concentrations increases the SPER velocity, at 570 °C this was ~0.5 nm/sec compared to its intrinsic value of ~0.29 nm/sec at this temperature.

**The Buried Interface as a Sink for Interstitials**

There has been conflict in the literature about whether the upper BOX interface has beneficial or detrimental effects on the activation and diffusion of dopants. This work was undertaken to study this issue. It has been postulated that the upper BOX interface in SOI allows for the recombination of interstitials. Although a competing hypothesis is that the interstitials are reflected by the interface.

The results in Chapter 4 of this thesis show that in SOI wafers compared to bulk Si with an 8 keV Ge PAI there is very little difference between the two with respect to dopant behaviour (activation and diffusion). However with the 20 keV PAI there was a reduced amount of de-activation in SOI when compared to bulk Si (36% reduction in $R_S$ from the value at 700 °C and that at 850 °C) and also less TED was observed. SIMS results also show a reduction in the localised peak in the B depth distribution corresponding to the decoration B of EOR defects by B in SOI wafers. This was correlated with a lower
density of defects in the EOR band (observed by TEM micrographs). This evidence is interpreted by arguing that the two interfaces in SOI material, the upper BOX and the Si surface, act as sinks for interstitials. It is the competition between these two sinks that improves the junction properties (smaller $R_s$ and $X_j$). By increasing the PAI energy the EOR defects are positioned closer to the upper BOX interface. This results in a larger flux of interstitials towards it and thus a higher absorption of interstitials at this interface. With a corresponding reduced flux towards the Si top surface region where the B dopant is located.

**Optimisation of the PAI Technique in SOI**

Having studied and understood that the upper BOX interface can act as a sink for interstitials in SOI. Where the relation between the distance of the EOR band from the buried interface can control the dopant activation and diffusion. Experiments were then designed to study and enhance this effect further.

Chapter 5 studied the optimisation through careful design of implantation parameters. PAI energies were chosen to situate the EOR band closer and close to the BOX interface. This effectively reduced the distance between the two, where the best results were seen for a 32 keV Ge PAI in SOI. The results for this sample showed that for a temperature range of 700 – 1000 °C the $R_s$ is almost constant at $\sim 800 \ \Omega/\square$. Very little $R_s$ deactivation was observed $\sim 80 \ \Omega/\square$ and was compared to $\sim 480 \ \Omega/\square$ for the same implant in bulk Si, representing a 6x improvement in $\Delta R_s$ for SOI. TED is also reduced in SOI, showing an improvement of 1.5x at 850°C compared to bulk Si. Increasing the PAI energy resulted in a reduction in electrical deactivation and TED, for both substrates but with a larger effect for SOI wafers. A corresponding $X_j$ of $\sim 19$ nm at 700 °C is produced for the optimised condition of 32 keV Ge PAI in SOI. Comparing this data to the ITRS requirements for 2007 ($X_j = 7.5$ nm and $R_s = 1368 \ \Omega/\square$) in terms of $R_s$ the challenge is met with this technique, however not for $X_j$. By tailoring the B implant still further and combining it with spike or non melt laser [77] anneals it is speculated that perhaps the full ITRS conditions can then be met.

The 32 keV Ge PAI also showed interesting XTEM results, primarily, only a crystal seed of $\sim 2$ nm is necessary for SPER to occur. Also the layer does not need to be continuous; it can contain Si islands where re-growth occurs laterally as well as vertically. This works because the lattice within each island belongs to a common lattice originating in the initial single crystal Si layer prior to PAI, and remains locked in place after PAI by its bonding to
the BOX. This is an important issue for PAI in SOI, since an effective seed is needed to give defect free re-growth; these results show that it does. This knowledge helps to remove any doubts about using this process in SOI material. The second important piece of information is the overlapping of the excess interstitial profile with the BOX interface, shown both by XTEM, SIMS and simulations. A lower as-implanted population of excess Si interstitials means that there are already fewer interstitials in SOI compared to bulk Si. This results in fewer excess interstitials available to form EOR defects and therefore fewer which interact with the B implant.

Two phenomena are thought to be responsible for the effects seen in this work; (i) the SOI BOX interface acting as an efficient sink for self interstitials and (ii) the overlap of the interstitial profile with the BOX interface, reducing the initial number of interstitials within the Si overlayer.

MC simulations showing the relative effectiveness of the upper BOX interface in SOI were performed. Conclusions are that the recombination length of Si interstitials with the BOX interface is fitted best by a value of near zero for all PAI energies used. This indicates that the BOX interface is an efficient sink for interstitials and plays an important role in the control of defects, deactivation and TED in SOI layers.

**MAIN FEATURES**
Several main features have resulted from this research:

1. In the RTA setup used in this work, SOI and bulk Si reach the same temperature when annealed together. A comparison with the work of Mannino [138], which showed significant differences in temperature for SOI and bulk Si samples, suggests the good control achieved here is a result of the placement of lamps above and below during annealing, therefore negating radiation reflectivity effects in SOI.

2. Increasing PAI energy corresponds to a decrease in the distance between the EOR defect band with the upper BOX interface, and shows a subsequent decrease in $R_S$ and reduction in TED.
3. The SOI BOX interface acts as an efficient sink for self interstitials, with a near zero value for recombination length.

4. The overlap of the interstitial profile with the BOX interface reduces the initial number of interstitials within the Si overlayer.

5. A thin (~2 nm) surviving crystal Si layer between a/c and upper BOX interfaces is sufficient to seed SPER.

6. This technique is suited for industry, due to its low implantation energy needs allowing easy integration into existing processes.

Finally, the consequent reduction in the number of interstitials driving BIC formation in the near surface region leads to more stable electrical activation, less TED, and a more abrupt junction. The optimum result is achieved by tailoring the Ge PAI to ensure that the amorphous / crystalline interface is placed as close as possible to the BOX, consistent with the requirement to maintain a single-crystal Si layer adjacent to the upper BOX interface for reliable SPER. The method used here for PAI in SOI can still be further optimised and understanding its effects in alternative conditions is important, as discussed in the following section.

FURTHER WORK
The understanding of the pre-amorphisation technique combined with SPER in SOI has been undertaken in this work, showing the effects and their benefits. However to continue this research several avenues can be taken and are outlined here.

Extended Optimisation
In order to fully meet the requirements of the ITRS for p-type s/d extensions in CMOS devices it is expected that further optimisation is needed. In terms of $R_s$ the requirement is met. For $X_j$ and subsequent TED it is possible that tailoring the B ion energy and dose will have an effect. If the $R_p$ of the B profile is closer to the top Si surface, effectively positioned further away from the EOR band and closer to an interstitial sink, results have shown, even in bulk Si that this can improve dopant behaviour. Also anneal conditions could be optimised; perhaps using spike or non melt laser anneals to reduce the ramping rates, also shown in the literature to reduce TED.
Alternative dopants

This technique has the potential to improve the behaviour of other dopant species, provided their diffusion and/or clustering is interstitial mediated. Work has already begun in this area, with P and BF$_2$ implants; presently results show little effect or differences between SOI and bulk Si with these dopants – however these results are very preliminary.

Modelling

A progression from the basic model used in this work could be undertaken in order to fine tune the current calculation for the dose of interstitials related to B deactivation. It is hoped that the experimental data from this work can serve as a building block for a model of the interstitial sinking efficiency of the upper BOX interface, to be used for prediction of B TED and deactivation in SOI.
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## APPENDIX

### APPENDIX A – FOUR POINT PROBE CORRECTION FACTOR TABLES

<table>
<thead>
<tr>
<th>CF1 (d/s)</th>
<th>Circle</th>
<th>Square</th>
<th>CF1 (L/W = 2)</th>
<th>CF2 (&lt;0.4)</th>
<th>F(t/s)</th>
<th>Square</th>
<th>CF2 (t/s)</th>
<th>F(t/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>0.9988</td>
<td>0.9994</td>
<td></td>
<td>0.400</td>
<td>0.995</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.25</td>
<td>1.2467</td>
<td>1.2248</td>
<td></td>
<td>0.500</td>
<td>0.9974</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.50</td>
<td>1.4788</td>
<td>1.4893</td>
<td>1.4893</td>
<td>0.555</td>
<td>0.9948</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1.75</td>
<td>1.7196</td>
<td>1.7238</td>
<td>1.7238</td>
<td>0.625</td>
<td>0.9896</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.00</td>
<td>1.9475</td>
<td>1.9475</td>
<td>1.9475</td>
<td>0.714</td>
<td>0.9798</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.50</td>
<td>2.3532</td>
<td>2.3541</td>
<td>2.3541</td>
<td>0.833</td>
<td>0.9600</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.00</td>
<td>2.2662</td>
<td>2.4575</td>
<td>2.7000</td>
<td>1.000</td>
<td>0.9214</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4.00</td>
<td>2.9289</td>
<td>3.1127</td>
<td>3.2246</td>
<td>1.111</td>
<td>0.8907</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5.00</td>
<td>3.3625</td>
<td>3.5098</td>
<td>3.5749</td>
<td>1.250</td>
<td>0.8490</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7.50</td>
<td>3.9273</td>
<td>4.0095</td>
<td>4.0361</td>
<td>1.429</td>
<td>0.7938</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10.00</td>
<td>4.1716</td>
<td>4.2209</td>
<td>4.2357</td>
<td>1.667</td>
<td>0.7225</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15.00</td>
<td>4.3646</td>
<td>4.3882</td>
<td>4.3947</td>
<td>2.000</td>
<td>0.6336</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>20.00</td>
<td>4.4364</td>
<td>4.4516</td>
<td>4.4533</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>32.00</td>
<td>4.4791</td>
<td>4.4878</td>
<td>4.4899</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>40.00</td>
<td>4.5076</td>
<td>4.5120</td>
<td>4.5129</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Infinity</td>
<td>4.5324</td>
<td>4.5324</td>
<td>4.5325</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
APPENDIX B – HALL RESULTS FROM THEORETICAL CALCULATIONS

SPECIMEN
Wafer ID: B 500eV 2E15
Batch ID: n3.7s set 2 rep.
Material: SOI + Ge 24keV 1E15
Description: 950°C for 60s
Thickness: 55 nm

MEASURING CONDITIONS
l-meas: 0.00021 A
Temperature: AMB
Field: 0.328 T
Targ.Vr: 0.02 V

RESULTS SUMMARY FROM HALL SOFTWARE
Qe: 1.60218E-19 C
Rs: 416.5 \( \Omega \)
\( R_{hs} \): 1.55 m\( \Omega \)C

RESULTS SUMMARY FROM THEORETICAL CALCULATIONS
Rs = 416.492 \( \Omega \)
\( R_{hs} \): 1.56 m\( \Omega \)C

RESISTIVITY MEASUREMENTS
\( V \) (V) \( R \) (\( \Omega \))
V34 = 0.01941 R21,34 = 92.43
V43 = 0.01942 R12,43 = 92.49
V41 = 0.01918 R32,41 = 91.33
V14 = 0.01918 R23,14 = 91.33
V12 = 0.01941 R43,12 = 92.43
V21 = 0.01941 R34,21 = 92.43
V23 = 0.01918 R14,23 = 91.33
V32 = 0.01919 R41,32 = 91.38

HALL VOLTAGE MEASUREMENTS
+B Field
V24p = 0.000140
V42p = -0.000128
V13p = 0.000074
V31p = -0.000084

-B Field
V12p = -0.000077
V43n = 0.000082
V13n = -0.000141
V31n = 0.000131

\( V_c \) = 0.000217
\( V_o \) = 0.000210
\( V_e \) = 0.000215
\( V_r \) = 0.000215

RESULTS SUMMARY FROM THEORETICAL CALCULATIONS
Rs = 416.492 \( \Omega \)
\( R_{hs} \): 1.56 m\( \Omega \)C

Mob (\( \mu \)) (cm\( ^2 \)Vs) = 37.34

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APPENDIX C – TYPICAL SET OF HALL RESULTS

Accent HLb50U Hall System
Measured on 20/07/07 at 14:53

**SPECIMEN**
Wafer ID:  
Batch ID:  
Material: Si  
Description: n3.7s set2 rep  
Thickness: 0.000 μm

**MEASURING CONDITIONS**
I-meas: 0.21 mA DC  
Temperature: AMB  
Field: 0.328 Tesla  
Targ.Vr: 20 mV

**RESULTS SUMMARY**

<table>
<thead>
<tr>
<th>Rs:</th>
<th>416.5 Ω/sq</th>
<th>RsH: +1.55 m²/C</th>
<th>Na: +4.01e+14 /cm²</th>
</tr>
</thead>
<tbody>
<tr>
<td>R:</td>
<td>Ω/cm</td>
<td>Mob: 37.3 cm²/V-s</td>
<td>N: /cm³</td>
</tr>
</tbody>
</table>

**CONTACT CHECK**

<table>
<thead>
<tr>
<th>Pair</th>
<th>Ohms</th>
</tr>
</thead>
<tbody>
<tr>
<td>12</td>
<td>1729</td>
</tr>
<tr>
<td>23</td>
<td>1649</td>
</tr>
<tr>
<td>34</td>
<td>1607</td>
</tr>
<tr>
<td>41</td>
<td>1956</td>
</tr>
<tr>
<td>13</td>
<td>1872</td>
</tr>
<tr>
<td>24</td>
<td>1670</td>
</tr>
</tbody>
</table>

**RESISTIVITY**

<table>
<thead>
<tr>
<th>Meas</th>
<th>Vm</th>
<th>Sym Factor R-sheet</th>
</tr>
</thead>
<tbody>
<tr>
<td>43</td>
<td>1.941e-02</td>
<td>1.01 1.00 416.5</td>
</tr>
<tr>
<td>41</td>
<td>1.918e-02</td>
<td>1.01 1.00 416.5</td>
</tr>
<tr>
<td>21</td>
<td>1.941e-02</td>
<td>1.01 1.00 416.5</td>
</tr>
<tr>
<td>23</td>
<td>1.918e-02</td>
<td>1.01 1.00 416.4</td>
</tr>
</tbody>
</table>

**HALL MEASUREMENTS**

<table>
<thead>
<tr>
<th>Misalignment</th>
<th>Offset applied</th>
<th>V-hall North</th>
<th>V-hall South</th>
<th>V-hall (mean)</th>
<th>V-hall (over all cycles)</th>
</tr>
</thead>
<tbody>
<tr>
<td>+2.34e-04</td>
<td>+2.00e-04</td>
<td>+1.40e-04</td>
<td>-7.66e-05</td>
<td>+1.107e-04</td>
<td>+1.07e-04</td>
</tr>
<tr>
<td>-2.33e-04</td>
<td>-2.00e-04</td>
<td>-1.28e-04</td>
<td>+8.20e-05</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

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APPENDIX D – THERMAL BUDGET SPER PROGRAM

```c
CCC

C PROGRAM T
C
C Program calculates re-growth for a given time-temperature cycle
C
C

DIMENSION TIME_KNOT(10000),TC_KNOT(10000)

C THICKNESS Initial thickness of amorphous layer (nm)
THICKNESS=175.

C Number of time-temperature knots
NKT=10000

C Timestep of RTA T-t data
DT=0.1

C Temperature correction
C 700C TEMP_CORR=-.2
TEMP_CORR=+2.

NK=0

C Read RTA T-t data (1 column with Tc*10 at intervals of 0.1s)
DO 20 IK=1,NKT
   READ(5,*,END=30) INTEGER_TC
   NK=NK+1
   TIME_KNOT(IK)=FLOAT(IK)*DT
   TC_KNOT(IK)=INTEGER_TC/10.+TEMP_CORR
20 CONTINUE
30 CONTINUE

DT_INIT=0.01
```
BK=8.6173E-5
THICK1=THICKNESS
THICK2=THICKNESS
R01=3.1E15
RE1=2.68
R02=2.04E15
RE2=2.64

C Initial temperature
TC=TC_KNOT(1)
TEMP=TC+273.15

C Time at end of anneal cycle
TIME_MAX=TIME_KNOT(NK)

C Initialize quantities for time looping

C Time, time step, and integral of Dx(t)dt
TIME=TIME_KNOT(1)
DT=DT_INIT

C Start time loop

DO 500 K=1,3e7

C Update time
TIME_OLD=TIME
TIME=TIME+DT

C End of anneal?
IF (TIME.GT.TIME_MAX) THEN
  GO TO 600
END IF

C Update temperature
C Piecewise-linear interpolation from T-t cycle data

DO 250 IK=2,NK
   IF( (TIME.GE.TIME_KNOT(IK-1))
     & .AND.(TIME.LT.TIME_KNOT(IK)))
   & THEN
      TC=TC_KNOT(IK-1)
      & +(TC_KNOT(IK)-TC_KNOT(IK-1))
      & *(TIME-TIME_KNOT(IK-1))
      & /(TIME_KNOT(IK)-TIME_KNOT(IK-1))
   END IF
250 CONTINUE
   TEMP=TC+273.15

C Update temperature-dependent quantities

   BKT=BK*TEMP

C R1 (re-growth rate according to Olson)
C R2 (re-growth rate according to Haynes)
   R1=R01*EXP(-RE1/BKT)
   R2=R02*EXP(-RE2/BKT)

C Update (decrement) layer thickness
   THICK1=THICK1-R1*DT
   THICK2=THICK2-R2*DT

C End of time loop
500 CONTINUE

600 CONTINUE

   THICK=0.5*(THICK1+THICK2)
   WRITE(6,*),THICKNESS=',THICK

   STOP
END