Stable transistors in hydrogenated amorphous silicon

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Thin-film field-effect transistors in hydrogenated amorphous silicon are notoriously unstable due to the formation of silicon dangling bond trapping states in the accumulated channel region during operation. Here, we show that by using a source-gated transistor a major improvement in stability is obtained. This occurs because the electron quasi-Fermi level is pinned near the center of the band in the active source region of the device and strong accumulation of electrons is prevented. The use of source-gated transistors should enable stable analog circuits to be made in amorphous silicon. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1772518]

Thin-film field-effect transistors (FETs) made using hydrogenated amorphous silicon (*a*-Si:H) as the semiconductor are notoriously unstable. This instability, characterized by a large shift in threshold voltage and a reduction in drain current during operation,[1] severely limits their use in both analog and digital circuits for displays and large area electronics, in general. As such, the most important application is as a simple pixel switch in actively addressed liquid-crystal display arrays with anything more demanding such as peripheral or pixel circuitry being difficult or impossible.

Silicon dangling bond defects are formed over a wide range of energies within the band gap of amorphous silicon in regions where the electron quasi-Fermi level moves from its equilibrium position determined during the growth of the *a*-Si:H.[1,2] This position, close to the center of the band in undoped material, determines the energy distribution and number of the different bonding configurations between silicon and hydrogen when in chemical equilibrium. For a FET, the electron quasi-Fermi level in the channel region moves toward the conduction band as the transistor is biased into accumulation.[3,4] This is accompanied by an increase in the electron concentration. The microscopic mechanisms for the creation of dangling bond defect states are complex[3] as the material strives to achieve an equilibrium between the weak silicon–silicon bonds, the dangling bond defects and the electron concentration.[4] Defect states trap electrons and there is a shift in the threshold voltage of the FET.

Since the defect generation mechanism is fundamental, there is very little that can be done about it in FETs as they rely on electron accumulation in a channel region for their operation. At a given gate voltage, drift and instability are independent of current and are particularly severe when operating well above threshold.

Source-gated transistors (SGTs)[5] form a class of thin-film transistors in which the current is controlled entirely by the source.[6] Their most important advantage compared with a FET is the much smaller saturation voltage V_{SAT}. An example of the characteristics of a SGT made using a Schottky barrier source is shown in Fig. 1 together with a schematic showing its structure. V_{SAT} at $V_G=20$ is <2.5 V. This compares with 17 V (V_G-V_T) for a FET made with the same layers. The SGT also has a large output impedance.[5,6] The main difference with a FET is the provision of a source barrier rather than an ohmic contact and a gate located below it that controls the current flowing across the reverse biased barrier. Current saturation occurs when the source barrier depletes the underlying *a*-Si:H. Ion implantation is used to control the source barrier height and compensate for the region between the source and drain contacts.[6,7] This region [(d) in Fig. 1] forms a parasitic FET in series with the gate-controlled source which determines the off current, while the gated source barrier controls the on current. A full description of how the SGT works and how it was made can be found in Refs. 5 and 6.

FETs and SGTs were made using the same depositions of insulator and *a*-Si:H. The insulator was SiN grown at 250 °C to a thickness of 300 nm while the *a*-Si:H also grown at 250 °C had a thickness of 100 nm. The hydrogen content was ~10%. The transfer characteristics of an SGT and FET following stress at 30 °C, 20 V gate voltage for various times are shown in Fig. 2. The FET shows the classical threshold voltage shift, which affects the current up to the maximum gate voltage of 20 V. The SGT has a current determined by the height of the source barrier and a far su-

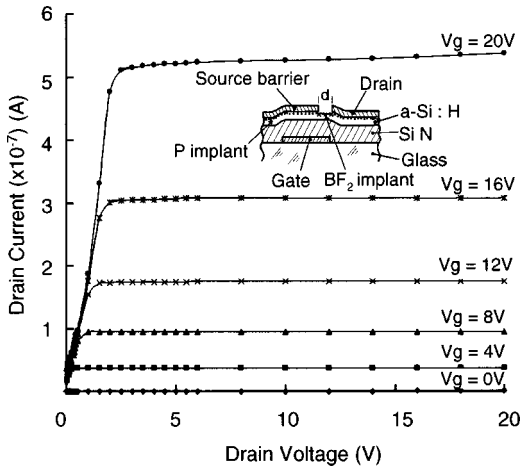

FIG. 1. Transistor characteristic of a SGT similar to those used in this work ($W=600$ microns and $d=6$ microns). The characteristic shows a small saturation voltage and high output impedance. The inset shows the transistor structure made using ion implantation.

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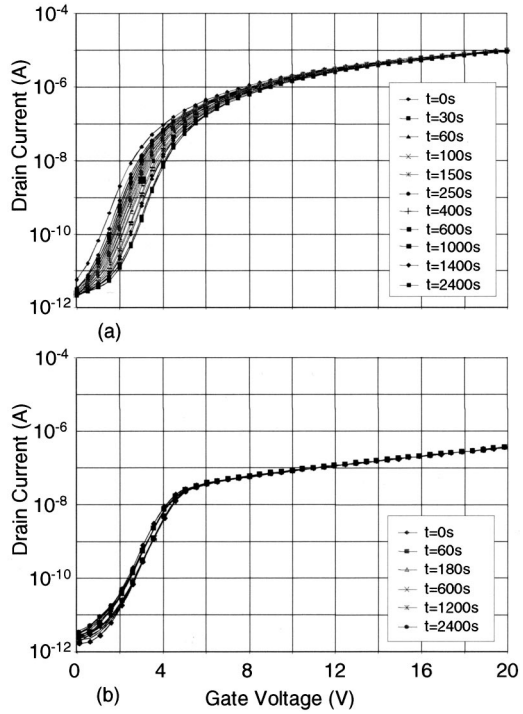

FIG. 2. Drift in the transfer characteristic of (a) a FET and (b) SGT measured at $V_D=5$ V after various stressing times ($W=120$ microns, $L=10$ microns, and $d=6$ microns).

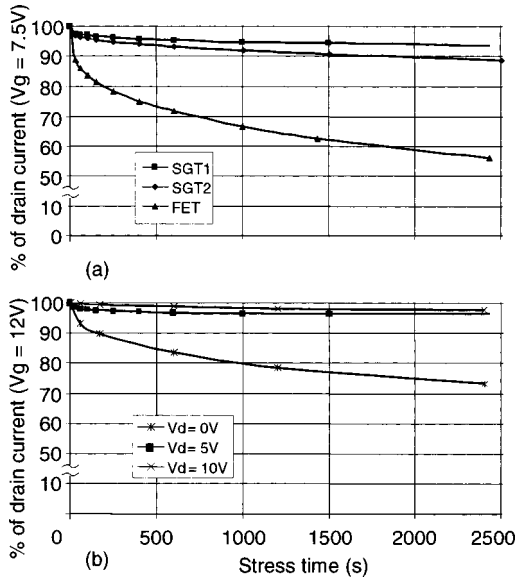

FIG. 4. (a) Change in drain current during stressing of SGTs and a FET ($V_D=5$ V). (b) Drain current degradation for different drain voltages applied to an SGT during stressing. The same layer depositions were used in all cases.

perior stability. The reason for the excellent stability of the SGT lies in the fact that the electron quasi-Fermi level in the depleted source at the nitride–semiconductor interface is close to midgap and similar to where it was when the *a*-Si:H was grown. Therefore, the distribution of states in chemical equilibrium is very similar and few states are generated. In contrast, the electron quasi-Fermi level in the FET moves toward the band edge (Fig. 3) and states are generated as the distribution of states in the *a*-Si:H moves toward a chemical equilibrium.

The decrease in current as a percentage of the initial current during current stressing is shown in Fig. 4(a) for a FET and a high and low current SGT. It is seen that the SGT is much more stable. Extrapolating the decay curves shows that the current through the FET under these accelerated stress conditions decays by 50% in ≈ 1 h. The corresponding values for the SGTs are $>10^5$ h and 10^8 h for the high and low current devices, respectively. The difference between the two SGTs arises because they operate at different current densities. SGT2 had a current density per unit width nearly ten times larger than SGT1 and within a factor of 2 smaller than the FET. Computer calculations (SILVACO) show that the electron concentration in the FET is a factor $>10^4$, and $>10^3$ higher than in the source of the low and high current SGTs, respectively. Our assumption that the quasi-Fermi level is in the center of the band is, therefore, less valid as the current increases but the high current device is still much more stable than the FET.

Our understanding of the improved stability of the SGT compared to the FET suggests that the stability will be strongly dependent on drain bias. The source will not be depleted for small drain bias and the stability will be "FET like," while for $V_D > V_{SAT}$ the stability will be "SGT like." This feature is illustrated in Fig. 4(b) where accelerated stress tests are performed on a similar device to SGT1 but with different drain voltages. It is clearly seen that an undepleted source ($V_D=0$) drifts rapidly while applying a drain voltage above the saturation voltage (2 V) provides us with a very stable mode of operation. The improvement between 5 V and 10 V occurs because the parasitic FET also becomes depleted at higher drain voltages. The change in current at the end of the accelerated stress tests was $<2.5\%$, which suggests that under normal operating conditions the instability would be negligible over many thousands of hours. Therefore, we should be able to achieve stable operation at low currents using gate voltages well above the threshold region where threshold variations are the most deleterious. It should be noted that a SGT made using a Schottky barrier source has a characteristic that is more sensitive to temperature than a FET, especially at low currents, and proper circuit design is required to correct for this.

In summary, it has been shown that the stability of a SGT in *a*-Si:H under temperature–voltage stress is very much better than a standard FET. This arises from the fact that the current through a SGT is controlled by a fully de-

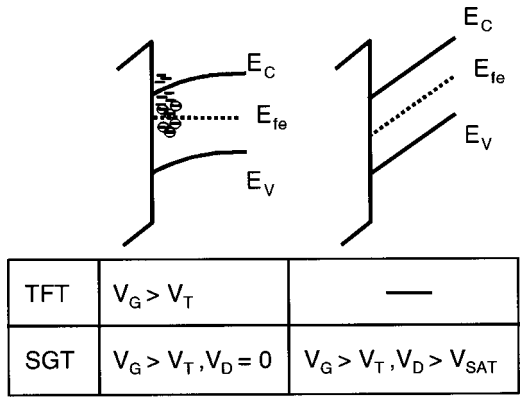

FIG. 3. Band structure at the semiconductor insulator interface for FET and SGT showing the position of the electron quasi-Fermi level (E_{fe}). The circles are silicon dangling bond electron traps generated during electron accumulation.

pleted source and the electron quasi-Fermi level is pinned close to the middle of the band gap where the equilibrium density of states is similar to that introduced when the *a*-Si:H was grown. This feature of the SGT has implications for all materials where transistor stability is dependent on changes in the position of the quasi-Fermi level.

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