A RECORDING-HEAD ADDRESSING-SYSTEM
FOR A
MEDIUM SPEED, LINE-AT-A-TIME
FERROGRAPHIC PRINTER

BY
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Master of Philosophy at the University of Surrey.

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The general principle of printing is defined in which a recording surface is drawn past a single row of writing points for recording text in mosaic form in line-at-a-time mode. This principle is assessed for diverse methods of recording. Details are given of recording by magnetic means.

A system for addressing magnetic recording heads has been developed and detailed discussion is given of basic design considerations, both for general addressing systems, and for the particular case of a printer having 132 characters per line, 9 mosaic columns per character, and a character repertoire of 96, for use on a 2400 baud channel.

Operation at 1800 lines per minute has been achieved and a specimen of the print quality obtained is given.

Recommendations and suggestions for further work and system extensions conclude the study.
TO MY WIFE AND SON
ACKNOWLEDGEMENTS

The author wishes to express his gratitude to ITT Creed for allowing him to carry out the work, to his university supervisor Mr. L. S. Mansi, and to his industrial supervisor Mr. F. P. Mason for their co-operation and support throughout the period of research.

Thanks are also due to Dr. Ream of the University of Surrey, for his careful scrutiny of the manuscript.
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<td>A5.1</td>
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<td>Switch decoding</td>
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### LIST OF SYMBOLS

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<tr>
<td>$\alpha_n$</td>
<td>normal alpha</td>
</tr>
<tr>
<td>$\alpha_i$</td>
<td>inverted alpha</td>
</tr>
<tr>
<td>$\omega_n$</td>
<td>normal cut-off frequency</td>
</tr>
<tr>
<td>$\omega_i$</td>
<td>inverted cut-off frequency</td>
</tr>
<tr>
<td>$I_c$</td>
<td>collector current</td>
</tr>
<tr>
<td>$I_b$</td>
<td>base current</td>
</tr>
<tr>
<td>$V_{ce(\text{off})}$</td>
<td>the voltage between collector and emitter in the off condition</td>
</tr>
<tr>
<td>$V_{ce(sat)}$</td>
<td>the saturation voltage between collector and emitter</td>
</tr>
<tr>
<td>$I_{CEO}$</td>
<td>The collector leakage current with the base open circuit</td>
</tr>
<tr>
<td>$V_{be}$</td>
<td>the base-emitter voltage</td>
</tr>
<tr>
<td>$t_r$</td>
<td>current rise time</td>
</tr>
<tr>
<td>$t_f$</td>
<td>current fall time</td>
</tr>
<tr>
<td>$T$</td>
<td>time constant or periodic time</td>
</tr>
<tr>
<td>$V_{cc}$</td>
<td>positive collector supply voltage</td>
</tr>
<tr>
<td>$Hz$</td>
<td>periodic frequency</td>
</tr>
<tr>
<td>$s$</td>
<td>Laplace variable</td>
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This work was conducted at the ITT Creed Research and Development Laboratories, Burgess Hill, Sussex, in the Department of Applied Research, during the period October 1968 to March 1970.

It represents part of the study required to assess the technical feasibility and commercial viability of a medium speed ferrographic dataprinter for use on a 2400 baud channel. These studies were jointly undertaken by the Standard Telecommunication Laboratories Ltd. (STL) Harlow, Essex, and ITT Creed.

The basic research on the ferrographic process, recording head design, magnetisable surface, and magnetic ink, was the responsibility of STL. The application of this information in the design of a medium speed printer, and the practical realisation, was the objective of ITT Creed, and culminated in a demonstration of an analytical machine at the ITT headquarters in Brussels during March 1970.

The following sections pertain to the author's work in developing a head addressing system with the associated logic necessary to simulate accurately the full speed printing capability of a medium speed line-at-a-time dataprinter.
CHAPTER 1
NON-PERCUSIVE PRINTING

The speed of modern transmission systems has increased considerably over the past decade such that printers employing percussive techniques have become both costly and unreliable. Current trends are towards non-percussive printing, thereby avoiding the problems imposed by mechanical inertia.

There are numerous methods of non-percussive printing and the more common of these which have already been exploited will be briefly discussed.

1.1 Xerographic printing with electrostatically charged paper.

In this method a sheet of paper is drawn past an array of recording styli. A negative voltage applied to the styli causes spots of excess charge to be deposited on the paper surface. The charged patterns are then made visible by powder application. A heater permanently fixes the ink by softening a thermoplastic coating on the paper.

This system although having a very high speed capability suffers from the disadvantages that a high voltage is needed which is not compatible with modern semiconductor techniques, and that special paper is required. In addition the performance deteriorates in humid atmospheres and multiple copies are not available unless the input data is re-interrogated.
1.2 **Xerographic printing using electrostatically charged drum.** 3, 9

In this system a precharged photo-conductive selenium drum is exposed to a pattern of light from a cathode-ray tube which discharges selected areas. Charged powder is then cascaded on to the drum, which adheres to these areas, forming the pattern in powder. Paper is brought into contact with the drum and the powder transferred electrostatically. Finally the powder is fixed by heating.

The method suffers the same disadvantages as the electrostatic system except that special paper is not required.

1.3 **Magnetic paper** 3, 10, 11

One method records mosaically and uses permeable pins arranged in a helix round a drum, their ends passing close to a bar which can be magnetised in accordance with given signals. The paper is placed between the pins and the bar, and if the bar is magnetised a strong field exists between the point of the pin and the bar, which magnetises the special paper. With this is used a mosaic character generator comprising a cathode-ray tube with the repertoire cut out of a mask which is scanned in time with the passage of the pins past the bar, and the resulting scans are photo-electrically sensed, amplified, and made to govern the field of the bar. However, any form of character generator could have been used.

Another method uses shaped magnetic poles arranged round the periphery of a drum. A sheet of magnetically coated
paper passes tangentially to the drum, and on the other side of the paper there is an electromagnet. By pulsing this electromagnet at the correct time the required character is magnetised on the paper. Subsequent powdering visualises the character, and heating fixes the print.

Both methods suffer the disadvantages of special paper, which is expensive and has a limited usable life.

1.4 Electrolytic

One method uses a single turn helix wound around a drum. Moistened paper is sandwiched between the helix and an iron bar. As the drum rotates, the point of contact between the helix and the paper varies, thus enabling the complete page width to be scanned. Modulation of the potential between the helix and the bar allows text to be built up in mosaic form by electrolytic deposition of iron on to the paper. It suffers the disadvantages that the paper rolls must be transported in sealed containers and that some 5 inches of paper is lost due to drying out of the paper.

Another method uses ordinary teleprinter paper wound round a tellurium platen. Underneath the platen is a wetting device which moistens the paper to make it electrically conductive. Pins in the recording heads slide with slight pressure over the rear side of the paper. The tellurium platen is connected to the negative side of a supply. If the pins are energised by connecting them to the positive side of the supply, current flows and tellurium is electrolytically dissolved from the platen, and transported into the paper.
Neither of the two foregoing methods can yield multiple copies.

1.5 Electrothermal

This method makes use of the discolouration which takes place with certain chemicals when heated. Some systems generate the heat by the passage of an electric current through the paper, whilst others rely on conduction from small heating elements acting as the recording transducers. These transducers build up the character as an array of dots. The method requires special paper.

1.6 Summary

The common methods of non-percussive printing have been discussed. They are electrostatic, magnet, electrolytic, and thermal, and their relative merits and de-merits have been presented.
CHAPTER 2

THE FERROGRAPHIC PROCESS

STL have developed a process 16, 17 whereby the pattern to be printed is first recorded on to a magnetic surface by means of an in-line configuration of recording heads. This is achieved by movement of the magnetic medium relative to the heads, which builds up the pattern as an array of dots.

Application of a powder comprising resin coated ferromagnetic particles results in the powder clinging only to the magnetised areas, giving visual indication of the pattern. The magnetic surface is then placed in intimate contact with ordinary paper thereby transferring most of the powder to it. Heat is then applied to melt the resin and seal the print.

STL have designated this process as FERRODOT®.

2.1 Application to page printing

For a page printer the magnetic surface takes the form of a drum, which is spanned by a line of recording heads, 6 mils apart. Rotation of the drum builds up the character mosaics in a line-at-a-time mode. Around the drum periphery is a powder application station, scavenging station to collect surplus powder, and an erasure station to remove the recorded pattern of dots in readiness for the next recording. The paper leaving the drum surface passes a heating or fixing station before egressing from the machine.

* Registered Trademark
The PERRODOT process does not suffer from any of the disadvantages outlined earlier, namely,

(a) High voltages

(b) Effect of humidity

(c) Re-interrogation of input data for multiple copies

(d) Use of special paper

and in addition has a dot writing time of less than 1 micro-second thus enabling very high speeds to be obtained. The only other system at present, whose speed is comparable is the electrostatic system, all others being significantly slower. A speed comparison of the various techniques has been made by Stirling and Mason and is included in Appendix A1. At the present state of the art, drum periphery speeds of 30 inches per second are possible, corresponding to about 12,000 lines per minute.

The FERRODOT process has the potentiality of producing multiple copies since the magnetic flux pattern is essentially non-volatile. However, for this application, certain constraints must be imposed on the system. These are:

(a) The message length must not exceed the drum capacity.

(b) Either

(i) It must be possible to hold up transmission while additional copies are being produced, or

(ii) sufficient drum recirculations can be made before the next line of text is received, or
Figure 1 shows the block diagram of the organisation of a medium speed Ferrodot dataprinter operating in a line-at-a-time mode.

Data is received serially over a line from the data source, and is converted into a parallel code. As each character is parallelised, it is placed into a collection store of capacity 10 characters. When the collection store is full, its contents are transferred rapidly into an action store of capacity 132 characters, thereby leaving the former ready to receive the next 10 characters. The purpose of the collection store is to act as a buffer between the action store and the serial-to-parallel converter during the printing period, when a new line of information is being received. Since transmission cannot be held up, it is temporarily stored in the collection store. The capacity of 10 characters is based on the shortest line to be accommodated, which is limited by the drum stepping mechanism. This mode of operation does however result in an economy of storage and has been fully documented. The collection store fills again and is emptied into the action store and this process repeats itself until an end of line signal is received, which initiates the printing cycle.

The action store which has accumulated a line of text is now operated such that successive characters appear at its
output, in an order identical to that in which they were received. Hence, the first character, corresponding to the extreme left hand character in the line, appears first at the output of the action store. After being clocked once the second character appears at its output, and after 132 clock pulses, the last character in the line appears. Since the output of the action store is in a parallel 7-unit code, it must be translated into a mosaic code. This process is achieved firstly by decoding the 7-unit code into all of its 128 combinations, which are then encoded by the mosaic generator. As successive characters reach the generator for the first time it emits the mosaic elements for the top rows of the character mosaics. This is shown in Figure 2 where the top row mosaics correspond to row 1. Therefore when the action store has been circulated once, all the top rows of all the characters in the line have been emitted from the mosaic generator.

Next the action store is circulated again and as the characters reach the mosaic generator for the second time, so the elements for the second rows are emitted. This process repeats itself until all the rows of all the characters have been emitted, and must be completed in the arrival time of the next 10 characters, which have accumulated in the collection store and require to be transferred into the action store.

Each mosaic row emitted has to be delivered to the recording heads which correspond to the character in the line of text of which that row forms part.
The delivery path for each row emitted differs from that of its predecessor, so that after each row is delivered, the old path is broken and a new path is set up.

There are many different ways in which the heads may be addressed and the criterion of least cost must operate to indicate the preferred switch deployment.

2.3 Summary

The Ferrographic process has been discussed with particular reference to page printing. A Ferrodot dataprinter has been described and the requirements for a head addressing system defined.
CHAPTER 3
HEAD GROUPING AND SELECTION

The following sections discuss the fundamental timing and switching considerations for the recording head current and serve to disclose the diversity of switch deployments for the case of a printer having 132 characters per line of text, 9 mosaic columns per character, and an input data rate of 300 characters per second. Based on the foregoing considerations and disclosures, an optimum arrangement for addressing the recording heads is evolved.

3.1 Method of Recording

STL advise a method of recording, by simultaneously energising two adjacent heads (but of opposite polarity) and using the surface of the drum to complete the magnetic circuit. This method, although requiring 10 heads as opposed to 9, means that twice the magnetising force is available for recording each element, and this is accompanied by a corresponding reduction in writing time. To produce alternate polarities, each head could be alternately wound or the directions of the currents could alternate. Alternate winding has the advantage of eliminating the problem of arranging the circuitry to route current in opposite directions through adjacent coils.

It will therefore be assumed that the method of alternate winding (as opposed to alternate current) will be adopted.

3.2 Magnetic Recording Heads

For the heads being used, a current of 1 ampere simultaneously in two adjacent tracks is necessary. The d.c.
Resistance of the head is 3 ohms and the inductance 0.5 microhenries. For the head alone a supply of about 5 volts (with a suitable series resistor) suffices to achieve the required current. However, when connecting leads of up to 1 foot length are allowed for, a supply voltage of up to 30 volts may be required, in order to achieve a high enough rate of change of current.

The necessary dwell period for the current in a pair of heads is 500 nanoseconds.

3.3 Speed of Operation

It is required to operate at 300 characters per second with a short line capability of 10 characters. Since it is not permissible to hold up transmission and an endless succession of 10 character lines may be received, a line of text must be recorded in the arrival time of 10 characters, that is, 33 mS. Of this 33 mS only 1/4 are available for actual recording, the rest being lost by virtue of the space between lines. In this space acceleration and deceleration of the drum occurs, as the drum advances stepwise with variable-duration inter-step pauses to accommodate variation of arrival time of long and short lines.

Since each character is based on a 9 x 15 dot matrix, the number of dots per line of text is:

\[ 9 \times 15 \times 132 = 17,820 \]

and these must be written in 1/4 mS, giving only 0.8 pS per dot when only one dot is written at a time.
3.4 Switching Considerations.

3.4.1 Switch Timing

For reasons of economy, it is proposed that the 1320 recording heads (132 characters x 10 heads/character) be orientated in a matrix, accessing of individual pairs of heads being by switches inserted in the control lines. With this arrangement it is necessary to incorporate a diode in series with each head to prevent sneak paths.

Of the switches in the control lines, some must be used for data injection which feed a number of groups of heads, and these will be called data switches. The remaining switches which determine the group of heads being selected will be called group selector switches.

Since there is only 0.8 μS available to record a dot (that is, to energise a pair of heads), the available time for turn-on and turn-off of the switches is limited. If however more than one dot is written at a time, the available turn-on and turn-off time for the switches is increased. However, as the number of dots written simultaneously increase, so does the current rating of the group selector switches.

The corresponding times and currents for 1, 2, 3, 5 and 9 deliveries (that is, 9, 5, 3, 2, 1 simultaneous energisations) based on a 500 nS dwell time, are as follows:-
<table>
<thead>
<tr>
<th>No. of Deliveries</th>
<th>Time Available per delivery (μS)</th>
<th>Turn-on plus Turn-off (μS)</th>
<th>Current (amps)</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>0.8</td>
<td>0.3</td>
<td>2</td>
</tr>
<tr>
<td>5</td>
<td>1.45</td>
<td>0.95</td>
<td>3</td>
</tr>
<tr>
<td>3</td>
<td>2.4</td>
<td>1.9</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>3.6</td>
<td>3.1</td>
<td>6</td>
</tr>
<tr>
<td>1</td>
<td>7.2</td>
<td>6.7</td>
<td>10</td>
</tr>
</tbody>
</table>

Now in order to operate correctly it is necessary to satisfy the following conditions:

a) After the current in a pair of adjacent heads has reached its maximum value, the duration of that current is sufficiently long so as to magnetise the drum satisfactorily.

b) (i) The group selector switches must be suitably rated to pass the sum of all the currents flowing concurrently in the heads in that group.

   (ii) The pairs of heads being stimulated at any one time, must be sufficiently remote from one another so as not to introduce cross-talk effects.

c) Whenever the group selection path is broken it is necessary to ensure that:

   (i) Before the (n + 1)th group of information is fed to the data switches, the n'th group selection path is broken.
(ii) Before the \((n + 1)\)th group selection path is set up the \(n\)'th group data switches have been turned off.

The result of (a) not being satisfied will be reduced recording density. Violation of (b) (i) may cause reduced life and eventual failure of the group selector switches. For (b) (ii) the cross talk effect will manifest itself as additional dots. This can be seen by considering the effect of writing dot 1 and dot 3 in any character simultaneously. To write dot 1, heads 1 and 2 must be energised. To write dot 3, heads 3 and 4 must be energised. Therefore when dots 1 and 3 are written, dot 2 must automatically be written, since heads 2 and 3 are energised simultaneously. This condition is erroneous and must therefore be avoided.

Conditions (c) not being satisfied will also result in additional dots.

Various ways of ensuring that the required conditions are not violated will be briefly discussed.

3.4.2 Arrangement of Timing

By arranging the timing as shown in Figure 3, which say represents the data switches, switch 2 turn-on is delayed from switch 1 turn-off by an amount dependent on \(T\). In order to achieve this a multiphase clock may be necessary.

3.4.3 Arrangement of Logic

By grouping the heads in two electrically isolated matrices, and arranging the logic such that when one matrix
is operating, the other is relaxing, the time available for
turn-on and turn-off is considerably increased. Similarly
the heads may be arranged in more than two groups with further
increase in relaxation time. The disadvantages of such an
arrangement are:

(a) More address switches are required for any given
number of heads. If it is assumed that each matrix
or sub-matrix is arranged in a square array the
number of switches required is minimised. Thus
if \( N \) heads are to be addressed in a single array,
the optimum dimensions are a \( \sqrt{n} \) by \( \sqrt{n} \) matrix
giving a total of \( 2\sqrt{n} \) switches. If these \( N \) heads
are now divided into 'x' groups each with \( \frac{n}{x} \) heads,
the optimum choice of dimensions of these sub-
matrices must be \( \frac{\sqrt{n}}{x} \) by \( \frac{\sqrt{n}}{x} \) and the total number
of switches required is \( 2x \frac{\sqrt{n}}{x} \). Thus the number
of switches is increased by:

\[
2x \frac{\sqrt{n}}{x} - 2 \sqrt{n} = (\sqrt{x} - 1) \times 100\%
\]

\[
\frac{2}{\sqrt{n}}
\]

This does not necessarily imply that the cost will increase
by this amount unless it is assumed that all the switches
inserted in both X and Y address lines, cost the same.

For the proposed system, the group selector switches are
likely to cost more than the data switches since they carry
twice as much current. However, whatever the cost differential
between group selector and data switches, the multiple
matrix arrangement will always be more expensive.

(b) Extra buffer stores and logic are required since
the mosaic generator must now be time-division-
multiplexed between the two arrays.

3.4.4 Arrangement of Circuit

To ensure an adequate dwell time for the head current,
the available time for turn-off followed by turn-on is limited,
and to ensure that the transistors operate within this period,
careful worst case design is necessary.

3.5 Group Selection Switch Pattern

There are 132 characters per line, and groups of
characters are selected by means of group selector switches.
In series with these switches, are placed data switches, which
are used to inject the mosaic data.

Table 1 shows the various switch patterns for a single
head matrix.

Table 2 shows the same switch patterns but for two
electrically isolated matrices, as discussed in Section 3.4.3.

The corresponding logic diagrams for Table 1 are shown
in Figure 4 and Figure 5.

3.6 Evolution of the Final Matrix

From Tables 1 and 2 it is clear that the two main head
<table>
<thead>
<tr>
<th>Group Selector Switch Pattern</th>
<th>Position of Data Switches with Respect to heads</th>
<th>Number of Group Switches on non-data side of heads</th>
<th>Number of Switches on Data Side of heads</th>
<th>Total number of Switches Rated for 'n' heads</th>
<th>Rated for 1 head</th>
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<tr>
<td>66 x 2</td>
<td>Adjacent</td>
<td>66</td>
<td>2 20</td>
<td>68 20</td>
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<td>3 30</td>
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<td>28 60</td>
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<td>25 80</td>
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<td>12 x 11</td>
<td>&quot;</td>
<td>12</td>
<td>11 110</td>
<td>23 110</td>
<td></td>
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<tr>
<td>66 x 2</td>
<td>Remote</td>
<td>66</td>
<td>20 10</td>
<td>66 30</td>
<td></td>
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<td>44 x 3</td>
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<td>30 10</td>
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<td>60 10</td>
<td>22 70</td>
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<td>&quot;</td>
<td>17</td>
<td>80 10</td>
<td>17 90</td>
<td></td>
</tr>
<tr>
<td>12 x 11</td>
<td>&quot;</td>
<td>12</td>
<td>110 10</td>
<td>12 120</td>
<td></td>
</tr>
</tbody>
</table>
Table 2. Group selector switch Pattern 2.

<table>
<thead>
<tr>
<th>Group Selector Switch Pattern</th>
<th>Position of Data Switches with respect to head</th>
<th>Number of Group Switches on Non-data side of head</th>
<th>Number of Switches on data side of head</th>
<th>Total Number of Switches</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Group:   2</td>
<td>Data: 20</td>
<td>'n' heads: 70</td>
</tr>
<tr>
<td>33 x 2</td>
<td>Adjacent</td>
<td>33</td>
<td></td>
<td></td>
</tr>
<tr>
<td>22 x 3</td>
<td>&quot;</td>
<td>22</td>
<td>3</td>
<td>30</td>
</tr>
<tr>
<td>17 x 4</td>
<td>&quot;</td>
<td>17</td>
<td>4</td>
<td>40</td>
</tr>
<tr>
<td>11 x 6</td>
<td>&quot;</td>
<td>11</td>
<td>6</td>
<td>60</td>
</tr>
<tr>
<td>33 x 2</td>
<td>Remote</td>
<td>33</td>
<td>20</td>
<td>10</td>
</tr>
<tr>
<td>22 x 3</td>
<td>&quot;</td>
<td>22</td>
<td>30</td>
<td>10</td>
</tr>
<tr>
<td>17 x 4</td>
<td>&quot;</td>
<td>17</td>
<td>40</td>
<td>10</td>
</tr>
<tr>
<td>11 x 6</td>
<td>&quot;</td>
<td>11</td>
<td>60</td>
<td>10</td>
</tr>
</tbody>
</table>
group arrangement is more expensive than the single main head group arrangement. It was therefore proposed that a single main head group arrangement be adopted.

To eliminate the effects of switching transients it was decided to arrange the logic such that one data switch was turned off before the next one was turned on. This meant that under no circumstances would the current in the group selector switches be more than 2A. The reason for this decision and the decision to write only one dot at a time was due to the cost of the group selector switches. At the time the cost of a 4A device was significantly higher than that of a 2A device.

Study of the relative cost of a 2A and 1A switch, including the necessary driver stages revealed a 2:1 ratio.

Using this 2:1 ratio of costs in conjunction with Table 1 the minimum cost was found to occur with a 33 X 4 switch pattern, and the data switches positioned adjacent to the heads.

Now it was shown in Section 3.4.1 that the time available to write a dot is 0.8 μS, and of this, 0.5 μS is required for actual recording, the remaining 0.3 μS being available for turn-on and turn-off of the switching elements. Since in general the turn-off time of a transistor is longer than the turn-on time, due to storage effects, it was decided to allow 0.1 μS for turn-on and 0.2 μS for turn-off. Now to have used transistors with similar switching times at the currents concerned would have proved prohibitively costly,
since, although the matrix had been optimised, 40 dots and 33 group selector switches were still required. In order to permit the use of relatively slow and cheap devices for the data and group selector switches, it was decided to insert in series, high speed switches.

The system is shown in Figure 6 which represents part of the head matrix. The group selector switches are arranged in two groups, each group being returned to the supply via the high speed switches HS1 and HS2. The data switches are also arranged in two groups, DS1-1/10 and DS3-1/10 being fed with one set of data whilst DS2-1/10 and DS4-1/10 is being fed with another. The operation will now be described for the case of a continuous line of dots across the page.

Consider data being fed to groups 1 and 3, this information representing the first row of the first character in the line. Since sequential operation is to be employed, initially only the first two switches in each group will be closed, i.e. DS1-1/2 and DS3-1/2. Also at this time assume that the group selector switch GSS1 is closed. Now if HS1 is closed, current will flow through a pair of heads and record the first dot of the first character. Up to and during this period however, the data switches in groups 2 and 4 and GSS2 are being primed, i.e. base current is allowed to flow, although no collector current passes since HS2 is open.

Now HS1 is opened and HS2 is closed. This diverts the current to another pair of heads and records a dot in the second character. By the end of this second recording, groups 1 and 3, and GSS3 have been primed, such that when HS2 is opened
and HS1 is closed again, current is diverted yet again to another pair of heads in the third character. Now the time between HS1 turning off and then on again represents the time available for GSS1 to turn off. Hence GS1 may be slow compared to HS1. After the first dot in the first four characters has been recorded, the second dots are each recorded in turn in a manner identical to the above. The time between the group selector switches turning off and then on again represents the time available for the data switches to turn off and hence the data switches may be slow relative to the group selector switches.

Next it was decided to study the economics of making the 4 group selector switches high speed elements, and eliminating HS1 and HS2. Results indicated that there was little to choose between 4 slow elements plus 2 high speed elements, and 4 high speed elements. The latter was selected since the logic complexity was reduced.

This technique of introducing high speed switches to permit the use of slower devices for the group selector switches, can also be applied to those group selector switches remote from the data switches. In this case 3 such switches are required, since 33 is not divisible by 2.

Since this system relies on having two sets of data available concurrently, it becomes necessary to staticise the output of the mosaic generator, but as only one dot is written a time, it is only required to store one dot of information for two characters.
Based on the foregoing considerations the resultant matrix is a 4-dimensional array and is shown in Figure 7. The high speed switches HS1-4 control the current flow whilst the data switches DS1/2/3/4/1-10 control the injection of the mosaic code for any block of 4 characters. Selection of any particular block of 4 characters is by the group selector switches GSL-33, with the required speed being provided by the high speed switches HS5-7.

3.7 Summary

A matrix has been evolved based on a criterion of least cost, taking into account the method of recording, speed of operation, and limitations of the switching elements.
In order to satisfy the conditions discussed earlier, it is necessary to design the switching circuits with known transient responses. Other considerations are power dissipation in the switching devices, and the transient response of the complete head matrix.

The following sections examine these and other considerations in detail and discuss the design of the switching elements.

4.1 Transition times of transistors

Much has been written on the subject and is available in the literature. The expressions which will be used here, are the original 'Ebers and Moll' equations.

For the common emitter configuration, they are:

\[
\begin{align*}
  t_r &= \frac{1}{(1 - \alpha N)} \ln \frac{I_b}{I_{b1} - 0.9 \frac{(1 - \alpha N)I_c}{\alpha N}}, \\
  t_s &= \frac{\omega_1 + \omega_3}{\omega_1 \omega_3 (1 - \alpha N)} \ln \frac{I_{b1} - I_{b2}}{I_c (1 - \alpha N) - I_{b2}}, \\
  t_f &= \frac{1}{(1 - \alpha N)\omega_N} \ln \frac{I_c - \frac{\alpha N}{1 - \alpha N}I_{b2}}{0.1 I_c - \frac{\alpha N}{1 - \alpha N}I_{b2}}.
\end{align*}
\]
where

\( t_r \) is the time taken for the collector current to rise from 10 per cent to 90 per cent of its maximum value.

\( t_s \) is the storage time and is measured from the time the forward base drive ceases to the time the collector current starts to fall.

\( t_f \) is the time taken for the collector current to fall from 90 per cent to 10 per cent of its maximum value.

\( \omega_n \) is the normal cutoff frequency

\( \omega_i \) is the inverted cutoff frequency

\( \alpha_n \) is the normal alpha

\( \alpha_i \) is the inverted alpha

\( I_{b_1} \) is the forward base current

\( I_{b_2} \) is the reverse base current

\( I_c \) is the maximum collector current

From the above equations it can be shown that the transition times are related to the cutoff frequency of the device and it is this parameter which was used for device selection.

4.2 Power ratings of switches

So as to design the switches for reliable operation it is essential that the power dissipation of the transistors does not exceed their rating. Now the transistors used in the system will have different power dissipations depending on their current carrying capacity, duty ratio and response times.
A general expression for the power dissipation in a transistor is given below, the full derivation being given in Appendix A2. This expression does not take into account the power dissipated in the base region during transients, and assumes that the thermal time constant of the transistor junctions is large compared with the periodic time of the current.

\[ P = \frac{1}{T_1 + T_2} \left[ A + B + C + D + E \right] \]

where

- \( A = I_{\text{max}} \left( V_{\text{ce(\text{off})}}/6 + V_{\text{ce(sat)}}/3 \right) \cdot t_r \)  
  Rise-time energy

- \( B = I_{\text{max}} \cdot V_{\text{ce(sat)}} (T_1 - t_r + t_s) \)  
  On-time energy

- \( C = I_{\text{max}} \cdot (V_{\text{ce(\text{off})}}/6 + V_{\text{ce(sat)}}/3) \cdot t_f \)  
  Fall-time energy

- \( D = I_{\text{ceo}} \cdot V_{\text{ce(\text{off})}}(T_2 - t_f - t_s) \)  
  Off-time energy

- \( E = I_b \cdot V_{\text{be}} \cdot T_1 \)  
  Base on-time energy

and

- \( T_1 \) is the duration when the forward base current is present
- \( T_2 \) is the duration when the forward base current is absent
- \( V_{\text{ce(\text{off})}} \) is the voltage between collector and emitter in the off condition
- \( V_{\text{ce(sat)}} \) is the saturation voltage between collector and emitter
\[ V_{be} \] is the base-emitter voltage during the on condition

\[ I_{\text{max}} \] is the maximum collector current during the on condition

\[ I_{\text{CEO}} \] is the collector leakage current during the off condition

4.3 Effects of Inductance and Capacitance

With a 0.5 \( \mu \text{H} \) coil inductance and a 30 volt supply and perfect switches the rise time is ideally less than 50 ns. In practice the actual rise time will be greater than this because of:-

(a) Stray inductance and capacitance due to wiring and unselected paths

(b) The response time of the switches

It is very difficult to predict accurately the magnitude of the strays, but it is possible by choice of arrangement, to minimise the stray capacitance. Table 3 shows the loading (i.e. paths to unselected heads and switches) for a single head matrix. Clearly some of these loadings will reduce for a multiple head matrix.

4.4 Head considerations

Table 4 shows the number of wires required to feed the head system when the blocking diodes are mounted at the head, and all interconnections made.

With the blocking diodes remote from the heads, the number of wires required increases to more than 1300.
### Table 3. LOADINGS

<table>
<thead>
<tr>
<th>Group Selector Switch Pattern</th>
<th>Position of Data Switch with Respect to Head</th>
<th>GSS 1 Loading Paths</th>
<th>GSS 2 Loading Paths</th>
<th>Data Switch Loading Paths</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 x 2</td>
<td>Adjacent</td>
<td>10</td>
<td>20</td>
<td>66</td>
</tr>
<tr>
<td>44 x 3</td>
<td>&quot;</td>
<td>10</td>
<td>30</td>
<td>44</td>
</tr>
<tr>
<td>33 x 4</td>
<td>&quot;</td>
<td>10</td>
<td>40</td>
<td>33</td>
</tr>
<tr>
<td>22 x 6</td>
<td>&quot;</td>
<td>10</td>
<td>60</td>
<td>22</td>
</tr>
<tr>
<td>17 x 8</td>
<td>&quot;</td>
<td>10</td>
<td>80</td>
<td>17</td>
</tr>
<tr>
<td>12 x 11</td>
<td>&quot;</td>
<td>10</td>
<td>110</td>
<td>12</td>
</tr>
<tr>
<td>66 x 2</td>
<td>Remote</td>
<td>66</td>
<td>20</td>
<td>2</td>
</tr>
<tr>
<td>44 x 3</td>
<td>&quot;</td>
<td>44</td>
<td>30</td>
<td>3</td>
</tr>
<tr>
<td>33 x 4</td>
<td>&quot;</td>
<td>33</td>
<td>40</td>
<td>4</td>
</tr>
<tr>
<td>22 x 6</td>
<td>&quot;</td>
<td>22</td>
<td>60</td>
<td>6</td>
</tr>
<tr>
<td>17 x 8</td>
<td>&quot;</td>
<td>17</td>
<td>80</td>
<td>8</td>
</tr>
<tr>
<td>12 x 11</td>
<td>&quot;</td>
<td>12</td>
<td>110</td>
<td>11</td>
</tr>
</tbody>
</table>
### Table 4. Termination : diodes adjacent to head

<table>
<thead>
<tr>
<th>Group Selector switch pattern</th>
<th>Position of Data switch with respect to head</th>
<th>No. of Wires</th>
</tr>
</thead>
<tbody>
<tr>
<td>66 x 2</td>
<td>Adjacent</td>
<td>86</td>
</tr>
<tr>
<td>33 x 4</td>
<td>&quot;</td>
<td>73</td>
</tr>
<tr>
<td>22 x 6</td>
<td>&quot;</td>
<td>82</td>
</tr>
<tr>
<td>17 x 8</td>
<td>&quot;</td>
<td>97</td>
</tr>
<tr>
<td>12 x 11</td>
<td>&quot;</td>
<td>122</td>
</tr>
<tr>
<td>66 x 2</td>
<td>Remote</td>
<td>86</td>
</tr>
<tr>
<td>33 x 4</td>
<td>&quot;</td>
<td>73</td>
</tr>
<tr>
<td>22 x 6</td>
<td>&quot;</td>
<td>82</td>
</tr>
<tr>
<td>17 x 8</td>
<td>&quot;</td>
<td>97</td>
</tr>
<tr>
<td>12 x 11</td>
<td>&quot;</td>
<td>122</td>
</tr>
</tbody>
</table>
Clearly from a manufacturing point of view it is preferable to mount the diodes at the head. For the 33 x 4 switch pattern, only 73 wires from the head system are required.

By manufacturing the heads in modules, with say 80 heads per module, replacement is cheaper and easier in the event of failure.

It is desirable to protect the heads from high currents for long durations due to logic or transistor failure. This can be achieved by capacitively or inductively coupling the drive to the output transistors. This will not protect against failure in the output devices themselves, but this may be remedied by pulsing the supply to the heads. Rather than introduce a high-speed transformer coupled pulse generator it appeared economic to make the high speed switches capable of delivering the required pulse. Since these would be operating with approximately a 25 per cent duty cycle, the individual power dissipation would be less than that of a single element. Figure 8 shows the four-dimensional matrix with the mechanical switches replaced by their transistor counterparts. The high speed switches HS1-4 are now replaced by pulse generators PG1-4 which provide the source of EHT. The return to the high speed pulse generators is connected to the high speed transistors to close the loop, which is now completely dc isolated from any other point in the system.
4.5 Design of the switching elements

4.5.1 Choice of transistors

The primary requirements for the output devices are:

(a) Suitable current rating
(b) Usable gain at the currents concerned
(c) Fast switching times
(d) Low cost

After reviewing the market, the following transistors were selected:

- Data switch: BFY51
- Group selector switch: 2N5190
- High speed switch: BFX34

4.5.2 Maximum permissible switching times

The dot writing periods are fixed by the high speed elements. It was stated in section 3.6 that 0.1 μS would be allowed for turn-on and 0.2 μS for turn-off. These periods must therefore be the maximum transition times of the high speed switches.

The data switches are arranged in groups 1 and 3, and 2 and 4. This selection allows a full dot writing period for the data switches to turn on and turn off. These must therefore turn on and turn off in 0.8 μS.

Now there are three high speed switches associated with the 33 group selector switches, each of which is turned on for 36 dot writing periods and off for 72 dot writing periods. The group selector switches must therefore
turn on and turn off within 72 dot writing periods or 57.6 µs.

4.5.3 Pulse generators PG1 to PG4

A single stage pulse generator is shown in Figure 9. Current drive from a logic output is fed to the base of T₁. The transistors T₁ – T₄ constitute an active pull-up, active pull-down totem pole drive for the output transistor T₅. The differentiating network CR performs two functions. They are:

(a) To introduce a decay in the base drive in order to eliminate storage effects and speed up the turn-off time by reversal of the base current in the transistor T₅.

(b) Protection of the output transistor should the logic fail.

The diode D is to prevent back feed of the 30 volts to the logic should T₁ break down.

No clamping diode is used between the collector of T₅ and Vcc since this increases the turn-off time. The transistor has been selected with a suitable Vce rating to accommodate the positive excursion of the collector voltage due to the stored energy in the transformer.

A multiple stage output pulse generator was designed to see if any economy could be made by replacing the expensive high speed high current device with a number of high speed lower current devices operating in
parallel. In this configuration it is necessary to introduce resistance in series with each transistor to prevent current hogging. The analysis of parallel connected transistors is given in Appendix A3.

Results indicated little cost saving and it was therefore not adopted.

4.5.4 Data switch

The circuit configuration is shown in Figure 10. The two diodes D₁ and D₂ are for input and output protection respectively. The transistor T₃ and the resistor R represent part of the matrix. The current drive to the base of T₃ is allowed to decay in order to speed up the turn-off.

Since two data switches are operated simultaneously to write a dot, it is necessary to introduce resistance in series with each data switch in order that current hogging can be minimised. This is the function of the current defining resistor R.

4.5.5 Group selector switch

This is essentially the same as the data switch except for the output transistor which is rated for 2 amperes. The circuit configuration is shown in Figure 11.

4.5.6 High speed switch (US5, 6, 7)

This is similar to the data and group selector switches and is shown in Figure 12.
In order to obtain a current pulse of 2A in 100ns a supply voltage of at least 30 volts is required. The use of a 30 volt supply is justified later. This means that 60 watts must be instantaneously dissipated in the resistances in the circuit which limits the current to 2A.

Some resistance is required in series with each data switch, to give an even distribution of current through individual heads, and some source resistance is required in the pulse generators for protection of the output devices. It is desirable to minimise that resistance in the pulse generators since there are only four of these and they operate with a high duty cycle resulting in large power dissipations, which may cause a local heat hazard. Therefore it was decided to confine the main bulk of the power dissipation to the 40 data switch resistors, thus giving a more even distribution of heat throughout the machine.

The maximum collector current rating of the BFX34 used in the high speed pulse generators is 5A. Therefore the series resistance required is 6 ohms and the power dissipation is $1^2 \times R \times$ the duty cycle, or 6 watts. This assumes the worst case of a continuous row of dots.

Taking into account the source resistance of the high speed pulse generator, the 3 ohm coil resistance, and the worst case voltage drops across the head diode, the data, group selector, and high speed switches, which are 1.1v,
1.6v, 0.7v and 0.3v respectively, the resistance required in series with each data switch is 12 ohms.

4.6 Transient response of the head matrix

4.6.1 Degree of crosstalk

The dimensions of the matrix have been decided, and the circuit constants fixed by the design of the switches. Now when a particular head is selected, a dc route is set up via the switches. In addition to this dc path there are many ac paths, and it is these which are being considered. As these paths include unselected heads, the transient current flowing may be sufficiently large both in magnitude and duration, to cause erroneous printing.

The 33 x 4 group pattern will be used for the analysis as shown in Figure 8. Each transistor will be assumed to have a capacitance of 12 pF. This figure was taken from the manufacturer's data for the devices used.

4.6.1.1 Assumptions

(a) The saturation resistance of the group selector switches and data switches is small compared with other resistances in the circuit.

(b) Transistors turn on immediately with no delay.

(c) The effect of coil and wiring self-inductance is neglected since this would
tend to delay the current rise and reduce the crosstalk effect.

(d) The effect of coil and wiring mutual inductance is considered negligible compared with the effects of transistor capacitances.

(e) Wiring capacitance will be neglected.

4.6.1.2 Analysis

Since current will only flow when the high speed pulse generators operate, the worst case conditions exist when all the data switches are open. It is assumed that the group selector and the high speed pulse generator associated with the particular group of data switches are already turned on. The equivalent circuit is shown below.

If \( R_1 \) represents the source resistance of the pulse generator, \( R_2 \) the resistance in series with each data switch, then the transient current \( i \) which flows through an unselected head is given by
\[ i = \frac{I_{\text{max}}}{10} \cdot e^{-\frac{t}{T}} \]

where \( R = R_1 + \frac{R_2}{10} \)

\[ I_{\text{max}} = \frac{V}{R} \]

\[ T = 10 \cdot CR \]

It has been reported by STL that in order to magnetise the drum sufficiently to cause background, a minimum current of 0.1A for 20 nS is required.

For \( C = 12 \text{ pF} \)
- \( R_1 = 6 \text{ ohms} \)
- \( R_2 = 12 \text{ ohms} \)
- \( R = 7.2 \text{ ohms} \)
- \( I_{\text{max}} = 4.16 \text{ amps} \)

Then \( T = \frac{0.9}{0} \text{ nS} \)

From the limited knowledge of the relationship between the background and the current amplitude and duration, it is not possible to assess whether or not there is a hazard.

This will be established experimentally.

4.6.2 Duration of current

In the previous section, the effect of inductance was ignored for crosstalk calculations. When a dot is written however, the inductance and resistance in the circuit will tend to reduce the growth rate of the current, which in turn
will affect the dwell time and the recording density. It is therefore necessary to estimate the maximum lead length required between the head address switches and the head modules in order to calculate the total circuit inductance, and hence the supply voltage required.

The inductance of a pair of parallel wires is given by

\[ L = 0.16 + 1.5 \log_{10} \frac{C}{a} \text{ mH per mile} \]

where \( a \) is the effective diameter of the wire
\( C \) is the spacing between wires

For the 7/0076 wire to be used at an estimated average spacing in a cable form of 0.5 inches, the inductance is approximately 1 \( \mu \text{H} \) per foot.

Since two heads are energised for each dot, one single wire will carry 2A whilst two other wires will carry only 1A. The equivalent circuit for inductance only is shown below

\[ L = 1 + \frac{1 + L_c}{2} \]

where \( L \) is the effective inductance as seen by the high speed pulse generators
\( L_c \) is the coil inductance
\( l \) is the inductance of the leads
For a maximum lead length of 17 inches based on the machine geometry, the corresponding value of $l$ is $0.7 \, \mu H$.

and for $l = 0.7 \, \mu H$

$L_0 = 0.5 \, \mu H$

$L = 1.3 \, \mu H$

Assuming there is no resistance in the circuit, the current would rise at $E/L$ amps/sec and for a current rise of 2A in 0.1 $\mu S$, the voltage required is 26 volts.

Resistance is however required in the circuit in order to limit the steady state current to a safe value, and also to ensure an even distribution of current in the pair of heads being simulated. The effect of this added resistance would be to back off the available voltage as the current rises, and thereby extend the rise time.

Increase of the supply voltage would compensate for the loss but would require a voltage of at least 100 volts to increase the current to within 5 per cent of its final value in the time allowed. In addition, more power would have to be dissipated in the series resistors and the size of the power supply would correspondingly increase. Therefore it was decided to increase the supply voltage to 30 volts only and capacitively by-pass the resistances in the circuit in order to maintain the driving voltage approximately constant during the 100 $\mu S$ turn on period.

This choice of voltage is based on power supply considerations (size, weight and cost), thermal considerations due to dissipation in the resistors and transistor considerations
In order to analyse the circuit so as to compute the optimum values of capacitance required, certain assumptions will be made.

4.6.2.1 Assumptions

(a) The saturation resistance of the switch-elements are small compared with the passive resistances in the circuit.

(b) The saturation voltages of the switching elements are small compared with the supply voltage.

(c) Transistors turn on immediately without delay.

(d) Stray capacitance effects are neglected.

(e) Mutual inductive effects are neglected.

(f) The pulse generator develops a perfect step function.

4.6.2.2 Equivalent circuit

The basic configuration based on the above assumptions is shown below.
where 

- $R_1$ is the source resistance of the pulse generators.
- $C_1$ is the source capacitance of the pulse generators.
- $R_2$ is the resistance in series with a data switch.
- $C_2$ is the shunt capacitance across $R$.
- $L_1$ is the effective individual loop inductance.

As the two parallel networks are identical, the complete network reduces to that shown below:

where $R = R_2/2$, $C = 2C_2$, and $L = L_1/2$.

It is required to choose values of $C$ and $C_1$ such that when a voltage step is applied, the current reaches 2A in 0.1 μS. If the capacitor $C$ is too large the effect of the
current limiting resistors \( R_2 \) during the dwell period may be lost. Since it is likely that there are numerous pairs of values of \( C \) and \( C_1 \) which will satisfy this condition, we will make the impedance of the series RC network much smaller than the impedance of the shunt RC network. The justification for this decision is threefold.

Firstly, by making \( C_1 \) large, \( C \) must be small in comparison, since in the design the resistors \( R_1 \) and \( R \) are of equal value. Now there are 40 capacitors represented by \( C \) (for the 4 groups of 10 switches) and only 4 represented by \( C_1 \). Therefore it is desirable to make \( C \) physically smaller than \( C_1 \) and hence improve the component packing density on the boards.

Secondly, it is desirable to keep the impedance of the network in series with each coil as high as possible, in order to give an even distribution of current throughout adjacent heads.

Thirdly, by making the time constant of \( R_1 \) and \( C_1 \) much greater than 0.1 \( \mu \)S, the effect of these components may be neglected for the period we are concerned with. This greatly simplifies the analysis and results in the equivalent circuit shown below.
4.6.2.3 Analysis

With zero initial conditions the time domain response is given by

\[ i(t) = I_1 - I_2 e^{-bt} + I_3 e^{-ct} \]

where \( I_1 = \frac{V}{R} \)

\[ I_2 = \frac{V}{L} \cdot \frac{a - b}{b(c - b)} \]

\[ I_3 = \frac{V}{L} \cdot \frac{a - c}{c(c - b)} \]

and \( a = \frac{1}{CR} \)

\[ b = \frac{1}{2CR} - \frac{1}{2} \sqrt{\frac{1}{2} \frac{R^2}{C^2} - \frac{4}{LC}} \]

\[ c = \frac{1}{2CR} + \frac{1}{2} \sqrt{\frac{1}{2} \frac{R^2}{C^2} - \frac{4}{LC}} \]

The full derivations of these equations are given in Appendix A4.

From the equations it can be shown that at \( t = 0 \),
\( i = 0 \) and when \( t = i = V/R \). Whether or not the current transient is oscillatory depends on the relative values of \( C, L \) and \( R \). The critical damping conditions is when

\[
\frac{1}{C} \frac{R^2}{2} = \frac{1}{C} \frac{L}{C} \quad \text{or} \quad C = \frac{L}{4R^2}.
\]

For \( L = 1.3 \, \text{pH} \) and \( R = 6 \, \text{ohms} \), \( C \) is 9,000 pF.

As \( V, L \) and \( R \) are fixed, we must examine the value of the current at \( t = 0.1 \, \mu\text{s} \) as \( C \) is varied. The resultant curve is shown in Figure 13 and from it a value of about 6000 pF appears to be the optimum. As this is less than the calculated value of 9000 pF for critical damping, the current transient will be non-oscillatory as long as the applied voltage to the network remains constant. Since however the applied voltage remains approximately constant over the first 100 ns only, by the choice of \( R_1 \) and \( C_1 \), it follows that at some time after \( t = 100 \, \text{ns} \), the current will reach a maximum value, and thereafter reduce towards the steady-state value of \( 2A \).

The corresponding value for \( C_2 \) is 3000 pF, and the nearest preferred value of 3300 pF will be used.

4.7 Summary

The switching circuits have been designed taking into account

(a) The transition times of the devices used

(b) The maximum power dissipation of the devices

(c) The effects of inductance and capacitance.

(d) The protection of the heads.
A transient analysis of the head matrix has been presented and the optimum value of capacitance across the current limiting resistors found in order to minimise the total power dissipation.
The following sections describe the operation of the overall system logic as used in the demonstration model, and the individual logic blocks as shown in Figure 14. The message store is an internal programmer to replace the action store which at the time was not available.

Operation of the system will be described with reference to Figure 15 (logic diagram), Figure 16 (timing diagram) and Figure 8 (head matrix).

5.1 Modus operandi

Clock pulses present at A have a periodic time of 0.8 $\mu$S and a duration of 0.2 $\mu$S. These are first fed to a modulo 36 counter, the outputs of which are decoded to provide the timing pulses $t_1$ to $t_{18}$, $PG_1$ to $PG_4$ (Figure 15). At time $t = 0$ stores $S_1$ and $S_2$ (Figure 15) contain the first track of the first two characters. Between $t = 0$ and $t = 0.6$ $PG_1$ closes and records track 1 of the first character, $DS_{1/2}$ having previously been primed. Between $t = 0.6$ and $t = 0.8$ $PG_1$ turns off. From $t = 0.8$ to $t = 1.6$ $PG_2$ turns on and records track 1 of the second character. Also during this period the information in $S_1$ is changed to track 1 of the third character, under the control of the timing signal $t_1$ and $X$. From $t = 1.6$ to $t = 2.4$ the first track of the third character is recorded, since $PG_3$ operates, and the information in $S_2$ is changed to track 1 of the fourth character.
During the period $t = 2.4$ to $t = 3.2$ track 1 of the fourth character is recorded by the operation of PG4, and the information in S1 is changed to the second track of the first character. Thus track 1 of the first four characters has been recorded under the control of the timing signals $t_1$ and $t_2$. Next, track 2 of these four characters is recorded under the control of $t_3$ and $t_4$, and PG1 to PG4. This process is repeated until all the tracks of the first four characters have been recorded, and is indicated by pulse 1 at $t = 28.8$. This pulse feeds a modulo 33 counter, the outputs of which are decoded to provide the timing pulses GSS1 to GSS33, HS5 and HS6.

From $t = 0$ to $t = 28.8$ GSS1 and HS5 were closed thus selecting the first four characters in the line. Now in the last 0.2μS of this period when PG4 turns off, HS5 also turns off. At $t = 28.8$ when PG1 turns on, HS6 also turns on (GSS2 has already been primed during the period $t = 0$ to $t = 28.8$) thus allowing the first track of the fifth character to be recorded. During the period from $t = 28.8$ to $t = 57.6$ when the second block of four characters is being recorded GSS1 turns off. GSS3 turns on in readiness for the change-over of HS5 and HS6 at $t = 57.6$ when the third block of characters will be recorded. Thus after 0.9548 ms all the top mosaic rows of all the characters have been recorded on the drum and correspond to GSS33 turning off. As the drum rotates this process must be repeated for the remaining 14 mosaic rows with the mosaic generator giving an output corresponding to the mosaic row being recorded. This is
achieved by the 15 way counter which is fed from the modulo 33 output and decoded to provide the dot row address to the mosaic generator. It will be noticed that the output of the mosaic generator is changing every 0.8 μS and provides 9 dots simultaneously. However, only the dot required is stored in S1 and S2 under the control of the timing signals t1, ..., t17, and X and Y.

Only two high speed switches HS5 and HS6 are employed to commutate the group selectors, instead of the three proposed earlier. This is because the actual drum used in the model was an 80 character version and not 132. Therefore it was only necessary to address 80 character positions, that is, GSS1 to GSS20. Since this is an even number, only two high speed switches were necessary although the third one would be required to print out the full 132 characters.

However, so as to simulate accurately the full speed capability at 132 characters the 33 way counter was not allowed to be reset at 20. Thus although between positions 20 and 33 on the 33 way counter no recording is actually taking place, these time slots simulate the addressing of the non-existent heads.

5.1.1 Control/Counters

The main control and counter logic is shown in detail in Figure 17. Closure of the switch S1 starts the cycle by setting over the R-S flip-flop FF1. The differentiating network is to allow FF1 to be reset after 8 mS since operation
of a mechanical contact for a period less than this is both complicated and unreliable. In a full system, S1 would be replaced by a logic gate indicating the reception of an end-of-line signal, and the differentiator would be redundant.

When FF1 is set one of the clutch magnets X or Y is energised depending on whether reed-switch P or Q is closed. Figure 18 shows the clutch control arrangement and it can be seen that there are two attitudes A and B giving two cycles in one revolution. When either of the clutch magnets operates the appropriate detent is moved, and releases the drum.

There are three phases of the drum displacement per cycle, the first and last being periods of acceleration and deceleration lasting about 8 ms. The second phase is one of constant velocity lasting about 14 ms, during which the recording is done. This nonlinear drum displacement was achieved with a Geneva mechanism. Since the start of the period of constant velocity is fixed purely by the mechanism geometry and is independent of the actual speed, it was found convenient to detect the start of the recording phase by two additional reed-switches R and S.

When either of these switches operate, FF1 is reset and the second R-S flip-flop FF2 is set over, allowing clock pulses to be applied to the first counter chain. This is a modulo 36 counter which may be considered as a 4 x 9 counter,
since throughout the period of count, 9 dots of 4 characters are written. It can be seen that a synchronous design has been used. This was to minimise the propagation delay such that after decoding, unwanted spikes would not be present.

When the counter is reset to zero a pulse appears at the output of the multi-input NAND gate N1, and this is fed via an inverter to a modulo 33 counter. Since there are 33 groups of four characters, this counter identifies which group of four characters is being addressed. The use of a ripple-through counter for this and subsequent counter was found acceptable because of their long periodic times.

The output of this counter is used to trigger the 15 way counter whose function is to address the mosaic generator such that the required mosaic row is emitted.

Finally there is a modulo 3 counter (synchronous for simplicity only), to identify which line is being written. This would not normally be required, but for the model described it was decided to generate a message internally composed of three lines of text.

After one line of text has been written, as indicated by a complete cycle of the 15 way counter, a line complete signal is fed back to reset FF2. S1 must now be depressed again in order to write another line of text. However there is an override facility in the clutch control amplifier to give a continuous run-out at 30 lines per second.
5.1.2 Clock

The system clock is derived from a free-running 5MHz clock as shown in Figure 19. Operation is by continuous charging of C through R and discharging through TR1. The threshold voltage to which C charges in order to change the state of the long-tailed pair is fixed by R1 and R2. When this threshold is reached C begins to discharge since TR1 and TR2 are now conducting. As soon as the voltage on C drops below that of the threshold TR1 and TR2 try to turn off. However because of the stored charges in their bases, sufficient time exists to allow the capacitor to be nearly discharged to zero. After TR1 and TR2 turn off, the cycle repeats.

If it is assumed that the saturation voltage of TR1 is zero, then the duration of charge is given by CR ln \( \frac{V}{V - v} \), where V is the supply voltage and v is the instantaneous voltage. Now, at the instant of switching

\[
V = V_0 R_2 / (R_1 + R_2),
\]

hence

\[
t = CR \ln \frac{1}{1 - k}
\]

where \( k = R_2 / (R_1 + R_2) \).

This therefore is independent of the supply voltage V. In practice the periodic time is not completely independent of V since the saturation voltage of TR1 is finite. However, good stability was achieved and a change of 10 per cent of supply voltage varied the frequency by only 0.5 per cent.
5.1.3 Decoding logic

The decoding of the states of the modulo 36 counter to provide the timing signals \( t_1, t_2, \ldots, t_{18}, t_{19} \) to \( t_{34} \), \( X, Y \), is shown in Figure 20 and the address to the mosaic generator plus message store in Figure 21. Timing signals for 20 of the 33 group selectors and the high speed switches are generated as shown in Figure 22.

The Boolean expressions for these signals, as derived from the timing diagram, are given in Appendix A5. Also shown are their minimisations in the form of sums of products, this resulting in approximately 50 per cent reduction in gates. The logic was implemented using nand logic elements.

5.1.4 Message store

This is shown in Figure 23 and its function is to generate a message so as to simulate an action store. The mosaic generator used in the system had a repertoire of 8 characters and there were chosen to be I, T, C, D, R, E, F and 0, with an additional redundant line for space. From this limited repertoire the words ITT, CREED and FERRODOT can be formed, and it was decided to print each of these words in three separate lines. The actual format adopted is shown below.

```
ITT  ITT  ITT  ITT  ..................  ITT
CREED CREED CREED CREED  ..................  CREED
FERRODOT FERRODOT FERRODOT FERRODOT  ..................  FERRODOT
```
Now it was stated earlier that the sequence of dot writing must be the first dot of the first character followed by the first dot of the second character and so on until the first dot of the fourth character which is then followed by the second dot of the first character. This means that the output address lines to the mosaic generator are stimulated sequentially at the dot writing rate. This is achieved by the FG1 to FG4 timing signals which feed the selection gates. Hence, when line 'a' is at '1' with all the other address lines at a '0' the output sequence is I,T,T, space, I,T,T, space, and so on. With 'b' at a '1' the 'space' line is continuously pulsed corresponding to the last four characters in a field width of 8.

When 'c' is at a '1' the sequence is C,R,E,E,C,R,E,E, and with 'd' at a '1' it is D, space,space,space,D,space, space,space.

Stimuli on the 'e' and 'f' address lines give sequential outputs corresponding to the first and last four characters in the word FERRODOT.

It is apparent that the input address lines a,b,c,...,f, are clearly functions of J and J which correspond to the block of four characters being written and T and U which correspond to the line being written.

It can also be observed that the message store emits its information one clock pulse in advance of the actual dot writing periods i.e. when 'C' in GREED is actually being
recorded, the 'R' output of the message store is being stimulated. This is because the slow data switches in the head address system are required to be turned on prematurely, recording being actuated by the pulse generators PG1 to PG4.

5.1.5 Mosaic Generator

Figure 24 gives the circuit configuration for the diode matrix type generator used in the machine. It has 9 character address lines, 15 mosaic row address lines, and 9 output lines. Stimulus of a character line results in a current flow through the diode shown ringed. These correspond to the dot locations within that character. However not all of this current reaches the bases of the sense transistors Q1 to Q9, as only one mosaic row is being addressed. The other 14 address lines act as current sinks via the diodes shown crossed. Hence only current representing dots in the particular mosaic row being addressed ever reaches the sense amplifier. The nine groups of 15 diodes at the crossed intersections prevent current sourcing from the logic. The nine groups of 15 diodes associated with each base is to prevent back feed along to the other inputs.

When a particular character address line is stimulated a current is routed through to the appropriate sense transistors. The turn on time of these amplifiers depend on the available current drive and the response of the transistor. With the devices used an access time of 100 nS was easily obtainable. When the input stimulus is removed there is nowhere for the stored charge in the base to leak away to,
since the input diodes block any reverse base current. This resulted in a long storage time (approximately 500 nS). Inclusion of an emitter-base resistor reduced this storage time but increased the turn-on time since some of the available drive was needed to drive current into the resistor. Finally it was decided to include an additional transistor with each sense amplifier connected between base and ground. These transistors were arranged to be off during the access period so that the full drive capability was available to the sense amplifiers. During the 200 nS dead space between the stimuli on the character lines, the additional transistors turn on, thus effecting a rapid dispersal of the base charge. With this arrangement the turn on and turn off times were found to be within 100 nS.

The diode type mosaic generator used in the machine has a repertoire of 8 characters and used over 500 diodes.

5.1.6 Staticiser and Multiplexer

This was fully described in section 5.1 and is shown in Figure 15.

5.2 Summary

The system of operation has been described in which the action store, operating in a read/write mode, is replaced by a message store operating in the Write mode only. It generates a repetitive message based on an internal programme and the limited character repertoire of the mosaic generator used,
but serves to demonstrate the maximum speed capability.

The counter chain, clock and decoding logic which controls the system have been fully described.
CHAPTER 6

RESULTS.

The following sections expose the physical reality of the work described in the preceding chapters, and examine both experimental and theoretical results including a print specimen.

6.1 Physical realisation

The system was implemented with diode-transistor logic (DTL) integrated circuits (930 series), since they were readily available within the establishment and their speed capability was adequate.

Standard printed circuit boards were used to accommodate both the integrated circuits and the discrete transistors and components. Interconnections between logic elements were by means of direct wiring.

The layout was arranged to minimise the number of board connections and the 30 volt circuitry was kept physically remote from the 5 volt logic in order that an accidental short between the two should not occur during test or repair. All boards were packaged in a rack.

6.2 Mechanical details

The mechanical unit was positioned on a pedestal as shown in Figure 25 with the electronic package mounted directly beneath. This was to minimise the lead inductance
between the head address switches and the head modules.

Various views of the mechanical unit and electronic packaging are shown in Figures 26 to 35.

6.3 Comparison of experimental and theoretical results

6.3.1 Transient response of switches

All theoretical results were calculated under worst-case conditions, using the equations given in section 4.1 in order to ensure correct operation. The experimental results show only typical responses.

Figure 36 shows the current waveform in a resistive load connected to the transformer output of one of the pulse generators. The delay on the trailing edge does exceed that of the theoretical maximum, and this was due to the delay produced by the transformer, which was neglected during the calculations, and the small amount of stored base charge present.

The delay through the transformer could be reduced by more careful winding of the coils, or an improved material, or both. A ferrite material for use up to 1 MHz was used in the design.

It was intended to design a circuit such that the output transistor just came out of saturation at the instant of turn-off. This however involved the critical choice of selection of differentiating components which was not practical, and therefore it was decided to accept a small
amount of storage time.

Figure 37 shows the typical response of the high speed switches and again some storage effects are present due to the complete impracticability of critically adjusting the transformer turns to reduce the base current to the desired amount at the instant of turn-off. Both high speed switches turned on and off within the specified limits of 100 nS and 200 nS respectively.

The data switch response is shown in Figure 38 and is within the specification.

Figure 39 shows only the experimental result of the group selector switch since a turn-on and turn-off time of 28.8 μS was well within the capability of the device used.

Crosstalk problems were apparent in the cableform, and it was found necessary to separate the high current carrying outputs of the head address system from the low level signal wires.

Inter-winding capacitance of the transformers also affected the transient response of the matrix and resulted in transistors being erroneously turned on for short periods. This was overcome by linking one point of the matrix to the system earth.

An analytical treatment of this phenomenon was not possible, because of the complex nature of the stray paths.
Measurement of the head currents at the module showed that for a dipole pair, a minimum current of 2A for a duration of 0.5 µs was maintained, reaching a maximum value of about 2.5A after 300 ns. This supports the theory developed in Section 4.62. It was assumed that negligible current was lost in the winding capacitance of the head coil. The typical current waveform for a pair of heads is shown in Figure 40.

An example of the print quality obtained with a half mil gap between the drum and the head and a drum stepping rate of 30 lines per second is shown in Figure 41.

Variations in print density are due to individual head module alignment. Additional strokes to certain characters in certain positions are due to shorts within the head module. The absence of dots in some positions is due to heads which have become open circuit during experimentation. No additional dots due to switch capacitances could be detected.

The possible causes of the background residual are as follows:

(a) residual magnetism in the drum due to variations in the erase magnet and the drum surface.

(b) electrostatic charges forming on the powder due to friction between particles during transport in the machine.

(c) surface effects due to drum irregularities.
(d) grease.

Gravitational effects were considered as a cause of unwanted adhesion but were eliminated after computation of the magnitude of the forces of attraction.

It was beyond the scope of the work to establish to what relative extent each of the causes (a) to (d) affected the background level.
7.1 Conclusions

A head addressing system and its associated control logic has been developed for use in a ferrographic printer writing mosaic dots at a rate of 1.2 million per second. The deployment of the switching elements is based on a criterion of least cost.

This rate of writing dots can be utilised in a whole spectrum of modes. The particular mode realised in the analytical model is the recording of 30 lines of text per second, each line comprises 132 characters each comprising 135 mosaic dots, with the drum advancing in stepwise mode to permit maintenance of line by line synchronism with arriving data. Where the data can be extracted from the source at a rate dictated by the drum, however, the drum may advance at constant speed and the average speed of recording is increased to about 2520 lines per minute.

Characters are based on a 9 x 15 mosaic and print quality has been shown to be acceptable for optical character reading. A print specimen with a qualitative analysis is given.

In respect of the design of the pulse generators and switches, reasonable agreement was obtained between the experimental and theoretical results, and were acceptable for demonstrating the machine operation. The turn-on
and turn-off times of each data switch was found to be dependent on the dot writing pattern. In a production machine it would be desirable to arrange for the data switches to turn on and turn off for a fixed time, assuming a dot is to be written, which is independent of the pattern of preceding or succeeding dots written. This would facilitate easier and more reliable design of the transformer coupled data switches, since the turn-on and-turn off transients are fixed and a wide range of variations in device parameters encountered during production, could be accommodated.

The design of the system was necessarily constrained by the inductance of the heads and the inductance of the leads to them. If different heads of much lower inductance had been available, and the power switches mounted directly on to, or close to, the head modules, a much lower supply voltage could have been tolerated, resulting in lower power supply costs and reduced cross-talk effects.

Similarly, if heads requiring lower currents, but producing the same flux, could be obtained, and even lower supply voltage could be used resulting in further economy, both from the power supply and the head address switches.

Reduction in the number of character mosaics will also result in economy since the time available to write a dot is increased, and slower transistors may be used.

In the design presented it is necessary for the action store and the mosaic generator to operate at 1.2 MHz, and
at the present state of the art would probably utilise metal oxide silicon (MOS) logic elements.

Since these have a maximum operating speed of 1 MHz, it would be desirable to reorganise the system such that these elements operate more slowly and hence increase the reliability of the system.

7.2 Further work

A cost reduction could be made in the group selector switches by replacing the existing transistors with a silicon controlled rectifier (SCR). They have a high enough current gain to translate from logic currents to power currents and since this work was started have become available at sufficiently low cost to render them advantageous.

Writing two dots or more at a time can be exploited in either of two ways. Either the printing speed can be increased in terms of lines per second, or there can be a significant increase in the time available for turn-on and turn-off of the switching elements. In the latter case this would permit either the use of slower switches or the elimination of the high speed switches by the introduction of non-dot writing periods for the change-over of the group selector switches, or both.

This could lead to a reduction in system cost but it must be borne in mind that the current rating of the group selector switches will increase and it is necessary to
examine the trade-off between the group selector and data switches. If the dots written simultaneously are in the same character, but sufficiently remote so as not to cause crosstalk effects, the speed of the action store and mosaic generator is reduced.

In addition, the power dissipation in the head address system is reduced, since for a fixed lead and head inductance, the voltage required for say two dots, is less than half of that required for a single dot, by virtue of the five-fold increase in available time for the current rise and fall.

7.3 System extensions

7.3.1 Multiple copies

Various methods of producing multiple copies have been proposed, and one such method is by successive drum recirculations. The drum which must have a capacity of one page of text is rotated much faster than was previously necessary, in order that channel time is not wasted. Since however the drum may be rotated at a constant velocity for copying, very high peripheral speeds can be obtained. The speed limit for a particular drum geometry is when the centrifugal forces are so great as to allow the powder to depart from the drum.

Owing to the higher drum speed, more dots at a time must be recorded, and the effect on the deployment and operation of the head switches have been studied \(^{22, 23}\).
7.3.2 Vertical skip

There are two methods of vertical skip which may be afforded. One is by successive transmission of new line signals, which is wasteful of channel time. The other is by transmission of a particular code character which is immediately followed by another character whose binary equivalent represents the number of lines to be skipped.

Both methods have been studied and documented. 22, 23.

7.3.3 Horizontal skip

Two proposals for horizontal skipping have been studied. Firstly, it is possible to arrange the head logic to address only those positions where printing is required.

Alternatively, the information can be located in the action store, in the same position as it is required in the line of text. This would entail clocking spaces into the action store until the desired position is reached, then transferring the information contained in the collection store.

This proposal has been studied in more detail and documented. 22

7.3.4 Displays

Replacement of the drum with a flexible magnetic band serves as the basis for a Ferrodot hard copy display. No paper transfer is required and the powder formation on the band is viewed directly.
A proposal for a specific requirement has been recorded.

7.3.5 Facsimile

The Ferrodot printing process lends itself to the display of pictorial information received over a telegraph line.

In a facsimile receiver data would be received from line and accumulated in a collection store. Two bits would represent one dot, thus allowing 4 grades of dot density. These grades could be obtained by variation of the head currents. A continuous row of heads would be required.

7.3.6 Label printing

A study has been made into the possible application of the Ferrodot technique for label printing.

In such printers, a large number of names and addresses are stored in coded form, on magnetic tape. Periodically the contents of the tape must be translated into printed labels suitable for fixing to envelopes for the distribution of literature. Such translators are commonly referred to as label printers, and the results of the study shows that a printing rate of 50,000 labels per hour is possible.

7.3.7 X-Y plotters (incremental)

The Ferrodot printer is ideally suited to presentation of graphical information emitted from a computer. Since the output is in digital form, it can be used directly to
control the head-address system such that the position where a dot is to be written corresponds to the instantaneous value of the Y-coordinate. Additional mechanical hardware would be required for the X-coordinate since the paper is required to be moved incrementally in both directions.

7.3.8 Strip chart recorders

In this application the independent variable is usually time, which results in a paper advance in one direction only and at a constant rate. The input to the recorder will in many cases be in analogue form and this must be digitised in order to control the head address system.

If multi-channels are required the inputs can be time division multiplexed, and the head address system made to operate over an assigned subdivision of the page for each input interrogated.
REFERENCES


A.1 Speed Comparison: Time required to record a dot.

A.1.1 Mechanical

3 ms per dot

A.1.2 Thermal

Hot electrode - 15 ms per dot
Passage of current through paper - 100 µS per dot

A.1.3 Electrochemical

140 µS per dot

A.1.4 Ink Jet

50 µS per dot

A.1.5 Electrostatic

Less than 1 µS per dot

A.1.6 Magnetic (including the Ferrographic process)

Less than 1 µS per dot
A2. Power dissipation in a transistor

\[ P = \frac{1}{T} \int_0^T v_i \, dt \]

Where

\[ A = \int_0^{T_r} \left[ V_{ce}(off) - \frac{V_{ce}(off) - V_{ce(sat)}}{T_r} \right] I_{max} \frac{t}{T_r} \, dt \]

\[ B = \int_0^{T_{tr}} V_{ce(sat)} I_{max} \, dt \]

\[ C = \int_0^{T_f} \left[ V_{ce(sat)} + \frac{V_{ce(off)} - V_{ce(sat)}}{T_r} \right] I_{max} \left(1 - \frac{t}{T_r}\right) \, dt \]

\[ D = \int_0^{T_{tr}} V_{ce(off)} I_{ceo} \, dt \]

\[ E = \int_0^{T_f} V_{be} I_b \, dt \]

Now \( A \) is the rise-time energy

\( B \) is the on-time energy

\( C \) is the fall-time energy

\( D \) is the off-time energy

\( E \) is the base on-time energy

and

\( T \) is the duration when the forward base current is present.
$T_2$ is the duration when the forward base current is absent.

$V_{ce\text{(off)}}$ is the voltage between collector and emitter in the off condition.

$V_{ce\text{(sat)}}$ is the saturation voltage between collector and emitter.

$V_{be}$ is the base-emitter voltage during the ON condition.

$I_{\text{max}}$ is the maximum collector current during the ON condition.

$I_{\text{ceo}}$ is the collector leakage current during the OFF position.

Solving the above equations gives:

\[
A = I_{\text{max}} \left( \frac{V_{ce\text{(off)}}}{6} + \frac{V_{ce\text{(sat)}}}{3} \right) \cdot t_r
\]

\[
B = I_{\text{max}} \cdot V_{ce\text{(sat)}} \left( T_1 - t_r + t_s \right)
\]

\[
C = I_{\text{max}} \left( \frac{V_{ce\text{(off)}}}{6} + \frac{V_{ce\text{(sat)}}}{3} \right) \cdot t_f
\]

\[
D = I_{\text{ceo}} \cdot V_{ce\text{(off)}} \left( T_2 - t_f - t_s \right)
\]

\[
E = I_b \cdot V_{be} \cdot T_1
\]
A3. Parallel operation of transistors

A3.1 Steady-state Analysis

The steady-state equivalent circuit is shown below.

\[
\frac{V_{cc} - V_x}{R} = \frac{V_x - V_1}{R_1} + \frac{V_x - V_2}{R_2} + \frac{V_x - V_3}{R_3} + \ldots + \frac{V_x - V_n}{R_n}
\]

\[
V_x \left[ \frac{1}{R} + \frac{1}{R_1} + \frac{1}{R_2} + \ldots + \frac{1}{R_n} \right] = \frac{V_{cc}}{R} + \frac{V_1}{R_1} + \frac{V_2}{R_2} + \ldots + \frac{V_n}{R_n}
\]

\[
\therefore V_x = \frac{V_{cc}}{R} + \frac{V_1}{R_1} + \frac{V_2}{R_2} + \ldots + \frac{V_n}{R_n}
\]

\[
\frac{1}{R} + \frac{1}{R_1} + \frac{1}{R_2} + \ldots + \frac{1}{R_n}
\]

\[
\therefore I_1 = \frac{V_{cc}}{R} + \frac{V_1}{R_1} + \frac{V_2}{R_2} + \ldots + \frac{V_n}{R_n} - \frac{V_1}{R_1}
\]

\[
= \frac{V_{cc}}{R} + \frac{V_1}{R_1} + \frac{V_2}{R_2} + \ldots + \frac{V_n}{R_n} - \frac{V_1}{R_1} - \frac{V_1}{R_2} - \frac{V_1}{R_1} \ldots - \frac{V_1}{R_n}
\]

\[
= \frac{1}{R} + \frac{R_1}{R} + \frac{R_1}{R_2} + \ldots + \frac{R_1}{R_n}
\]
\[ I_1 = \frac{1}{R} (V_{cc} - V_1) + \frac{1}{R_2} (V_2 - V_1) + \frac{1}{R_3} (V_3 - V_1) + \ldots + \frac{1}{R_n} (V_n - V_1) \]
\[
= \frac{V_{cc}}{R} + \frac{V_1}{R_1} + \frac{V_2}{R_2} + \ldots + \frac{V_n}{R_n} \]
\[
I_2 = \frac{V_2}{R_2} - \frac{V_2}{R_{2}} - \frac{V_2}{R_{3}} - \ldots - \frac{V_2}{R_n} \]
\[
= \frac{1}{R} (V_{cc} - V_2) + \frac{1}{R_1} (V_1 - V_2) + \frac{1}{R_3} (V_3 - V_2) + \ldots + \frac{1}{R_n} (V_n - V_2) \]
\[
I_r = \frac{1}{R} (V_{cc} - V_r) + \sum \frac{V_n - V_r}{R_n} \]
\[
= \frac{R - R}{R} + \sum \frac{R_r}{R_n} \quad (1) \]
For the case when

\[ V_1 = V_2 = V_3 = \ldots = V_n = V \]

\[ R_1 = R_2 = R_3 = \ldots = R_n = R \]

\[ I_r = \frac{V_{cc} - V}{R_s + nR} \quad (2) \]

A3.1.1 Transistor saturation characteristics

Now in order to compute the values of \( I_1 \) and \( I_2 \) for a given set of conditions, it is necessary to study the saturation characteristics of a transistor. The equivalent circuit is shown below.

Although the model is not strictly accurate, the author suggests that it is a reasonable approximation to a transistor in saturation. As justification it is pointed out that with zero collector current, one is still left with an offset voltage as is met in bipolar chopper circuits. To a first order of approximation, this voltage may be regarded as a constant.

From the equivalent circuit the linear equation

\[ V_{ce(sat)} = V + R_{sat} I_c \quad (3) \]

may be deduced. Using this equation, if two values of \( V_{ce(sat)} \)
and $I_c$ are known then $V$ and $R_{sat}$ may be found. However, it is necessary to find the minimum and maximum values of $R_{sat}$ and $V$.

Now in general, data sheets give only typical and maximum values of $V_{ce(sat)}$ for various collector currents. Therefore, it will be assumed that the minimum is as much below the typical as the maximum is above it.

A3.1.2 Optimum choice of $R$

The analysis so far has been based on one group of parallel switches in series with a common resistor $R$. In practice however $R$ will be composed of other groups of parallel switches.

Now the maximum current is 2 A and for a supply voltage of 30 V the equivalent resistance is 15 ohms. Now the number of groups of parallel switches required is 2. However the data switches effectively form a parallel pair since two data switches must be turned on simultaneously to record a dot, and also the resistance of the coil and series diode may not be sufficiently high to reduce current hogging to an acceptable level. Therefore there are 3 groups and each one must have an effective resistance of 5 ohms. Hence considering one group only, the other two groups constitute $R$ which is 10 ohms. Since $R$ is now fixed, we must increase $n'$ and $R_a$ to suit the specified conditions. We are interested in the minimum value of $n'$ acceptable, since further increase in $n'$ will increase the cost unnecessarily. It must be pointed out that a choice of $n'$ satisfying the steady-state conditions
may not necessarily satisfy the transient conditions which will be discussed later.

A3.2 Transient Analysis

In the previous section it has been assumed that steady-state conditions had been reached. However we must now consider the transient conditions. The worst case condition is when one transistor is conducting, all other parallel transistors in that group being non-conducting. The transient equivalent circuit is shown below.

Let $I$ = the required current

$I_m$ = the maximum current rating of the individual transistors

$I_T$ = the transient peak current

$P$ = the number of parallel groups

$n$ = the number of parallel paths in each group

The equivalent resistance $= \frac{V_{cc}}{I}$

Hence the resistance of each group $= \frac{V_{cc}}{I} \cdot \frac{1}{P}$

From which

$$R = \left(\frac{p - 1}{p}\right) \cdot \frac{V_{cc}}{I} \quad \cdots \cdots \quad (6)$$
Now if it is assumed that $V_r \ll V_{cc}$ then

$$R_r = \frac{V_{cc}}{I_p} \quad n \quad \quad \quad (7)$$

Under worst case conditions

$$I_T = \frac{V_{cc}}{R_r + R}$$

Equating $I_T$ and $I_m$ (since the transient peak current must not exceed $I_m$) yields

$$R_r = \frac{V_{cc} - I_m R}{I_m} \quad \quad (8)$$

Equating (7) and (8) yields

$$n = \frac{(V_{cc} - I_m R) I_p}{V_{cc} I_m}$$

Substituting for $R$ (equation 6) gives

$$n = \frac{I \cdot I_p - I_m (p - 1)}{I_m} \quad \quad (9)$$

Transposing (9) yields

$$I_m = \frac{I \cdot I_p}{n + p - 1} \quad \quad (10)$$

For $p = 3$

$I = 2$ A

$n = 2$

then $I_m = 1.5$ A

This represents a 50% overload of current if 1 A devices are used.

Using equation (9) for $I_m = 1$ yields $n = 4$. 
A4. Analysis of head network

Taking Laplace transforms

\[ i(s) = \frac{V(s)(R + \frac{1}{sC})}{sI(R + \frac{1}{sC}) + \frac{R}{sC}} \]

For \( V(s) = \frac{V}{s} \)

\[ i(s) = \frac{V(R + \frac{1}{sC})}{s^2LR + s\frac{L}{C} + \frac{R}{C}} \]

\[ \therefore i(s) = \frac{V(s + a)}{Ls(s + b)(s + c)} \]

where

\[ a = \frac{1}{CR} \]
\[ b = \frac{1}{2CR} - \frac{1}{2}\sqrt{\frac{1}{C^2R^2} - \frac{L}{LC}} \]
\[ c = \frac{1}{2CR} + \frac{1}{2}\sqrt{\frac{1}{C^2R^2} - \frac{L}{LC}} \]

Arranging as partial fractions gives

\[ i(s) = \frac{V}{L} \left[ \frac{a}{bc} + \frac{a - b}{s} + \frac{a - c}{s + b} \right] \]

\[ = \frac{I_1}{s} \frac{I_2}{s + b} + \frac{I_3}{s + c} \]

Where \( I_1 = \frac{V}{R} \)

\[ I_2 = \frac{V}{L} \cdot \frac{a - b}{b(c - b)} \]

\[ I_3 = \frac{V}{L} \cdot \frac{a - c}{c(c - b)} \]

Taking inverse Laplace transforms, the time domain response is given by

\[ i(t) = I_1 - I_2e^{-bt} + I_3e^{-ct} \]
A5. Decoding logic

A5.1 Timing pulses decoding

\[ t_1 = BCDEFG + BCDEFG + BCDEFG + BCDEFG \]
\[ = BDEFG + CDEFG + BCDEFG \]

\[ t_2 = BCDEFG + BCDEFG + BCDEFG + BCDEFG \]
\[ = DEFG \]

\[ t_3 = BCDEFG + BCDEFG + BCDEFG + BCDEFG \]
\[ = BCDEFG + CDEFG + BDEFG \]

\[ t_4 = BCDEFG + BCDEFG + BCDEFG + BCDEFG \]
\[ = DEFG \]

\[ t_5 = BCDEFG + BCDEFG + BCDEFG + BCDEFG \]
\[ = BDEFG + CDEFG + BCDEFG \]

\[ t_6 = BCDEFG + BCDEFG + BCDEFG + BCDEFG \]
\[ = DEFG \]

\[ t_7 = ACDEFG + BCDEFG + BCDEFG + BCDEFG \]
\[ = BDEFG + CDEFG + BCDEFG \]

\[ t_8 = BCDEFG + BCDEFG + BCDEFG + BCDEFG \]
\[ = DEFG \]
<table>
<thead>
<tr>
<th>$t_9$</th>
<th>$BCDEFG + BCDEFG + BCDEFG + BCDEFG$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$BCDEFG + CDEFG + BCDEFG$</td>
</tr>
<tr>
<td>$t_{10}$</td>
<td>$DEFG$</td>
</tr>
<tr>
<td>$t_{11}$</td>
<td>$BCDEFG + BCDEFG + BCDEFG + BCDEFG$</td>
</tr>
<tr>
<td></td>
<td>$BDEFG + CDEFG + BCDEFG$</td>
</tr>
<tr>
<td>$t_{12}$</td>
<td>$DEFG$</td>
</tr>
<tr>
<td>$t_{13}$</td>
<td>$BCDEFG + BCDEFG + BCDEFG + BCDEFG$</td>
</tr>
<tr>
<td></td>
<td>$BDEFG + CDEFG + BCDEFG$</td>
</tr>
<tr>
<td>$t_{14}$</td>
<td>$DEFG$</td>
</tr>
<tr>
<td>$t_{15}$</td>
<td>$BCDEFG + BCDEFG + BCDEFG + BCDEFG$</td>
</tr>
<tr>
<td></td>
<td>$BDEFG + CDEFG + BCDEFG$</td>
</tr>
<tr>
<td>$t_{16}$</td>
<td>$DEFG$</td>
</tr>
<tr>
<td>$t_{17}$</td>
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<tr>
<td></td>
<td>$BDEFG + CDEFG + BCDEFG$</td>
</tr>
<tr>
<td>$t_{18}$</td>
<td>$BCDEFG + BCDEFG + BCDEFG + BCDEFG$</td>
</tr>
<tr>
<td></td>
<td>$BCDEFG + BCDEFG + BCDEFG + BCDEFG$</td>
</tr>
</tbody>
</table>
A5.2 Switch decoding

\[
\begin{align*}
\text{HS 1} &= \text{ABC} \\
\text{HS 2} &= \text{ABC} \\
\text{HS 3} &= \text{ABC} \\
\text{HS 4} &= \text{ABC} \\
X &= \text{AB} \\
Y &= \text{AB} \\
\text{I} &= \text{ABCDEFG} \\
\text{HS 5} &= \text{JI} \\
\text{HS 6} &= \text{JI} \\
\text{GSS 1} &= \text{JKLMNO} + \text{JKLMNO} \\
&= \text{JKLMNO} \\
\text{GSS 2} &= \text{JKLMNO} + \text{JKLMNO} \\
&= \text{JKLMNO} \\
\text{GSS 3} &= \text{JKLMNO} + \text{JKLMNO} \\
\text{GSS 4} &= \text{JKLMNO} + \text{JKLMNO} \\
&= \text{JKLMNO} \\
\text{GSS 5} &= \text{JKLMNO} + \text{JKLMNO} \\
\text{GSS 6} &= \text{JKLMNO} + \text{JKLMNO} = \text{JKLMNO} \\
\text{GSS 7} &= \text{JKLMNO} + \text{JKLMNO} \\
\text{GSS 8} &= \text{JKLMNO} + \text{JKLMNO} = \text{JKLMNO}
\end{align*}
\]
GSS 9 = JKLMNO + JKLMNO
GSS 10 = JKLMNO + JKLMNO = KLMNO
GSS 11 = JKLMNO + JKLMNO
GSS 12 = JKLMNO + JKLMNO = KLMNO
GSS 13 = JKLMNO + JKLMNO
GSS 14 = JKLMNO + JKLMNO = KLMNO
GSS 15 = JKLMNO + JKLMNO
GSS 16 = JKLMNO + JKLMNO = KLMNO
GSS 17 = JKLMNO + JKLMNO
GSS 18 = JKLMNO + JKLMNO = KLMNO
GSS 19 = JKLMNO + JKLMNO
GSS 20 = JKLMNO + JKLMNO = KLMNO
GSS 21 = JKLMNO + JKLMNO
GSS 22 = JKLMNO + JKLMNO = KLMNO
GSS 23 = JKLMNO + JKLMNO
GSS 24 = JKLMNO + JKLMNO = KLMNO
GSS 25 = JKLMNO + JKLMNO
GSS 26 = JKLMNO + JKLMNO = KLMNO
| GSS 27 | JKLMO  +  JKLMO |
|        |                |
| GSS 28 | JKLMO  +  JKLMO = KLMNO |
|        |                |
| GSS 29 | JKLMO  +  JKLMO |
|        |                |
| GSS 30 | JKLMO  +  JKLMO = KLMNO |
|        |                |
| GSS 31 | JKLMO  +  JKLMO |
|        |                |
| GSS 32 | JKLMO  +  JKLMO = KLMNO |
|        |                |
| GSS 33 | JKLMO  +  JKLMO |
FIGURE 3 ARRANGEMENT OF TIMING
FIGURE 4(b) DATA SWITCH ARRANGEMENT

ADJACENT TO HEADS
Figure 5(a) Data Switch Arrangement
Remote from Heads
Figure 6 Switching Arrangement
FIGURE 7 4-DIMENSIONAL HEAD MATRIX
FIGURE 10 DATA SWITCH

YCC

VCC

T3
BFY51

5.6kΩ

2.2kΩ

D2
1N9465

220Ω

T2
1N552

T1
1N552

D1
1N4148
Figure 13: Variation of \( i \) with \( C \)
FIGURE 14: BLOCK DIAGRAM

- Head Address System
- Multiplexer Staticiser
- Mosopic Generator
- Message Store
- Decoders
- Counters
FIGURE 16 TIMING DIAGRAM
Figure 17 Control/Counter
FIGURE 16 DRUM DRIVE
FIGURE 24 MOSAIC GENERATOR

COLUMN OUTPUTS

ROW ADDRESS

CHARACTER ADDRESS

ALL DIODES IN 4148 CONNECTED AS SHOWN
FIGURE 25 COMPLETE MACHINE
FIGURES 26 AND 27 MECHANICAL UNIT
FIGURES 28 AND 29 MECHANICAL UNIT WITH RAISED HOTPLATE
FIGURES 32 AND 33 ELECTRONICS PACKAGE
FIGURES 3A AND 25 HEAD MODULES (MATCH SHOWS SCALE)
FIGURE 36 PULSE GENERATOR

FIGURE 37 HIGH SPEED SWITCH

EXPERIMENTAL
THEORETICAL
Figure 4.0 HEAD CURRENT TRANSIENT RESPONSE