A HYBRID SYSTEM FOR ROOT LOCUS COMPUTING

by

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SUMMARY

The problem of displaying rapidly the root locus of a system has not previously been solved. The computer described in the thesis will display the root locus of a system having up to six poles and four zeroes.

The computer consists of a hybrid combination of analogue and digital circuits. It employs an adaptive strategy to find successive points in the s-plane that satisfy the angle equation defining a branch of the root locus.

The possible errors arising from circuit limitations are analysed, and design compromises to achieve a required performance at the lowest cost are specified.

Some typical plots obtained on a cathode ray oscilloscope are shown. These not only demonstrate the validity of the approach used but also indicate the limitations imposed by the instrument specification.

Possible alternatives to the design are suggested as a result of the changes that have occurred, both in cost and technology, in the integrated circuit field in recent years.
TO MY WIFE

FOR HER SUPPORT

AND ENCOURAGEMENT
ACKNOWLEDGEMENTS

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INTRODUCTION

In control system analysis, and more especially design, it is important to be able to predict the stability of a system from a knowledge of the properties of the system components. Nyquist diagrams, Bode plots and Nichols Chart deal with system sine wave response, but fail to give direct information regarding system response to other forms of input. An alternative method of determining system stability is the root locus method developed by Evans\(^1\) in 1948. This technique has the particular advantage that it gives an indication of the compensation to be applied to a system to achieve an improvement in closed loop performance.

Consider a negative feedback system as shown in Fig 1.1. The equation governing its performance is

\[
W(s) = \frac{\theta_o(s)}{\theta_i(s)} = \frac{KP(s)}{1 + KF(s)} = \frac{KG(s)}{H(s) + KG(s)} \tag{1.1}
\]

It is observed that the zeroes of \(W(s)\) occur at the zeroes of \(V_F(s)\). The poles of \(W(s)\) are given by the roots of the equation:

\[
H(s) + KG(s) = 1 + KF(s) = 0 \tag{1.2}
\]

which is called the characteristic equation.

From equation 1.2 \[\frac{KG(s)}{H(s)} = KF(s) = -1 \tag{1.3}\]

Expressed in polar co-ordinates: \[K|F(s)|/F(s) = 1/(2\pi n + 1)\pi\]

that is, a pole of \(W(s)\) must satisfy the conditions:
Fig 1.1 Negative feedback system block diagram.
\[ K|F(s)| = 1 \]  \hspace{1cm} (1.4)

\[ \arg F(s) = (2n + 1)\pi \]  \hspace{1cm} (1.5)

\[ n = 0,1,2,3 \ldots \ldots \]

As the loop gain \( K \) varies, the roots of equation 1.2 can be plotted as a locus in the complex plane. Root solving is achieved by searching for points in the \( s \)-plane where the net phase angle of \( F(s) \) is an odd multiple of \( \pi \).

From the root locus, the closed loop pole positions can be identified with the transient response modes of the system. The frequency response can be readily obtained by measurement to points in the imaginary axis. The system designer can, with experience, introduce compensating poles and zeroes to reshape the locus to a pattern known to give the desired performance.

Until comparatively recently root loci have been plotted manually, this being both a tedious and time consuming process. Furthermore, given a transfer function it is not easy to sketch a rough shape for the locus unless it is of a type previously known. These factors have tended to limit the use of the root locus method in engineering design.

Several methods of automatic root locus plotting have been proposed or implemented and these are described below. Apart from the one used by the author, the remaining methods have disadvantages either in their principle of operation or in their hardware implementation.

1.1. Methods of automatic root locus computing

1.1.1. Analogue methods
Many methods have been proposed that are based on either the D'Azzo and Hoppis servo loop\(^2\) or Levine's steepest descent technique\(^3\). Both these methods, in the form proposed by their authors, have the disadvantage of excessive hardware requirements.

In the D'Azzo and Hoppis method, a search vector \(\Delta s\) is struck out from the starting pole. From the tip of this vector a phase error is produced that is used to change the heading of the search vector until the servo set point (180°) is reached. \(\Delta s\) increases and with the starting pole as an anchor point the heading is changed again to bring the tip of this new vector into the locus and so on. This method will only plot loci where the distance from the starting pole to the locus is monotonically increasing. It will not plot back-curving loci. Moreover, as \(\Delta s\) increases, the servo loop gain is increasing and the system can become unstable. The method proposed by the authors employed one inverse synchro resolver per pole or zero used. Not mentioned by them was the possibility of time sharing a single inverse resolver.

Additional disadvantages of the method are:

(i) Breakpoints in the locus cannot be detected. Actually this could be achieved by setting the servo set point to an angle slightly different from 180°, say 179°.

(ii) Each branch of the locus must start at one of the open loop poles. Pure time delay loci, therefore, cannot be obtained.

Levine's method of steepest descent yields an error function that is used to correct the angular heading of a search vector until the phase error is zero. To generate his equation for steepest...
descent requires one multiplier and one resolver for each pole and zero. The resolvers generate functions of the form \( r \cos \theta, r^2 \cos 2\theta, r^3 \cos 3\theta \) etc. To time share a single resolver to yield these functions (not suggested by the original author) would be a difficult undertaking.

In Levine's method the coefficients of the open loop polynomials are set up on coefficient potentiometers. This has the disadvantage that one cannot alter readily the position of one open loop pole or zero. When the points in the locus for a particular value of \( K \) (loop gain) are found, the value of \( K \) is updated, i.e. the polynomial coefficient potentiometers require altering. After a point in the locus is found, a new steepest descent search is initiated for the next point, that makes no use of the previous search. The method is therefore slow. Furthermore, it does not detect break points, and cannot plot pure time delay loci.

1.1.2 Digital computer methods

Prior to Williamson, computer program methods available were based either on the direct factorisation of the characteristic equation or on a grid search technique in the s-plane.

A computer program for the factorisation method was first proposed by Doda. A disadvantage of the method is that it does not locate accurately break points in the locus. Break points represent multiple closed loop poles, and there is no known technique for factorising a polynomial having two or more repeated roots. Pure time delay systems have to be represented by approximations which can give rise to erroneous results.
A digital implementation of this method would require storage facility and would be prohibitively expensive. Analogue implementation would call for a large number of multipliers, integrators and potentiometers.

In recent years grid search techniques in the s-plane have been proposed. The first of these by Cook and Cook\(^6\) (1968) tests the magnitude of a phase error function, \(C\), at a large number of equally spaced points in the s-plane. A point is taken as being on the true locus if \(C\) is less than a specified amount and its sign is different from that of its four nearest neighbouring points. The resulting plot gives only a vague indication of the shape of the locus. It is extremely inefficient, plotting only a few per cent of the points tested and requiring a large amount of storage.

Aird and Moseley\(^7\) have used a simpler technique of testing the sign of the phase error at successive points in the s-plane. This method is also inefficient, requires storage and the quality of loci produced are no better than those of Cook and Cook.

Williamson\(^4\) has developed a highly sophisticated digital computer program that can plot loci to a phase accuracy better than 20 seconds of arc. The method detects break points and can be employed for time delay systems. The principle of this method is described in Chapter 2. It forms the basis of the hybrid system, the development of which is the subject of this thesis.

1.1.3 Special purpose computers

The EASIAC\(^8\) marketed in 1960 and costing about £6,000 is, to date, the only commercially available so called "automatic" root
locus plotter. It requires a skilled operator to search for points in the s-plane where the phase error is zero. Reports from users suggest difficulty in operation, especially in high sensitivity regions. Root loci can be difficult for many engineers to interpret, and this instruments adds another burden by plotting the loci on a logarithmic scale.
2.1 Basic method of root locus computation.

Consider an open loop transfer function of the form:

\[ KF(s) = \prod_{i=1}^{n} \frac{n}{(s + z_i)} \cdot \prod_{j=1}^{m} \frac{m}{(s + p_j)} \]  

(2.1)

where \( z_i \) and \( p_j \) are the zeroes and poles respectively of the function.

For physically realisable systems \( m > n \). Any point \( \gamma \) in the locus satisfies equation (1.5) which can be written as:

\[ \sum_{i} \psi z_i - \sum_{j} \psi p_j = (2n + 1)\pi \]  

(2.2)

where \( \psi z_i \) is the angle from the point \( \gamma \) to the zero \( z_i \) and \( \psi p_j \) is the angle from the point \( \gamma \) to the pole \( p_j \).

From equation (1.4) the value of loop gain \( K \) at any point \( \gamma \) is given by:

\[ K = \frac{\prod_{j=1}^{m} \frac{m}{(s + p_j)}}{\prod_{i=1}^{n} \frac{n}{(s + z_i)}} \]  

(2.3)

From now an equation (2.2) will be expressed in the form:

\[ \sum Z - \sum P = (2n + 1)\pi \]  

(2.4)

If the angles are continuously adjusted to lie in the range \( 0^\circ \)
Figure 5: Accessing 6800 Peripherals on the Synchronous bus.

Figure 6: Input Data Hardware Block Diagram.
to $360^\circ$ we have:

$$\Sigma Z - \Sigma P - \pi = 0 \quad (2.5)$$

When this computation is carried out at one of the open loop poles of the system, the contribution this pole would make to the calculation is lost. The computation yields the tangent ($\theta$) to the locus at the pole in question. (See Fig 2.1)

If a trial point $P$, (co-ordinates $X_{i1}, Y_{i1}$), is taken at a distance $\Delta s$ from the pole in the set-off direction $\theta$, then

$$X_{i1} = X_1 + \Delta s \cos \theta$$
$$Y_{i1} = Y_1 + \Delta s \sin \theta$$

Applying equation 2.5 at the trial point, produces the phase error $\psi_1$ at this point, i.e.

$$\Sigma Z - \Sigma P - \pi = \psi \text{ at a trial point.}$$

The heading of $\Delta s$ is now changed from $\theta$ to $\theta + \psi_1$ and a new phase error $\psi_2$ at a second trial point $(X_{i2}, Y_{i2})$ is determined. The heading of $\Delta s$ is again changed to $\theta + \psi_1 + \psi_2$. The process is repeated until the phase error $\psi_r$ at the $r$th trial point $(X_{ir}, Y_{ir})$ is less than a specified amount $\epsilon$.

The point $(X_{ir}, Y_{ir})$ is now taken to be a 'true point' in the locus. The last computed angle $\phi = \theta + \sum_{1}^{r} \psi_i$ (where $r$ is the number of computations performed) is the angle from the starting pole $(X_1, Y_1)$ to the point $(X_{ir}, Y_{ir})$. A new trial point $Q$, is now taken at a distance $\Delta s$ from the 'true' point $(X_{ir}, Y_{ir})$ in the direction $\phi$.

With the point $(X_{ir}, Y_{ir})$ as an anchor point, the procedure outlined above is repeated until the next 'true' point $R$ is found.

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Fig 2.1 Method of root locus computing.
The process is continued until the required portion of the branch of the locus associated with the starting pole \((X,Y)\) has been plotted.

The method described plots the \((180 \pm \epsilon)^\circ\) locus, satisfying an angle condition:

\[
\left| \arg F(s) - \pi \right| = \left| \Sigma Z - \Sigma P - \pi \right| \leq \epsilon
\]  

(2.6)

This procedure, in which the trial point tracks the locus, is similar in behaviour to the guidance system of a beam-rider missile.

2.2. Brief description of the automatic root locus computer

An abbreviated block diagram and a typical pole pattern in the s-plane are shown in Fig. (2.2a) and (2.2b) respectively. Initially the cartesian vector components \((x,y)\) from the starting pole (1) to the pole (2) are derived. These values are applied to an inverse resolver and polar co-ordinates \(R/\theta\) produced. The vector components from the starting pole (1) to the pole (3) (in this case \(0,2y\)) are derived, fed to the inverse resolver and the angle \(\theta_2\) obtained. The angle \(-\theta_1 - \theta_2 - \pi = \theta\) is the angle of the tangent to the locus at the starting pole.

The angle \(\theta\) controls a resolver to which is fed an arbitrary vector magnitude \(A\); hence the resolver yields outputs \(A\cos\theta\) and \(A\sin\theta\). These are added to the co-ordinates of the starting pole to give the first trial point \(P\).

The cartesian vector components from the trial point to the first pole (1) are determined and again by means of the inverse resolver, the angle \(\theta_3\) is computed. This is repeated with the trial point and poles (2) and (3) to yield \(\theta_4\) and \(\theta_5\) respectively. The total angle
Fig 2.2a Basic block diagram of automatic root locus computer.

Fig 2.2b Pole pattern in the s-plane, showing angles to the starting pole and the first trial point.
\( \theta' = -\theta_3 - \theta_4 - \theta_5 \) is equal to \(-\Sigma P\). Subtracting \(\pi\) yields the phase error \(\psi_1\). If \(\psi_1\) is greater than a specified error \(\varepsilon\), it is added to 0 and by means of the resolver a new trial point is found. The procedure is repeated until a point is reached where the phase error is less than \(\varepsilon\). When this occurs the co-ordinates of the current trial point are displayed on the cathode ray oscilloscope as a true point in the locus. The last computed angle is used in conjunction with \(\Delta s\) and controls the resolver circuit to produce a fresh trial point \(Q\), (See Fig. 2.1). With the previous true point as an anchor point the basic procedure is repeated to find the next true point and so on.

It is noted that if cartesian components involving zeroes are applied to the inverse resolver the angles produced are given a positive sign since the algorithm used is \(|\Sigma Z - \Sigma P - \pi| < \varepsilon\).

2.3 Detailed block diagrammatic description

The block diagram of the root locus computer is shown in Fig 2.3. The system described can handle up to six open loop poles and four open loop zeroes, and can be extended.

2.3.1 Cartesian co-ordinate differences generation

The cartesian co-ordinate values of the open loop poles and zeroes are set up as input voltages by means of front panel switches and potentiometers. In the X channel these input voltages are connected by a group of analogue switches \(A_x\) to buffer amplifier \(a_{x2}\), the output of the latter being connected to sample and hold circuit \(S2X\). Analogue switches \(A_x\) are controlled by a six stage shift register \(SRA\). The X channel input voltages are also connected by a further group of analogue switches, \(B_x\), to buffer amplifier \(a_{x1}\) the output
Fig 2.3 Root locus computer block diagram.
of which is inverted in amplifier $a_{x3}$. The output of summing amplifier $a_{x4}$ gives the difference voltage between the outputs of $a_{x3}$ and S2X. Analogue switches Bx are controlled by an eleven stage shift register SRB. The Y channel is similarly connected.

When start is initiated, all stages of both shift registers are set to logical '0', i.e. all analogue switches are open circuit. The first stage of SRA then changes to logical '1', closes the first switch of groups Ax and Ag and allows the first pair of voltages $(X_1^, Y_1^)$ representing cartesian co-ordinates $(X_1^, Y_1^)$ to be sampled and stored in S2X and S2Y. The outputs of S2X and S2Y are further stored in sample and hold circuits S1X and S1Y respectively. The first analogue switch is re-opened.

The first stage of shift register SRB now changes to logical '1', closes the first switch of groups Bx and By and connects $(X_1^, Y_1^)$ via the unity gain amplifiers $a_{x4}$ and $a_{y4}$. From the connections shown in the block diagram it is seen that the output of each of these amplifiers is ideally zero. Under these conditions the output of the gate labelled G inhibits the "angle computation cycle" that would normally follow, and SRB is advanced to logical '1' in its second stage. The second pair of input voltages $(X_2^, Y_2^)$ are inverted and connected to amplifiers $a_{x4}$ and $a_{y4}$. The outputs of $a_{x4}$ and $a_{y4}$ represent $(X_1^ - X_2^)$ and $(Y_1^ - Y_2^)$ respectively. These voltages are inserted as initial conditions to the inverse resolver circuit and the required angle computed (see later). Shift register SRB is advanced to a logical '1' in its third stage and the procedure is repeated, that is $(X_1^ - X_3^)$, $(Y_1^ - Y_3^)$ are fed to the inverse resolver and so on.

It is arranged that unused inputs are connected, by means of
front panel switches, to their respective sample and hold circuits S2X and S2Y. When these inputs are interrogated the outputs of amplifiers $a_x^4$ and $a_y^4$ are both zero; the output of gate 'G' inhibits the angle computation cycle and advances SRB.
2.3.2 The inverse resolver

Before proceeding further with the block diagram description, a brief note is included explaining the operation of the inverse resolver and resolver circuits that were employed in the final system. These are discussed in detail in Chapter 7.

The inverse resolver consists of two integrators and a sign reversing amplifier connected as shown in Fig 2.4a. The arrangement satisfies the equation:

\[ \ddot{z} + \frac{1}{\tau^2} z = 0 \]  \hspace{1cm} (2.7)

Having a general solution \( z = A \sin \omega t + B \cos \omega t \). (\( \omega = \frac{1}{\tau} \))

If, at \( t=0, z=y, -\tau \dot{z} = x \), we obtain:

\[ \text{o/p}_1 = z = -x \sin \omega t + y \cos \omega t \]  \hspace{1cm} (2.8)

\[ \text{o/p}_2 = -\frac{z}{\omega} = x \cos \omega t + y \sin \omega t \]  \hspace{1cm} (2.9)

Considering \( x \) and \( y \) to be voltage co-ordinates of a point \( P \) (Fig 2.4b) it is seen that

\[ \text{o/p}_2 = R = x \cos \omega t + y \sin \omega t. \]

Also \(-x \sin \omega t + y \cos \omega t = 0\)

Suppose that a counter is allowed to function when the circuit is switched to the 'operate' or 'compute' mode. At the instant that \( \text{o/p}_1 \) passes through zero, the counter will contain the scaled angle \( \omega t \). At this instant also \( \text{o/p}_2 \) yields the resultant magnitude \( R \). Since in one cycle \( \text{o/p}_1 \) passes through zero twice, the correct crossing point has to be determined.
Fig 2.4a  Schematic diagram of the inverse resolver.

Fig 2.4b  Representation of a point P in cartesian and polar co-ordinates.
From equation (2.8) \[ \frac{d(o/p_1)}{dt} = -\omega(y\sin \omega t + x\cos \omega t) = -\omega R \]

For the correct angle condition the resultant R is positive.
Therefore detecting when \( o/p_1 \) crosses zero with a negative slope yields the required angle.

### 2.3.3 The resolver (Polar to cartesian co-ordinate transformation)

If only one initial condition \((-)\Delta s\), is applied to the circuit of Fig 2.4a (say to the second integrator) then in the 'compute' mode the output of this integrator describes the function \( \Delta \text{scos} \omega t \). The first integrator yields \( \Delta \text{ssin} \omega t \) at its output. If the circuit is allowed to operate for a time corresponding to an angle \( \theta/\omega \) and then stopped, the integrator outputs will be \( \Delta \text{scos} \theta \) and \( \Delta \text{ssin} \theta \).

### 2.3.4 Angle computation cycle

The cartesian co-ordinate voltage differences, \((X_1 - X_2), (Y_1 - Y_2)\) are connected as initial condition voltages to the inverse resolver. This is set to the 'compute' mode and concurrently counters 1 and 3 operate (Fig 2.3). Counting ceases when the comparator detects the zero crossing point at the output of the inverse resolver. The counters now register the scaled angle \(-\theta_1\) from the starting pole \((X_1, Y_1)\) to the second pole \((X_2, Y_2)\). Shift register SRB is advanced to its third stage. With \(-\theta_1\) retained in the counters, the process is repeated to give the scaled angle \(-\theta_1 - \theta_2\), where \(\theta_2\) is the angle from the starting pole \((X_1, Y_1)\) to a third pole \((X_3, Y_3)\). Angles to other poles and zeroes of a given transfer function are determined similarly.

For the correct evaluation of \( \text{arg} F(s) \), the angle counters
operate in the forward direction when zeroes are considered, and in the reverse direction for poles. If the inverse resolver period (τ) is 2.0ms, a clock frequency of 2.048 MHz will cycle a twelve stage counter once in this time. Thus sums of angles that exceed ±360° are brought within the range of ±360°.

2.3.5 Δs resolution cycle

At the end of the first complete angle computation cycle, the tenth stage of shift register SRB is at logical '1', and counters 1 and 3 contain the resultant angle ∑Z − ∑P. SRB is advanced to its eleventh stage for the start of the Δs resolution cycle. The first operation to be performed is the subtraction of π. This is carried out by forward counting in counters 2 whilst reverse counting in counters 1 and 3. When counter 2 reaches 180°, the count ceases and counters 1 and 3 contain the angle ∑Z − ∑P − π. FOR THE FIRST RUN THIS GIVES THE TANGENT TO THE LOCUS AT THE STARTING POLE (X₁, Y₁) i.e. the set-off direction θ (see Fig 2.1).

Counter 2 is cleared and parallel set to the same value as counter 1. A voltage Δs is applied as an initial condition to the second integrator of the resolver circuit. This is set into the 'compute' mode, and counter 1 is set to reverse counting. When this counter reaches zero the resolver is switched to a 'hold' mode. The output voltages of the resolver are x' = Δs cosθ and y' = Δs sinθ. x' is applied to one input of the summing amplifier aₓ₅, the other input of which is connected to the output of S1X. (S1X is 'holding' the X co-ordinate of the starting pole). These two voltages are summed, inverted to restore their correct sign, and applied to the sample and hold circuit S2X. The output of S2X is therefore X₁ + x'.
Similarly \( y' \) is summed with the output of \( S1Y \) to produce \( Y_1 + y' \) at the output of \( S2Y \). Thus \( S2X \) and \( S2Y \) contain the voltage co-ordinates of the trial point \( P(X_{i1}, Y_{i1}) \) - see Fig 2.1. \( S1X \) and \( S1Y \) still contain the co-ordinates of the starting pole \( (X_1, Y_1) \).

Counter 1 is now parallel set to the value in counter 2 i.e. the set-off angle \( \theta \). Counters 2 and 3 are set to zero and shift register SRB recirculates setting its first stage to logical '1'.

2.3.6 Iteration phase

The whole process so far described repeats itself with certain exceptions. The outputs from amplifiers \( a_{x4} \) and \( a_{y4} \) sequentially take on pairs of values \( (X_1 - X_{i1}), (Y_1 - Y_{i1}); (X_2 - X_{i1}), (Y_2 - Y_{i1}); \) etc. Each time the angle computed is added or subtracted (for zeroes and poles respectively) to counters 1 and 3, the former still containing \( \theta \). At the end of the angle computation counter 1 contains \( (\theta + \Sigma Z - \Sigma P) \), and counter 3 contains \( (*Z - *P) \). This expression \( (*Z - *P) \) is the sum of the angles from the trial point to all the zeroes and poles.

The \( \Delta s \) resolution cycle commences and \( 180^\circ \) is subtracted from counters 1 and 3, which will yield \( (\theta + \psi_1) \) and \( \psi_1 \) respectively; where \( \psi_1 \) is the phase error.

If \( \psi_1 \) is less than \( \epsilon \) (a specified error) the system enters the 'output up-dating phase' (see later).

If \( \psi_1 \) is greater than \( \epsilon \) the procedure continues exactly as before, namely, counter 2 is set to the same value as counter 1, \( \Delta s \) is set into the resolver, this yielding the values:

\[
x'' = \Delta s \cos (\theta + \psi_1), \quad y'' = \Delta s \sin (\theta + \psi_1)
\]
The output of S2X is therefore updated to $X_1 + x''$. In the similar Y channel S2Y gives an output $Y_1 + y''$. S2X and S2Y therefore hold the co-ordinates of the second trial point $(X_{i2}, Y_{i2})$. S1X and S1Y still hold the co-ordinates of the starting pole.

Counter 1 is parallel set to the value in counter 2, i.e. $\theta + \psi_1$. Counter 2 and counter 3 are set to zero, shift register SRB recirculates, sets its first stage to logical '1' and the iteration phase commences again.

2.3.7 Output updating phase

(i) Eventually in the iteration phase the condition that the phase error $\psi_r$ is less than $\epsilon$ (monitored in counter 3) is satisfied. When this occurs counter 1 contains the total angle $(\theta + \psi_1 + \psi_2 + \ldots \psi_r)$ and this is parallel fed to counter 2. S2X and S2Y now hold the co-ordinates of a trial point which is also a true point $X_{ir}$ $Y_{ir}$ (see Fig 2.1) in the locus to within $\pm \epsilon^o$. The sample and hold circuits S1X and S1Y are now operated to hold these values of the locus co-ordinates, and give the required inputs to the cathode ray oscilloscope.

(ii) After the completion of (i) we have the last computed angle $\phi = (\theta + \psi_1 + \psi_2 + \ldots \psi_r)$ contained in counter 2. This is transferred back to counter 1, and still retained in counter 2.

$\Delta s$ is set as an initial condition to the resolver which is again operated in conjunction with counter 1 until the latter reaches zero. The resolver will now
hold the values $\Delta \cos \phi$ and $\Delta \sin \phi$. As before these are summed with the outputs of S1X and S1Y to give the co-ordinates of a new trial point $Q$ (see Fig. 2.1) stored in S2X and S2Y. Counter 1 is parallel set to the value in counter 2. Counters 2 and 3 are set to zero and the system re-enters the iteration phase.

The system explained above will plot points in the branch of the locus associated with the original starting pole $X_1, Y_1$ until a stop signal is given. In the constructed machine this was a timing pulse of nominally one second repetition rate, one second being the estimated maximum time required to plot a branch of a locus. This pulse sets the second stage of SRA to logical '1', resulting in the second pole $(X_2, Y_2)$ being made the starting pole. The whole procedure repeats itself and plots the branch of the locus associated with this pole.

When the system has plotted the locus of all the poles to be considered, the routine re-commences with pole 1.
Overall performance will be determined mainly by the inherent offset voltage drift and gain errors occurring in the analogue sections of the system. In studying these errors it is necessary to distinguish between totally self corrective and partially corrective errors. The latter are dealt with in this chapter, the circuit elements in question being amplifiers $a_{y1}$, $a_{y3}$ and $a_{y4}$ in the Y channel (see Fig 2.3) and the corresponding amplifiers in the X channel. The analysis shown can be applied to errors occurring in the remaining analogue sections. These errors are discussed in Chapter 4.

In the vicinity of a pole the phase distribution in the complex plane consists of radial lines and is independent of the pole-zero pattern$^9$. For a short vector length $\Delta s$, the locus can be considered as practically a straight line over two or three vector lengths. This assumption is made when analysing the different types of error occurring in the system.
3.1 Effects of offset voltage

For ease of explanation it will be assumed initially that the X channel has zero offset voltage. The total offset voltage occurring in the Y channel, due to elements \( a_{y1}, a_{y3} \) and \( a_{y4} \) (see Fig 2.1) is represented by \( e_{oy} \). As an example we consider the locus of a system having an open loop transfer function:

\[
\frac{K}{s(s + 3 + j4)(s + 3 - j4)}
\]  

(3.1)

the root locus being shown in Fig 3.1.

At the start of the computation the outputs of S2Y and S1Y are both set to a voltage representing the y co-ordinate of P (4 units). The output of S2Y is used to produce the y cartesian co-ordinate voltage difference values between P and Q and then between P and R. These values are employed in determining the set-off angle \( \theta \). If the offset voltage \( e_{oy} \) is small, \( \theta \) will have almost its correct value. The resolver yields components \( \Delta s \cos \theta \) and \( \Delta s \sin \theta \) that are summed with the outputs of S1X and S1Y respectively to update S2X and S2Y. The situation to this point is shown at the trial point S in Fig. 3.2, where PS = \( \Delta s \).

The cartesian co-ordinate voltage differences between S and the three poles would normally be applied in succession to the inverse resolver, but due to \( e_{oy} \) the trial point appears to be at the point a. The principal source of error occurs when determining the angle back to the starting pole P. If the line PS lies on the true locus, which is very nearly true for small \( \Delta s \), the first phase error \( \psi_1 \) is equal to \( /aPS \). This is added to the set-off direction \( \theta \) to give a new angle \( \theta - \psi_1 \).

The resolver outputs at this new heading angle are again summed with the outputs of S1X and S1Y to give the voltage co-ordinates of the point \( S_1 \) in S2X and S2Y.
Fig 3.1 Root locus for a system having an open loop transfer function: $\frac{K}{s(s + 3 + j4)(s + 3 - j4)}$
Fig 3.2 Diagram showing effect of Y channel offset voltage ($e_{oy}$) on trial point position ($S$) at successive iterations.
Due to the offset voltage $e_{oy}$, the second trial point appears to be at the point $b$. From this point the angle computation is carried out to yield a second phase error $\psi_2 = \angle bPS$. This angle is positive, being on the other side of the locus to $a$, and is added to $(\theta - \psi_1)$ to yield a further trial point $c$. The computations proceed in this fashion until a trial point $n$ is found having a phase error less than the permitted value $\epsilon$. It is observed that when this condition occurs the outputs of $S2X$ and $S2Y$ hold the voltage co-ordinates of the point $S_n$. These values are connected to the sample and hold circuits $S1X$ and $S1Y$ and hence to the output display. Thus the first 'true' point is lying below the correct locus by an amount $e_{oy}$.

When the first 'true' point has been found, the angle counter contains the angle $\angle OPS_n$ with the value of the last phase error($\leq \epsilon$) suitably added. $S2X$ and $S2Y$ are updated to yield the point $S_{na}$, where $S_{na} = \Delta s$. Again as far as the angle computation is concerned the trial point appears to be at 'd'. The system behaves as before, to produce eventually in $S2X$ and $S2Y$ values representing the 'true' point $S_{na}$, where due to the offset voltage the point 'n' lies on the correct locus.

After the second 'true' point has been found, a further trial point is taken at the last heading angle (plus the last phase error) at a distance $\Delta s$ from $S_{na}$. From now on trial points are displaced from the correct locus by an amount equal to $e_{oy}$ and no more iterations per point should be required than in a system having zero offset voltage.

The above conclusions were tested using a simple digital computer program and found to be valid.

The question arises as to how large an offset voltage can be tolerated. Consider a possible locus where the set-off direction $\theta$ from
the starting pole is 0°. If the total offset voltage $e_{oy}$ is such as to
displace the trial point by an amount greater than $\Delta s$, then it follows
that no amount of angle correction will bring the apparent trial point on
to the locus. Hence, one condition is that $e_{oy} < \Delta s$. It should be
pointed out that if the set-off direction is progressively increased to
$\pi/2$, larger offset voltages can be progressively tolerated.

A more important consideration is where successive phase errors
become equal and the system enters a limit cycle. For example,
consider a possible locus having a set-off direction of 45°, (Fig 3.3).
If $e_{oy}$ equals 0.707$\Delta s$ then the first phase error $\psi$ equals $\theta$. The search
vector $\Delta s$ is now directed at an angle $(\theta + \psi) = 90°$ and the new trial
point is at B. The phase error is now $-45°$ and $\Delta s$ is directed at angle
$\theta$ again, and so on. The system is in a limit cycle where successive
trial points alternate between A and B. An analytic expression is now
derived for the maximum offset voltage that can be tolerated without
limit cycling occurring.

3.1.1 Determination of maximum value of offset voltage

(i) $e_{oy}$ positive, $\theta$ in third and fourth quadrants

Fig 3.4a shows a limit cycle for a general set-off direction
$\theta$. The tip of the search vector $\Delta s$ takes on alternating values of $L'$
and $M'$. Due to the offset voltage $e_{oy}$, the trial points appear to be
at L and M respectively. For a limit cycle $\angle MON = \angle NOL = \alpha$, and it
follows that $\angle L'OM'$ equals $\alpha$. Constructing $OP = e_{oy}$, $PL = PM = \Delta s$,
and $\angle LPM = \alpha$. Since $\angle LOM = 2\alpha$, P lies on the circumference of a circle,
whilst O lies on the circumference of a second circle that passes through
the centre of the first circle. This is shown in Fig 3.4b, where $\angle TON$
equals $\theta$. $QN$ is a diameter of the inner circle and so $\angle QON$ is a right
Fig 3.3. Diagram showing the limit cycle that occurs when
\[ \theta = 45^\circ, \, e_{oy} = \Delta s/\sqrt{2}. \]
Fig 3.4a A limit cycle (L → M) for a general set off direction $\theta$.

Fig 3.4b Re-arrangement of Fig 3.4a with constructions.
angle. Therefore $\angle POQ = \theta$. Putting $PQ = A$ and $QR = B$, we have

\[ A = \frac{\Delta s}{2\cos \frac{\alpha}{2}} \]  
\[ B = \frac{\Delta s}{4\cos \frac{\alpha}{2}\cos \alpha} \]  

From Fig 3.4c $\tan \phi = \frac{y}{x}$, $\tan \beta = \frac{y}{x + A}$

thus $\tan \beta = \tan(\phi - \beta) = \frac{Ay}{Ax + x^2 + y^2}$  

(3.4)

The equation of the circle is given by:

\[(x - B)^2 + y^2 = B^2\]

i.e. $x^2 + y^2 = 2Bx$  

(3.5)

Substituting in equation 3.4

\[ \tan \theta = \frac{Ay}{x(A + 2B)} \]  

(3.6)

Also from Fig 3.4c $e_{oy}^2 = (A + x)^2 + y^2$

and substituting from equation (3.5):

\[ x = \frac{e_{oy}^2 - A^2}{2(A + B)} \]  

(3.7)

From equations (3.6 and 3.7) and employing (3.5) where applicable, and then substituting from equations (3.2) and (3.3), we obtain:

\[ e_{oy} = \frac{\Delta s \cos \frac{\alpha}{2}}{\sqrt{\cos^2 \alpha + (1 + 2\cos \alpha) \sin^2 \theta}} \]  

(3.8)

For a limit cycle not to occur, $\alpha$ must equal zero. The maximum allowable value of offset voltage $e_{oy}$ is then given by:
Fig 3.4c  Re-arrangement of relevant section of Fig 3.4b used in deriving equations (3.4) to (3.7).

Fig 3.4d  Degeneration of Fig 3.4b for the case $\alpha = 0$, i.e. no limit cycle occurring.
When $\alpha = 0$, the points $L$, $N$, and $M$ in Fig 3.4b become a single point. This situation is shown in Fig. 3.4d.

For the special case when $\theta$ is precisely equal to $\pi/2$, $\alpha$ as an acute angle does not exist and the above analysis is inapplicable. For this special case limit cycling occurs when $e_{oy} > \Delta s$, the limit cycle angle being $\pm 180^\circ$.

(ii) $e_{oy}$ positive, $\theta$ in first and second quadrants

For these conditions a limit cycle cannot occur. However if $e_{oy}$ is too large for a particular set-off direction a trial point lying on the locus will not be found. In Fig 3.5a, $OP$ is equal to $e_{oy}$ and a circle of radius $\Delta s$, centred on $P$, is constructed. Now $\Delta s$ must meet the line $ON$ (the set-off direction) in order to give an apparent trial point in the locus. Hence $e_{oy}$ is to be reduced to a value $P'O$ (Fig 3.5b) such that $ON$ touches the circle. Thus $ON$ meets the circle at a tangent. If this were not so, then $ON$ would cut the circle and imply that a larger value of $e_{oy}$ could be used for the tip of the search vector to lie on $ON$. Therefore the angle shown is a right angle, and the maximum value of $e_{oy}$ is given by:

$$e_{oy}(\text{max}) = \frac{\Delta s}{\cos \theta} \quad (3.10)$$

Fig 3.4d and Fig 3.5b can be combined to show the maximum allowable value of $e_{oy}$ (positive) for different set-off directions. This is shown in Fig 3.6.
Fig 3.5  Effect of offset voltage (e_{oy}) in first quadrant.

Fig 3.6  Diagram showing maximum permissible value of e_{oy} (positive) for different set off directions \( \theta \).
Fig 3.7 Maximum permitted values of $e_{oy}$ and $e_{ox}$ (in directions indicated in inset), for different set-off direction $\theta$. 

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From equations (3.9) and (3.10) the values of $e_{oy}(\text{max})$ are calculated for varying $\theta$ and the corresponding diagram is given in Fig 3.7. It is seen that the minimum value of $e_{oy}(\text{max})$ is $\Delta s/2$ when $\theta$ tends to $\pi/2$. If $e_{oy}$ had been negative, then the same analysis would have yielded a minimum value for $e_{oy}(\text{max})$ of $\Delta s/2$ for $\theta$ equal to $-\pi/2$.

The discussion so far is applicable to an offset voltage $e_{ox}$ occurring in the X channel alone, the Y channel being assumed perfect. These results are shown by the bracketed angles in Fig 3.7. It is observed that the more critical values of $e_{ox}(\text{max})$ are in the range $\theta = -\pi/2$ to $\theta = +\pi/2$, whilst for $e_{oy}(\text{max})$ the range is $\theta = 0$ to $\theta = \pi$. Hence for the polarities of $e_{ox}$ and $e_{oy}$ shown, the worst combination of these offset voltages occurs in the range $\theta = 0$ to $\theta = \pi/2$. Fig 3.8 shows diagrammatically the worst combinations of positive and negative values of $e_{ox}$ and $e_{oy}$ in the four quadrants.

(iii) Considerations of worst case combinations of $e_{ox}$ and $e_{oy}$

Fig 3.9 shows offset voltages $e_{ox}$ and $e_{oy}$ summing to give a resultant voltage $e_{r}$. Constructing $SS'$ perpendicular to $e_{r}$, $TT'$ perpendicular to $ON$, it follows that $\angle S'ON = \angle UOT' = \psi$. The results obtained in (i) can be applied here with $\theta$ replaced by $\psi$. That is:

$$e_{r(\text{max})}^2 = \left[ e_{ox}^2 + e_{oy}^2 \right]_{(\text{max})} = \frac{\Delta s^2}{1 + 3\sin^2\psi} \quad (3.11)$$

From Fig 3.13

$$\sin\psi = \frac{e_{ox}\cos\theta + e_{oy}\sin\theta}{\sqrt{\left( e_{ox}^2 + e_{oy}^2 \right)^{1/2}}} \quad (3.12)$$

From equation 3.11, the minimum value of $e_{r(\text{max})}$ occurs when $\psi = \pi/2$, i.e.

$$\left[ e_{ox}^2 + e_{oy}^2 \right]_{(\text{max})} = \frac{\Delta s^2}{4} \quad (3.13)$$
Fig 3.8 Worst combinations of $e_{oy}$ and $e_{ox}$ in the four quadrants.

Fig 3.9

Fig 3.10

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If \( e_{ox} = e_{oy} = e_0 \), then
\[
e_0(\text{max}) = \frac{\Delta s}{2^{\sqrt{2}}} \quad (3.14)
\]

Equation 3.13 gives us the maximum values that the sum of the squares, of the two offset voltages, can take without limit cycling occurring for any set-off direction \( \theta \).

Summarising the conclusions arrived at in section 3.1.1,

(i) The resultant of the two offset voltages occurring in both channels must not be greater than \( \Delta s/2 \).

(ii) Offset voltage results in an increased number of iterations being required to find the first and second 'true' points in the locus, the number increasing as offset voltage increases.

(iii) The locus displayed on the C.R.O. or any other output device, will be displaced from the correct locus by an amount equal to the offset voltage.

3.1.2. Determination of the number of iterations required in finding the first 'true' point in the locus.

Fig 3.10 shows the situation after a number of iterations for a set off direction \( \theta \) and an offset voltage \( e_{oy} \). Angle A is the summation of all the phase errors generated at the previous trial points. The new trial point is at T having a phase error \( \phi \). From the figure,

\[
/ONL = (\pi/2 + \theta) \quad \text{and} \quad /OTL = (\pi/2 + \theta - \phi).
\]
Putting \( e_{Oy} / \Delta s = E \) we obtain

\[
\phi = \tan^{-1} \frac{E \cos \theta - \sin \phi}{\cos \phi - E \sin \theta}
\]

(3.15)

At the start of the computation, \( A = 0 \) and the first phase error \( \phi_1 \) is found from equation (3.15). For the second iteration, \( A = \phi_1 \) and a new phase error \( \phi_2 \) is determined. For the third iteration, \( A = (\phi_1 + \phi_2) \) and so on.

A computer program was developed to determine the phase errors at successive iterations for different values of \( E \) and \( \theta \). The results for the more important cases are shown in Fig 3.11, 3.12, and 3.13. From these the number of iterations required, to reduce the phase error to less than a specific value, can be obtained. For example in Fig 3.12 phase error bounds of \( \pm 0.5^\circ \) have been drawn, and it is seen that, for \( E = 0.4 \), not more than eight iterations are required for any value of \( \theta \). Fig 3.14 shows the number of iterations required, to reduce the phase error to less than \( \pm 0.5^\circ \), as a function of \( \theta \) for different values of \( E \).

As is to be expected from equation 3.9 and Fig 3.7, the number of iterations increases as \( \theta \) approaches \( \pi/2 \) for the case \( E = 0.5 \). It should be noted that for example a set off direction of \( 85^\circ \) is almost in the \( y \) direction. Hence the angular error associated with the first trial point is small, being very closely equal to \( 5^\circ \) even when \( E = 0.5 \).

Fig 3.13 enhances a feature exhibited by Fig 3.11 and 3.12. Namely, that the maximum phase error magnitude, at successive iterations, occurs at increasing values of \( \theta \). Fig 3.15 shows the ratio of the phase error magnitude at the hundredth iteration to the phase error at the first iteration for the range \( 80^\circ \leq \theta \leq 89^\circ \) (\( E = 0.5 \)). It is observed that at \( 89^\circ \) this ratio is 0.97, indicating that the system is very close to a limit cycle.
Fig 3.11 Graph showing phase error at successive iterations for varying $\theta$. ($E = 0.3$)
Fig 3.12  Graph showing phase error at successive iterations for varying θ. (E = 0.4)
Fig 3.13  Graph showing phase error at successive iterations for varying $\theta$. ($E = 0.5$)
Fig 3.14 Graph showing number of iterations required to reduce phase error to less than $0.5^\circ$ vs. set-off direction $\theta$, for different values of $E$. 

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Fig 3.15 Graph of $\frac{\Psi_{100}}{\Psi_1}$ vs $\theta$, for the range $80^\circ \leq \theta \leq 89^\circ$. 

for the range $80^\circ \leq \theta \leq 89^\circ$. 

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For offset voltages in both channels, equation 3.15 can be applied with the following substitutions:

\[
E_r = \sqrt{\frac{e_{oy}^2 + e_{ox}^2}{\Delta s}}
\]

\[
\theta_r = \theta - \tan^{-1}\frac{e_{ox}}{e_{oy}}
\]

The values of \(\theta_r\) given in brackets Fig 3.11 to 3.15 (inclusive) are for the case \(e_{oy} = e_{ox}\).

3.2 Effect of gain error

This is to be considered for two cases:

(i) Effect of gain error in the system up to the point where the cartesian co-ordinate voltage differences are obtained, i.e. the virtual earth points of amplifiers \(a_{x4}\) and \(a_{y4}\) in Fig 2.3. This is shown to have similar effects to offset voltage.

(ii) Effect of non unity gain error in \(a_{x4}\) and \(a_{y4}\) (assuming that there is no error of type (i) above).

3.2.1 Effect of gain error in deriving cartesian co-ordinate voltage differences

Initially gain error \(a_y\) in the Y channel is considered. The transfer function employed in section 3.1 is again used; the root locus being shown in Fig 3.1.

From pole \(P\), in Fig 3.1 the set-off direction \(\theta\) is determined. Since the angle to the starting pole is ignored, \(\theta\) will be very nearly
equal to the true set-off direction, provided \( \alpha_y \) is small. The operation of the resolver circuit yields voltages representing \( \Delta \cos \theta \) and \( \Delta \sin \theta \). These are added to the voltage co-ordinates of P to give the first trial point \( S \) (see Fig 3.16) stored in sample and hold circuits S2X and S2Y.

From \( S \), the angle to each pole is measured. For small \( \alpha_y \) the angles to the poles Q and R have very nearly their correct values. When calculating the angle to the starting pole P, because of gain error \( \alpha_y \), point P appears to be at \( P' \). The resulting phase error \( \psi_1 \) is indicated in Fig 3.16. By simple geometry it is seen that \( \psi_1 = \alpha PS \) where \( \alpha S = PP' \). The situation is now very similar to that of amplifier offset voltage discussed in section 3.1. \( \psi_1 \) is now suitably added to the set-off direction to give a new trial point \( S_1 \) stored in the sample and hold circuits S2X and S2Y. From \( S_1 \), the second phase error \( \psi_2 \) is determined and added to the total angle so far computed to produce a third trial point, and so on. The process continues until a point \( S_n \) is reached where the phase error \( \psi_n \) is less than the permitted value \( \varepsilon \). The voltage co-ordinates of \( S_n \) are stored in S2X and S2Y and sample and hold circuits S1X and S1Y are updated to display the point \( S_n \).

From \( S_n \), a new trial point \( S_a \) is taken, the angle to the starting pole being measured from \( d \). The vector heading from \( S_n \) is adjusted by successive phase errors until the point \( S_{na} \) is reached, where the phase error at \( n_a \) is less than \( \varepsilon \). Thus the system takes extra iterations in finding the first and second 'true' points when compared with a system having no gain error.

It is observed that the effects of amplifier gain error are very similar to the effects of amplifier offset voltage for trial points
Fig 3.16 Diagram showing effect of $Y$ channel gain error ($a_y$) on trial point position ($S$) at successive iterations.
in the vicinity of the starting pole. The conclusions arrived at in section 3.1.1 can be applied to gain error, the term "offset voltage" now being equal to $a_V$ in the Y channel and $a_V$ in the X channel. $V_{nx}, V_{ny}$ are the voltage co-ordinates of a starting pole.

### 3.2.2 Effect of gain error following the derivation of the cartesian co-ordinate voltage differences

In Fig 2.3 the cartesian co-ordinate voltage differences for the X and Y initial conditions of the inverse resolver, are obtained at the respective outputs of $a_{x4}$ and $a_{y4}$. Let these voltages be $V_x$ and $V_y$ respectively. The general angle $\theta$, resulting from the operation of the inverse resolver is:

$$\theta = \tan^{-1} \frac{V_y}{V_x} \quad (3.16)$$

Assuming the gain error in amplifiers $a_{x4}$ and $a_{y4}$ to be $a_x$ and $a_y$ respectively, the angle computed will be:

$$\tan(\theta + \delta\theta) = \frac{V_y(1 + a_y)}{V_x(1 + a_x)} = \frac{V_y(1 + a)}{V_x} \quad (3.17)$$

where $a = a_y - a_x$

From equations 3.16 and 3.17 we obtain:

$$\delta\theta = \tan^{-1} \left( \frac{aV_y}{V_x} \right) \frac{1 + \left[ \frac{V_y}{V_x} \right]^2 (1 + a)}{1 + \left[ \frac{V_y}{V_x} \right]^2} \quad (3.18)$$

For $a \ll 1$, the maximum angular error occurs when $V_y = V_x$, that is $\theta = 45^\circ$, whence $\delta\theta = \tan^{-1} \frac{\alpha}{2} \approx \frac{\alpha}{2}$ radian.

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At any point in the locus, for any pair of values of \( V_y \) and \( V_x \) connected to the inverse resolver, the angle computed will be in error by the amount given by equation (3.18). Hence if all six poles of the machine were being employed for a particular transfer function, the maximum total error could be \( 6 \alpha/2 \) rad. This implies that a point in a branch of the root locus makes an angle of \( 45^\circ \) to every pole. This is a very remote possibility. It is estimated that a more realistic figure is \( 1.5\alpha \) rad. for the maximum total angular error at any point in any branch of a locus, for any combination of poles and zeroes. It is noted that when zeroes are used, the total angular error reduces since the basic machine equation is \( |\Sigma Z - \Sigma P - \pi| \leq \epsilon \). Fig 3.17 shows an enlarged portion (obtained by computer program) of the locus given in Fig 3.1. Also shown is the locus obtained when the gain errors in amplifiers \( a_{x4} \) and \( a_{y4} \) are zero and 5\% respectively. For comparison purposes, the \( 177.6^\circ \) and \( 186^\circ \) loci of the given transfer function are shown.
Fig 3.17  Phase angle loci for one branch of the system $K/s(s + 3 + j4)(s + 3 - j4)$, including locus obtained when $Y$ channel gain error is 5%.
4.1 Effects of errors in the locus updating circuits

In the Y channel the locus updating circuit comprises amplifiers \( a_{y5}, a_{y6} \) and sample and hold circuits S2Y and S1Y (Fig 2.3 and Fig 4.1). In the X channel the corresponding elements are \( a_{x5}, a_{x6} \), S2X and S1X. In each sub-section that follows we consider initially errors in the Y channel alone. The open loop transfer function taken as an example in Chapter 3 is again considered, the root locus being reproduced in Fig. 4.2.

4.1.1 Effect of errors in sample and hold circuit S2Y

(i) Offset voltage

With pole \( P (V_x, V_y) \) as the starting pole the output of sample and hold circuit S2Y would be set initially to the nominal value \( V_y \). Due to offset voltage \( e_{ly} \) resulting from the operation of S2Y, the output of S2Y is \( V_y + e_{ly} \) (shown as point \( P' \) in Fig 4.3). Sample and hold circuit S1Y is assumed perfect, and its output is set to the same value of voltage as in S2Y, namely \( V_y + e_{ly} \). At \( P' \) the set off direction \( \theta \) is determined. Since the angle to the starting pole is ignored for the computation, then \( \theta \) is very nearly equal to its correct value for small \( e_{ly} \).

The resolver outputs, \( \Delta \cos \theta \) and \( \Delta \sin \theta \), are summed with the outputs of S1X and S1Y respectively and connected to the sample and hold circuits S2X and S2Y. Consequently the outputs of the latter contain the co-ordinates of the first trial point \( a \) (Fig 4.3) the ordinate of
Fig 4.1 Locus updating circuit (Y channel).

Fig 4.2 Root locus for a system having an open loop transfer function: \( \frac{K}{s(s + 3 + j4)(s + 3 - j4)}. \)
Fig 4.3  Effect of offset voltage \( (e_{ly}) \) generated in sample and hold circuit S2Y. Diagram shows positions of trial points \((a, b, \ldots n, a', \ldots)\) at successive iterations.
which is given by

\[ V_y + e_{ly} + \Delta s \sin \theta + e_{ly} \]

The additional \( e_{ly} \) term arises from the re-operation of sample and hold circuit S2Y.

For small \( \Delta s \), the line \( PS_1 \) can be assumed to lie on the locus. The phase error \( \psi_1 \) at a is equal to \( \frac{\Delta PS_1}{2} \). This is added to the set-off direction and a new trial point b is established. At b a further phase error is determined, and the process continues until a trial point n is found having a phase error less than \( \varepsilon \). It is observed that several iterations are required to find the first true point, and that the set-off direction is changed by an amount such as to compensate for the total displacement \( 2e_{ly} \).

When the first 'true' point n has been located, S1Y is updated to the value contained in S2Y, i.e. the ordinate value of the first point in the locus. From n a new trial point is taken at the last heading \( \frac{\Delta P'S_n}{2} \) (plus the last phase error) and re-operation of S2Y yields a trial point at a'. Extra iterations are taken in finding the second true point in the locus, the heading angle changing to compensate for the offset voltage \( e_{ly} \). After the second true point has been found, subsequent true points in the locus are located with no extra iterations being required when compared with a system having zero offset voltage.

It is observed that there is a similarity between this error and the off-set voltage error in the circuits preceding the inverse resolver (Chapter 3). The important difference is that offset voltage errors in S2Y and S2X are self correcting; in the sense that the outputs of these circuits eventually achieve values representing a 'true' point in the locus (within ± \( \varepsilon \)).
The system can enter a limit cycle and the analysis shown in section 3.1.1 can be applied to this case by replacing $e_{oy}$ by $2e_{1y}$.

From equation 3.9:

$$2e_{1y}^{\text{(max)}} = \frac{\Delta s}{\left(1 + 3 \sin^2 \theta \right)^{\frac{1}{2}}} \quad (4.1)$$

Considering the worst combinations of offset voltage $e_{1x}$ and $e_{1y}$ in the X and Y channels, we obtain from equation (3.13):

$$\left[(2e_{1y})^2 + (2e_{1x})^2\right]_{\text{max}} = \frac{\Delta s^2}{4} \quad (4.2)$$

From Fig. 4.3 it is seen that the effective step length, $P_n(=\Delta z)$, is less than $\Delta s$, resulting in an increase in the computation time required to plot a given section of the locus. By application of the cosine rule it can be shown that

$$\Delta z = \Delta s \left[1 - \frac{(\Delta V_y \cos \theta + \Delta V_x \sin \theta)^2}{\Delta s^2} - \frac{(\Delta V_y \sin \theta - \Delta V_x \cos \theta)}{\Delta s} \right] \quad (4.3)$$

$\theta$ (measured in clockwise direction), is the true heading angle at points in the locus where

$$\Delta V_y = 2e_{1y}, \quad \Delta V_x = 2e_{1x} \quad \text{for the first 'true' point and}$$

$$\Delta V_y = e_{1y}, \quad \Delta V_x = e_{1y} \quad \text{for the second and subsequent 'true' points.}$$

(ii) Gain error $\delta_1$

Upon updating $S2Y$ to the first trial point, its output becomes (see Fig 4.1):

$$\left[V_y(1 + \delta_1) + \Delta s \sin \theta \right](1 + \delta_1) = V_y(1 + 2\delta_1) + \Delta s(1 + \delta_1) \sin \theta$$

where $V_y$ is the ordinate value of the starting pole P.
For points in the vicinity of P (or any chosen point in the locus) the term \( \delta V_y \) can be considered as a constant. The discussion in (i) above applies to this case and the same conclusions hold. The term \( \delta_1 \Delta \sin \theta \) and the corresponding term \( \delta \Delta \cos \theta \) at the output of S2X, produce a change in the search vector heading. Fig 4.4 shows the search vector \( \Delta s \) at the correct heading angle \( \theta \). Due to the error terms given above, the actual search vector is \( \Delta s \theta + \delta \phi \). From the diagram

\[
AB = \delta_1 \Delta s, \quad AC = \delta \Delta s
\]
\[
\therefore BC = (\delta_1 - \delta) \Delta s
\]
\[
\text{and } BD = (\delta_1 - \delta) \Delta \cos \theta
\]  

(4.4)

Further

\[
DE = BD \sin \theta
\]
\[
AE = AB - BD \cos \theta
\]
\[
\delta \phi = \tan^{-1} \left( \frac{DE}{\Delta s + AE} \right)
\]  

(4.5)

(4.6)

(4.7)

From equations (4.4), (4.5), (4.6) and (4.7)

\[
\delta \phi = \tan^{-1} \frac{(\delta_1 - \delta) \sin \theta \cos \theta}{1 + \delta_1 - (\delta_1 - \delta) \cos^2 \theta}
\]

For \( \delta_1 \) and \( \delta \ll 1 \),

\[
\delta \phi \approx \frac{1}{2} (\delta_1 - \delta) \sin 2 \theta
\]

(4.8)

which has a maximum value of \( \delta_1 - \delta \) radian \( \frac{\pi}{2} \).

For low values of gain error the change of search vector heading is so small compared to the shift \( \Delta V \delta_1 \) of the trial point, that it can be neglected.
Fig 4.4  Diagram showing effect of gain error in the X and Y channels on the search vector heading.
(iii) Drift

Any practical analogue holding circuit will exhibit an output drift with time. In Fig 4.2, when computing the set-off direction from the starting pole P, the effect of drift will be negligible if the co-ordinate differences to the other poles are large compared with the drift magnitude. Hence the set-off direction is very nearly that of an ideal system, and the resolver outputs are suitably added to the outputs of S1Y and S1X to give point a in the locus, see Fig 4.5. From a the phase error is computed but, whilst this is progressing, point a is moving towards a'. Suppose the last angle to be measured is the one back to the starting pole, whence a has moved to a'. The error angle a'Pa' is suitably added to \( \theta \) to yield a new trial point b. When measuring the phase error again, b drifts to b' and is again significant in the measurement of angle referred to P. The system converges to a trial point n, which drifts to n' and yields a phase error less than the permitted angle \( \varepsilon \) and hence is a 'true' point in the locus.

There is a second order effect present in that the trial point takes on different positions. The angles to other poles (and zeroes) are therefore changing slightly. Hence the time that elapses before the angle to the home pole is measured, changes slightly. This, for well spaced poles (and zeroes), can be neglected.

If the output sample and hold circuit S1Y were immediately updated, the true point n' in the locus would be displayed. The final heading angle would have a value such as to compensate for the drift voltage \( e_{2y} \). This heading angle would be used again to determine a fresh trial point a\(_1\) which would drift to a\(_1\)' when the angle back to the starting pole was determined. Hence no extra iterations would be required for the second point in the locus compared with an ideal system.
Fig 4.5  Effect of drift \( (e_{2y}) \) in sample and hold circuit S2Y.

Diagram shows final trial point positions \( (a', b', \ldots n', a_1', \text{etc}) \) at successive iterations.
For the first true point the effects of drift are similar to the effects described when dealing with offset voltage in S2Y. The conclusions arrived at in section 4.1.1(i) apply at this first true point.

It was stated earlier that if the output sample and hold circuit S1Y were updated immediately after the measurement of angles from the trial point to the starting pole, then S1Y would yield a "true" point in the locus. This is of course a hypothetical case. There will always be a time lapse whilst \( \pi \) is being subtracted. The worst case occurs when all possible poles (6) and zeroes (4) of the machine are being used, and the first pole locus branch is being plotted. The output cannot be updated before all other poles and zeroes have been interrogated and the angle calculated. Since the main effect of drift occurs only in the measurement of the angle back to the starting pole, then S2Y may have drifted to \( N \) before updating the output sample and hold circuit (see Fig 4.5). This is equivalent to introducing an offset voltage of \( N - n' \) in S1Y, hence the locus will be displaced by this amount. This offset voltage in S1Y will reduce as successive poles are made the starting pole. In the X channel the same conclusions hold.

4.1.2 Effects of errors in sample and hold circuit S1Y

(i) Offset voltage \( e_{3y} \) (Fig 4.2, Fig 4.6)

At the start of the computation the output of S2Y is set to the \( y \) value, \( V_y \), of the starting pole P. The output of S1Y is \( V_y + e_{3y} \) where \( e_{3y} \) is the offset voltage generated in S1Y. The set off direction \( \theta \) is determined and \( \Delta s \sin \theta \) is obtained. This is summed with the output of S1Y to give the ordinate of the first trial point, \( a \), at the output of S2Y. Since the locus lies virtually on the line PS, the first phase
Fig 4.6 Effect of offset voltage ($e_{3y}$) generated in sample and hold circuit S1Y. Diagram shows trial points ($a, b, ... n, n_1$, etc) at successive iterations.
error, \( \psi_1 \) equals \( \alpha_{PS} \). This is suitably added to \( \theta \) to give a new heading and a resulting trial point \( b \) and so on. Thus extra iterations are taken in finding the first true point in the locus, and the heading angle is changed such as to compensate for the offset voltage \( e_{3y} \). Again the system can enter a limit cycle and the analysis given in Chapter 3 can be applied to this case, i.e.

\[
e_{3y}(\text{max}) = \frac{\Delta s}{1 + 3\sin^2 \theta}^{\frac{1}{4}}
\]  

(4.9)

For the worst case combination of offset errors \( e_{3x} \) and \( e_{3y} \) in the X and Y channels respectively,

\[
\left( e_{3y}^2 + e_{3x}^2 \right)_{\text{max}} = \frac{\Delta s^2}{4}
\]  

(4.10)

The second and subsequent true points in the locus are located with no more iterations than in the ideal case. It is noted that the effective step length \( \Delta z = \Delta n \) is less than \( \Delta s \), and equation 4.3 applies with \( \Delta V_y = e_{3y} \) and \( \Delta V_x = e_{3x} \).

Since the outputs of sample and hold circuits S2X and S2Y always "home" in to the co-ordinates of a true point in the locus, it follows that offsets in S1X and S1Y will result in a displacement of the output locus.

(ii) Gain error \( \delta_2 \)

Close to the starting pole the error term \( \delta_2 V_y \) is almost constant and can be considered as a fixed offset voltage. Conclusions arrived at in (i) above are valid in this case.
(iii) Drift

Initially $S2Y$ and $S1Y$ are set to the $y$ value of the starting pole and the set-off direction $\theta$ is obtained, see Fig 4.7. The resulting resolver outputs are summed with the respective outputs of $S1Y$ and $S1X$ to give ideally the co-ordinates of the point $a$ in the locus. However if during this computation time $S1Y$ has drifted by an amount $e^{4y}$ the outputs of $S2Y$ and $S2X$, when updated, yield the co-ordinates of the point $a'$.

From $a'$ a phase error $\psi_1$ is measured, added to the original set-off direction $\theta$, to give ideally a new trial point $b$, but due to the further drift of $S1Y$, yields the point $b'$. It follows that if the phase error $\psi_1$ due to drift is greater than the permitted angular error $\varepsilon$, then subsequent trial points will yield phase errors of approximate value $\psi_1$. Hence the system never reaches the point where the phase error $<\varepsilon$. Since $\psi_1$ must be less than $\varepsilon$, the worst case occurs when the set-off direction is $0^\circ$.

Hence approximately

$$\psi_1 = \frac{e^{4y}}{\Delta s} < \frac{\varepsilon \pi}{180} \quad (4.11)$$

i.e. $$e^{4y} < \frac{\varepsilon \Delta s \pi}{180} \quad \text{in the time for one iteration}$$

In the identical $X$ channel, the same argument holds. It follows that since the contribution of drift is less than $\varepsilon$, no extra iterations should be required. Drift will result in a gradually increasing displacement of the output locus, but this will always be within a band defined by the $(180 \pm \varepsilon)^o$ loci.
Fig 4.7  Effect of drift ($e_{h_y}$) in sample and hold circuit SLY.
Diagram shows positions of trial points (a', b', c' etc) at successive iterations.
4.1.3 Effects of errors in the summing and inverting amplifiers. Fig 4.1

Offset voltage and gain error in these amplifiers can be considered as errors present in the respective sample and hold circuits S2X and S2Y when updating to the first trial point. These have been dealt with in sections 4.1.1 (i) and (ii). Extra iterations are executed in finding the first true point in the locus.

4.2 Errors occurring in amplifiers $a_{x2}$ and $a_{y2}$

It is noted that these amplifiers are employed only once per branch of the locus. Offset voltage and gain error occurring in say, amplifier $a_{y2}$ results in the incorrect ordinate value of the starting pole being stored in S2Y. Again extra iterations are taken in finding the first point in the locus. However, at a true point the output of S2Y and S1Y will be the correct value, i.e. there is no displacement of the locus. Limit cycling can occur and equation (3.13) will apply.
5.1 Pole-zero Interrogation and Multiplexing

The input potentiometers are front panel mounted ten turn helical types with a calibration dial. Fig 5.1 shows switches in their appropriate positions for the setting up of an open loop transfer function consisting of a complex pole, a single pole and a zero. Red lines indicate the relevant signal paths.

The x and y co-ordinates of the complex pole are set up as voltages on the first two potentiometers \( P_{x1} \) and \( P_{x2}(Py_1) \). Analogue switches \( A_{lx} \) and \( A_{ly} \) are used to store the co-ordinates of the starting pole in sample and hold circuits \( S2X \) and \( S2Y \) respectively (see Fig 5.2). The B groups of analogue switches interrogate in turn the X and Y co-ordinates at successive input lines. When \( B_{lx} \) and \( B_{ly} \) are operated the output points \( X_B \) and \( Y_B \) yield the co-ordinates of the starting pole. When switches \( B_{2x} \) and \( B_{2y} \) are closed the co-ordinates of the conjugate pole connect to \( X_B \) and \( Y_B \). The y co-ordinate of this pole is obtained at the output of \( a_y^8 \) by the closing of analogue switch \( AB1 \).

The single pole has its x value set up on \( P_{x3} \). Switch \( S_{b2} \) sets the corresponding y value to zero. These voltages are connected to the output lines \( X_B \) and \( Y_B \) by the closing of analogue switches \( B3x \) and \( B3y \) respectively. Similarly the single zero has its x value set up on the potentiometer \( Z_{x1} \), and its y value set to zero by switch \( S_{d2} \). These voltages are interrogated by switches \( B7x \) and \( B7y \) respectively.
Fig 5.2 Diagram of system analogue sections.
It is arranged that for unused poles and zeroes the remaining input switches of the B group connect to the respective outputs of the sample and hold circuits S2X and S2Y. When these analogue switches close, the angle computation cycle is inhibited.

Amplifiers performing the function of \( a_{y7} \) and \( a_{y8} \) could be connected at each switch \( S_{a2}, S_{b2}, \ldots, S_{e2} \), thereby dispensing with the multiplexing arrangement \( AB1 \ldots AB5 \). This was rejected because

(i) it increases the amount of amplifier zero setting to be carried out,

(ii) the cost saving is marginal.

Outputs \( X_A, X_B, Y_A, Y_B \) connect to the amplifiers shown in Fig 5.2. The outputs of amplifiers \( a_{x4} \) and \( a_{y4} \) give initially the cartesian co-ordinate voltage differences between the starting pole and the other poles and zeroes. As the locus is plotted, \( a_{x4} \) and \( a_{y4} \) yield the cartesian co-ordinate voltage differences between trial points (or true points) and the poles and zeroes.

5.2 System control Fig 5.3, 5.5, 5.6

The logic design is based on the 74 series of transistor-transistor logic elements. A positive logic convention is used throughout the description that follows and all circuit elements shown by circles are NAND gates, unless otherwise stated.
5.2.1 Pole-zero interrogation control (Fig 5.3)

When the start button is pressed, logic '0' is applied to the clear input of the bistable F/F1, the Q output of which becomes low. A bistable is used here to avoid difficulties associated with switch contact bounce. The output of F/F1 is connected to the preset input of bistable F/F2, input A1 of monostable MS1A, and after differentiation operates monostable MS2. This latter monostable, and all others employed in the system (with the exception of MS1A, MS1B and MS4) are of the form shown in Fig 5.4, which shows also the input differentiating circuit. MS1A, MS1B and MS4 are integrated circuit monostables (Type SN74121N). Though more expensive these give better waveforms for long duration pulses than the type shown in Fig 5.4.

Output 2 of MS2 is fed via gates 1 and 2 to the clear line of shift register SRA. SRA consists of a five stage integrated circuit shift register (SN7496N) and a D type flip-flop (SN7474N). The output of gate 2 is connected through gates 3 and 4 and clears the eleven stage shift register SRB which consists of two type SN7496N shift registers and D type flip-flop SN7474N.

After SRA and SRB are cleared the trailing edge of the pulse of output 1 of MS2 operates monostable MS3, which sets the Q output of the first stage of SRA to logical '1'. Monostable MS4 is now operated generating a pulse (g₁) of approximately 0.1s duration. Thus A1 rises to logical '1' and operates switches Alx and Aly which interrogate the X and Y voltage co-ordinates of the first pole (see Fig 5.1). Pulse g₁ also operates sample and hold circuits S2X, S2Y, S1X and S1Y which store the respective voltage co-ordinates. Subsequently monostable MS5 generates a 10 μs pulse that sets the Q output of the first stage (B1) of SRB to logical '1'. B1 operates the analogue switches Blx and Bly (Fig 5.1)
Fig 5.4 Monostable circuit diagram (Mullard TTL Application Book)
The signal from MS5 is fed via gate 8 to operate monostable MS6. This inserts a delay time during which amplifiers reach their true output values and correctly operate discriminator gate G. (Fig 5.2). After this delay monostable MS7 is triggered. Depending on the state of the input line $G_o$, derived from gate G, the output of MS7 is routed either to monostable MS8 or gate 14. For the sequence so far described, where A1 and B1 have operated, $G_o$ is at logical '0'. The pulse is therefore directed via gates 9, 10, 13, 14 and 15 to advance shift register SRB to its second stage, i.e. output B2 is set to logical '1'. MS6 is again triggered. Signal B2 operates analogue switches B2x and B2y. The output of amplifiers $a_{x4}$ and $a_{y4}$ are now the difference of the X and Y co-ordinates respectively of the first and second pole. In this case the signal $G_o$ is at logical '1'. Hence the output of MS7, when it is triggered, is routed via gates 9, 10 and 11 to operate monostable MS8.

For unused poles and zeroes, the corresponding input multiplexing switches (Fig 5.1) are connected to S2X or S2Y. When these switches are operated, signal $G_o$ is at logical '0' and the output pulse from MS7 is recirculated to advance SRB. The discriminator gate can cause a system malfunction when double poles are present in the transfer function being considered. This can be avoided either by additional logic circuitry being employed, or by separating double poles by an amount greater than the discriminator gate threshold.

5.2.2 Angle determination and counter control

Operation of MS8 generates a pulse, $V$, of sufficient duration to apply the outputs of amplifiers $a_{x4}$ and $a_{y4}$ as initial conditions to the inverse resolver (Fig 5.2). When this is completed, $\overline{V}$, triggers
the D type flip-flop F/F6 (Fig 5.5), the Q output of which falls to logical '0'. This output connects via gate 24 to the D input of F/F7, the Q output of which rises to logical '1' on the arrival of the next clock leading edge. Hence T rises to logical '1' and switches the inverse resolver to the compute mode. The D input of F/F8 also rises to logical '1', and the output of F/F8 goes high on the second clock leading edge. Clock pulses are fed to counters 1 and 3 via gates 21 or 22. The above sequence of events is shown in Fig 5.9 and more fully discussed in section 5.4.1.

At the requisite angle the comparator, connected at the output of the inverse resolver, generates a pulse that is connected to gate 26, clears F/F6, F/F7 and F/F8 and stops the count. The Q output of F/F7, in falling to logical '0', operates monostable MS9. This generates a pulse, Q', that is applied to gate 14 (Fig 5.3). SRB is advanced to its third stage and the process continues.

When the eleventh stage of SRB is set to logical '1', it is necessary to inhibit the pulse output of MS7. Otherwise, dependent on the state of G, this pulse will either circulate and advance SRB to its first stage or cause a spurious output at V. This inhibition is achieved by connecting \( \overline{Q(B11)} \) to gate 9.

Output B1 of SRB is connected via gates 16, 17 and 18 to the clear input of bistable F/F5. Thus when B1 is high, W is at logical '0' and counters 1 and 3 count down. When B7 is at logical '1' the bistable is reset, and the counters count up. This achieves the correct calculation of angle, namely \( \Sigma Z - \Sigma P \). With B11 set to logical '1', counters 1 and 3 require reverse operation only. \( \overline{Q(B11)} \) connects via gates 17 and 18 to clear F/F5 and set W to logical '0'.

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Fig 5.5  Angle determination control and locus updating logic.
5.2.3 Subtraction of π and phase error determination

When Q(B11) changes to logical '1' the $\overline{Q}$ output of F/F9 goes low (Fig 5.5) and clock pulses are fed to the three counters. The Q output of F/F9 removes the inhibit on gate 31 (Fig 5.6) and gate 29. When counter 2 reaches 180°, indicated by its final stage rising to logical '1', the output of gate 31 falls to logical '0' and operates monostable MS10. The output of MS10 is used to clear counter 2 and F/F9.

Counters 1 and 3 contain the angle $\angle EZ - \angle EP - \pi$, which for the first machine operation is the set off angle $\theta$.

5.2.4 Trial point generation and locus updating

The trailing edge of the pulse output of MS10 (Fig 5.6) operates, via line K, monostable MS11 (Fig 5.5). The output pulse of MS11 is of sufficient duration to apply a voltage representing the search vector magnitude $\Delta s$ to the resolver circuit (line U). At the same time counter 2 is parallel loaded from counter 1. Bistable F/F10 is triggered, the D input of F/F7 rises to logical '1', and the resolver is set to the compute mode (line T) on the first clock leading edge. Via gate 20, and its succeeding circuits, counters 1 and 3 are operated. When the output N, of the zero crossing point detector, falls to logical '0' F/F10 is reset and stops the count. At this time the resolver is set to a 'hold' mode.

The signal at N also operates monostable MS12. Output 1 is used to operate sample and hold circuits S2X and S2Y (see Fig 5.2) the outputs of which yield the co-ordinates of a trial point. Output 2 of MS12 loads counter 1 to the value of counter 2. It is noted that counter 2 has been used here purely as a temporary store.
Fig 5.6  Circuit arrangement of angle determination counters.
The trailing edge of the output pulse of MS12 triggers monostable MS13 which generates a pulse $Q_r$. This pulse is fed to gate 34 thus setting counter 3 to zero. $Q_r$ is also fed to gate 14 (Fig 5.3) the output of which advances SRB to its first stage and commences the second iteration.

When the phase error recorded in counter 3 is less than a specified value $\epsilon$, output E is at logical '1'. Thus when monostable MS11 operates, a pulse $e_2$ is generated that updates S1X and S1Y (Fig 5.2) to the voltage co-ordinates of the true point contained in S2X and S2Y respectively. This updating takes place during the time that $\Delta s$ is being applied as an initial condition to the resolver circuit. The fact that E may be at logical '1' when the set off direction has been determined is of no consequence. S1X and S1Y which contain the co-ordinates of the starting pole, are 'updated' to these same values.

5.2.5 Switching to other starting poles Fig 5.3

As stated earlier the output of F/F1 connects to A1 of MS1A and sets the Q output of F/F2 to logical '1'. MS1A generates a 1.5 second pulse, after which time MS1B operates to give a 50ms pulse. The output of MS1B connects to the inputs of gates 3, 5 and 6. This results in SRA being advanced to its second stage and the initiation of the plotting of the locus associated with a second pole. The output of MS1B connects via gate 20 to re-operate MS1A and thus SRA is advanced approximately every second to a succeeding stage. With SRA connected as a circulating register, the system will successively and continuously plot all branches of a locus. When the stop button is pressed, the A2 input of MS1A is inhibited and SRA and SRB are cleared down.

5.2.6 Counter 1 zero crossing point detector

The arrangement is shown in Fig 5.7. When the counter is
Fig 5.7 Counter 1 zero crossing point detector.
at zero the outputs of all the input NOR gates are at logical '1'. The output of gates 7 and 8 are therefore '0' and gate 9 output is high.

Provided M and St. P are at logical '1' the output N is low. St. P is applied to ensure that, at the start of a branch of a locus, when all counters are cleared down, N does not fall to zero and operate MS12. Shortly after the application of St. P, flip-flop F/F10 is cleared and M falls to zero holding N high.

5.2.7 Phase error comparison circuit

The logic diagram is shown in Fig 5.8. Logic networks 1 and 4 are operated by the four least significant digits of counter 3. These networks are designed for the minimum value of phase error ε specified by the overall system performance (see Chapter 8). For a net negative angle greater than -ε, the outputs of network 1 and gate 2 are at logical '0' and the output of gate 3 is high. This results in E being at logical '1'. For a positive angle less than +ε, the outputs of gates 4, 5, 6, 7 and 8 are high. The outputs of gates 9 and 10 are low, resulting in the output of gate 11 being at logical '1'. Again E is high. At the design stage only quad two input NOR gates were available in the 74 TTL series, this accounting for the structural differences in Fig 5.8.

5.3 Timing considerations

Monostables MS2 and MS3 are not critical in their timing since they are used only once per machine operation and contribute little to the total computation time. MS5 is employed once per branch of a locus and again little time is saved by reducing its pulse duration. The pulse width of MS4 is dictated by the performance requirements of the sample and hold circuits S1X, S2X, S1Y and S2Y, and in particular by
Fig 5.8 Phase error comparison circuit.
capacitor dielectric absorption effects. As will be seen later these factors set a limit of approximately 0.1s pulse duration.

Since monostables MS6, MS7 and MS8 are employed for every angle determination, their pulse durations contribute significantly to the total computation time. The output of MS6 must be of sufficient duration to allow for the worst slewing rate of any amplifier employed in the derivation of signal \( G_o \), plus propagation delays in any of the associated circuits. A value of 35 µs was decided upon; this will be discussed in Chapter 6. Since the output of MS7 can be recirculated then it is imperative that MS6 is not operated early in its recovery period. Thus MS7 is also set to give a 35 µs pulse. The pulse width of MS8 is dictated by the design of the inverse resolver, and for the circuit used a value of 0.5ms is specified.

Monostable MS8 could be replaced by an inverter if the output of MS7 were employed to generate the signal \( V \). However the pulse duration of MS7 would then have to be 0.5ms. This would result in increasing the total computation time, compared with that taken by the arrangement adopted. This difference becomes particularly apparent when simple transfer functions, containing few poles and zeroes, are considered.

Monostable MS9 is employed for every angle computation and hence its pulse duration is made short (1 µs). The pulse widths of MS10 and MS13 are kept small, these being generated once per iteration. The timing period of MS11 is decided by the requirements of the inverse resolver and sample and hold circuits S1X and S1Y. The acquisition time of sample and hold circuits S2X and S2Y determine the pulse duration of MS12.
5.4 Errors occurring in counters and associated circuits

5.4.1 Angle determination error

Errors occurring in each angle determination phase of an iteration are additive in counters 1 and 3. These errors result from delays occurring in (i) the logic elements employed, (ii) the analogue switch and associated drive circuit connected to point T (Fig 5.5) and (iii) the comparator circuit. In addition when the count is stopped, the output of gate 21 (or 22) is raised to the high state. If this output had previously been at logical '0', one extra digit is counted.

To minimise the errors resulting from the above effects the arrangement of bistables F/F6, F/F7 and F/F8 was employed. Fig 5.9 shows the waveforms at relevant points in the circuit. It is seen that clock pulses to counters 1 and 3 are delayed for one period after the nominal start of the compute mode. The time interval 0 to \( t_1 \) represents

(i) the delay in F/F7
(ii) the delay in the analogue switch and associated drive circuit connected to T.

\( t_1 \) is the start of the event time to be measured. At a later time \( t_2 \), the output of the inverse resolver signals the cessation of count. After a time \( (t_3 + \delta) \) counting stops, where \( t_3 \) represents the delay in the comparator and logic elements 26, 27 and F/F8 and \( \delta \) is the delay in gate 21 (or 22). Expressing time in units of clock period \( \tau \),

\[
\text{True event time } T = t_2 - t_1 \\
\text{Count time } = t_2 + t_3 + \delta - (0.5 + \delta) \\
\text{Number of counts } N = T + t_1 + t_3 - 0.5
\]
Fig 5.9 Angle determination control logic timing waveforms.
N is an integer and is taken as the nearest whole number. This automatically includes the effect of the extra digit that can be counted when the count stops. Fig 5.10 shows the range of event time represented by a constant value N for different values of delay time \( t_1 + t_3 \).

Suppose \( t_1 + t_3 = \tau \) and that all six poles and four zeroes of the machine are in use. The range of error between the total count and the total event time in the computation \( \Sigma Z - \Sigma P \) is \( +6\tau \) to \(-4\tau \). If \( t_1 + t_3 = 0.5 \tau \), the range of error is \( \pm 5\tau \). For the range \( 0 \leq (t_1 + t_3) \leq \tau \), the maximum error in the computation is within the limits \( +6\tau \) to \(-6\tau \) for any instrument produced.

From chapter 7, the maximum delays in the comparator and analogue switching circuits, are 200 ns and 155 ns respectively. The total delay time in logic elements 26, 27 and F/F8 has a maximum value of 84 ns. Hence \( t_3(\text{max}) = 284 \) ns. Including the delay in F/F7, the maximum value of \( t_1 \) is 185 ns, resulting in \( (t_1 + t_3)_{\text{max}} \approx 470 \) ns. For a clock frequency of 2048kHz (\( \tau = 500 \) ns) the maximum error between the count and the total event time is less than \( \pm 6\tau \) (\( \pm 3\mu s \)) when all poles and zeroes are used in a computation.

The number of digits required to cycle a n-stage counter once (this representing 360°) is \( 2^n \). At a clock frequency of \( 2^{11} \)kHz, the time taken for this is \( 2^n/2^{11} \)ms. The frequency of the sine/cosine loop comprising the inverse resolver is therefore \( 2^{11}/2^n \)kHz. One clock digit, representing a time \( \tau \), corresponds to an angle of 360/2^n degrees. If n is large, the inverse resolver frequency is low, resulting in a long computation time. However, one digit represents a small angle and the total error in the computation \( \Sigma Z - \Sigma P \) is small. On the other hand if...
Fig 5.10  Ranges of value of event time (T) represented by a constant count N, for different values of total delay time ($t_1 + t_3$).
n is low, the computation time is shorter but the computation error is large. It was decided to make \( n = 12 \), this being partly prejudiced by the availability of fully connected reversible four stage counters in a single integrated circuit package. The resulting maximum computation angular error, \( k \), is therefore \( \pm 0.54^\circ \).

### 5.4.2 Determination of permitted phase error \( \varepsilon \)

In Chapter 3 it was shown that in a system having offset voltages in the X and Y channels extra iterations would be taken in finding the first true point in the locus. These iterations continue until the phase error at a trial point is less than or equal to a permitted value \( \varepsilon \). This situation is shown in Fig 5.11, where P is the starting pole and the search vector \( \Delta s \) is at a heading angle \( \theta \) from P. Due to an offset voltage \( e_y \) in the Y channel, the trial point is at \( n \). In the diagram the angle \( \pm\varepsilon \) centred on \( \theta \) represents the permitted phase error aperture determined by logic networks 1 and 4 of the phase comparison circuit (Fig 5.8). In Fig (5.11) the angle \( \varepsilon \) has been greatly exaggerated to clarify the explanation and analysis that follows.

If the phase error angle at \( n \) is slightly greater than \( \varepsilon \), a new iteration commences. The heading of \( \Delta s \) is changed by an amount of \( \varepsilon \) to give a new trial point within the aperture angle \( \pm\varepsilon \). This trial point, having a phase error less than \( \varepsilon \), would be taken as a true point in the locus.

As stated in section 5.4.1, the maximum error in the angle computation \( \Sigma Z - \Sigma P \) is \( \pm k \). Consider that when carrying out the angle computation at \( n \), the measured phase error is not \( \varepsilon \) but \( \varepsilon + k \). The
Fig 5.11 Diagram showing a trial point n at the limit of the phase error aperture $\pm s$. Due to counter error $\pm k$, the phase error is $(s + k)$ and the new trial point is at $n'$. 

$PQ = \Delta s$
heading of $\Delta s$ is changed by an angle $(\varepsilon + k)$ to give a new trial point $n'$ (see Fig 5.11) at a heading angle $(\theta - \delta)$. At $n'$ the phase error is again measured. This angle computation could now be in error by $\pm k$ indicating that $n'$ is not within the specified phase error aperture. Further iterations are executed until the phase error angle at a trial point is less than $\varepsilon$. If the point $n'$ is at a heading angle $(\theta - \varepsilon)$, then a limit cycle occurs, the limit points being $n$ and $n'$.

To ensure that extra iterations do not occur $\sqrt{E - \delta}$ must be greater than $\sqrt{k}$. To simplify the analysis that follows, it is assumed that angles $\varepsilon, \delta$ and $k$ are small. This is reasonable in the present application.

In Fig 5.11, considering $S$ as a tangent to the circle at the point $Q$,

$$\tan(\varepsilon + k) = \frac{S}{\Delta s}.$$  \hfill (5.1)

The line $nn'$ (which is parallel to $S$) produced, will meet $PQ$ at right angles. $nR$ is constructed perpendicular to $Pn'$.

$$\angle PnT = \frac{\pi}{2} - (\theta - \theta - \varepsilon)$$

$$\angle PnR = \frac{\pi}{2} - (\varepsilon + \delta)$$

Therefore $\angle Rnn' = (\theta - \theta + \delta) \frac{\pi}{2} (\theta - \theta)$. Hence $Pn = S\cos(\theta - \theta)$

and $$\tan(\varepsilon + \delta) = \frac{S\cos(\theta - \theta)}{Pn}.$$  \hfill (5.2)

Further putting $\theta + \varepsilon - \theta$ we obtain

$$\Delta s \cos(\theta - \theta) = Pn + e_\theta \sin \theta$$  \hfill (5.3)
Using the cosine rule, we obtain

\[ P_n = \Delta s \left[ \sqrt{1 - \frac{(e_{oy} \cos \theta)^2}{\Delta s^2}} - \frac{e_{oy} \sin \theta}{\Delta s} \right] \]  (5.4)

For the condition \((e - \delta) > k\), we obtain from the above equations:

\[ e > k \left[ \frac{2 \sqrt{1 - E^2 \cos^2 \theta - E \sin \theta}}{\sqrt{1 - E^2 \cos^2 \theta - 2E \sin \theta}} \right] \]  (5.5)

where \(E = e_{oy}/\Delta s\).

This expression is of importance in that it forms a link equation between the analogue and digital errors occurring in the system. From equation (5.5) the design curves shown in Fig 5.12 are obtained, the half aperture values of \(e\) are shown in degrees for \(k = 0.54^0\). For equal offset voltages in the X and Y channels, \(E\) is replaced by \(\sqrt{2}E\) and \(\theta\) by \((\theta - \pi/4)\) in equation (5.5) and Fig 5.12.

The results given in Fig 5.12 should be used as a guide only since they have been derived from worst case conditions that are unlikely to occur in practice. The basic assumption has been that the counter error alternates by its maximum positive and negative values \((\pm k)\) on alternate iterations. When measuring the phase error at \(n'\), the angles to the poles and zeroes (other than the starting pole) have barely changed from the value measured at \(n\). Hence we would expect the counter error to have a value nearly equal to \(+k\) again rather than the worst case value considered earlier of \(-k\). A factor of 0.5 applied to the value of \(e\) is considered reasonable, giving the values shown in brackets in Fig 5.12.

Further points to note are:

(i) Fig 5.12 applies when all six poles and zeroes of the instrument are employed. The situation eases when less are used.
Fig. 5.12 Graph showing phase error aperture $\varepsilon$, for different values of fractional offset voltage $E = \frac{e_o}{\Delta s}$, as a function of $\theta$. 

- 100 -
(ii) At successive points in the locus, moving away from the starting pole, the effects described become increasingly less important.

(iii) The angular accuracy of the instrument is ± (ε + k)°.

5.4.3 Resolver errors

After inserting the initial condition Δs in the resolver circuit bistables F/F10 is operated. Again there is a time delay t₁ (Fig 5.9) before the compute mode commences. When counter 1 reaches zero, detected by the signal on line N (Fig 5.7) falling to logical '0', the resolver is switched to 'hold'. The maximum total delay time t₄, due to all elements employed in generating N, plus M512 and F/F7 is 135 ns. The delay time t₅ incurred in turning OFF the resolver analogue switches is 240 ns (see Chapter 7). From Fig 5.9, it is observed that before the start of the first full clock period, the resolver is in operation for a time (0.5T - t₁). The total "over-run" time for the resolver is therefore (0.5T - t₁ + t₄ + t₅). The maximum value this can have is 625 ns, assuming t₁ = 0. This represents an error in search vector heading of less than 0.12° which is negligible.

5.5 The clock generator

Fig 5.13 gives the circuit diagram of the clock generator employed. The design is based on the Bowes¹⁰,¹¹ emitter coupled multivibrator. To ensure good frequency stability it is arranged that

(i) Transistor T₁ does not saturate.

(ii) The voltage swing at the collector of T₁ is made as...
Fig 5.13  Clock generator circuit diagram.
large as possible consistent with (i) above, thus reducing effects of base-emitter voltage ($V_{BE}$) changes of $T_2$.

(iii) The collector currents of $T_3$ and $T_4$ are constant, thus not altering the base current of $T_2$. This is achieved by means of zener diode $D_3$ and the diode $D_4$.

The voltage drop across $D_4$ tends to track with the $V_{BE}$ of transistors $T_3$ and $T_4$ as the temperature varies. A zener diode having a breakdown voltage $V_Z$ of 5.6V is employed, since the temperature dependency of $V_Z$ is a minimum at this value.

The resulting frequency stability of the circuit is typically ±0.1% for a ±10°C change in temperature.

Given a nominal clock frequency, $f$, at room temperature, then at a different temperature the frequency will be $f(1 \pm \delta)$. Thus in the angle computation ($\Sigma Z - \Sigma P$) all angles will be in error by the factor $(1 \pm \delta)$. No error occurs in the subtraction of $\pi$ since this is carried out digitally. The basic algorithm is now:

$$\Sigma Z(1 \pm \delta) - \Sigma P(1 \pm \delta) - \pi = 0$$

i.e.

$$\Sigma Z - \Sigma P - \frac{\pi}{1 \pm \delta} = 0$$

For small $\delta$, $\Sigma Z - \Sigma P - \pi(1 \mp \delta) = 0$

The system therefore plots the $180(1 \mp \delta)^0$ locus. For the frequency stability quoted above, the plotted locus is within the band of ±0.18° centred on the $180^0$ locus.
Diodes $D_1$ and $D_2$ ensure protection against base emitter reverse voltage breakdown in transistors $T_1$ and $T_2$. The resistor $R_2$ acting as a potential divider with $R_1$ removes the necessity of the additional supply voltage rail customarily employed for $T_1$. The frequency is given by the expression $f = 1/(4CR)$ where, $C = C_1 + C_T$ and $R$ is the parallel combination of $R_1$ and $R_2$. To ensure that this frequency tends to track with the inverse resolver/resolver frequency, similar types of components are employed in the timing sections of each circuit (see 7.2.2(i)). $R_1$ and $R_2$ are metal film resistors and $C_1$ is a polystyrene capacitor. The air spaced trimmer capacitor $C_T$, having a maximum value of 30pF, adjusts the clock generator frequency. The output of $T_2$ is suitably level changed in transistors $T_5$ and $T_6$ to give an output voltage compatible with the 74 series of TTL elements.
This chapter and the one that follows, deal with the design of the analogue sections of the system. Since the instrument is intended for laboratory use, an ambient temperature range of operation from 10° C. to 30° C is considered suitable. Throughout these two chapters results quoted will be maximum worst case values in this temperature range. These are followed, in brackets, by typical values in the temperature range. Amplifier zero adjustment is assumed to be carried out at 20° C.

The requirements of operational amplifiers employed in analogue computers are well known, and an optimum performance could be achieved by using the best (and most expensive) amplifiers available at the design stage. The author's objective was to show the feasibility of, and to produce, a relatively inexpensive instrument.

6.1 Specification of total permissible error

If the maximum value of any input pole or zero is 3.0V, and the C.R.O. has a tube face diameter of four inches, then the y axis sensitivity is 1.5 volts per inch. For a spot density of 10 locus points per inch, the value of $\Delta s$ is 150mV. Choosing a phase error aperture of ±1.15°, the permissible value of $E$ from Fig 5.11 is 0.3. From Fig 3.11 it is seen that not more than four iterations are required at the first trial point. For the specified value of $E$, the maximum quadrature sum of equivalent offset voltages in the X and Y channels is 50mV. In the design that follows, this figure is taken as the maximum allowable worst case value over the temperature and supply voltage range.
6.2 Choice of input potentiometers, analogue switches and amplifiers

The factors influencing the value of potentiometers are:

(i) Amplifier bias currents $I_B$, flowing in the input potentiometers, of resistance $R$, result in offset voltages being produced. In Fig 5.1 and 5.2, there is never more than one input amplifier connected to a potentiometer at any one time. Balancing of these amplifiers ($a_{x1}$, $a_{x2}$, $a_{y1}$, $a_{y2}$, $a_{y7}$) at a potentiometer setting of approximately $0.15R$, yields a maximum offset voltage of $\pm I_B R/8$ over the range of the potentiometer.

(ii) Close matching of the electrical and mechanical settings of the potentiometers is achieved if their resistance is much less than the input resistance of the input amplifier.

(iii) Potentiometer values should not be so low as to impose power supply difficulties.

For the purpose of this feasibility study potentiometer linearities of 1% were considered suitable, keeping in mind that the system output is displayed on a standard laboratory cathode ray oscilloscope.

Bipolar transistors can be used as series analogue switches but have an inherent offset voltage. Further, the base
driving current of any ON transistor flows into the connected
potentiometer and produces an error voltage. This latter effect can
be eliminated by transformer coupling the base switching drive. The
isolation between the gate drive and signal circuits provided by the
field effect transistor, and its lack of offset voltage make it highly
suitable in this application. Practically any type of junction FET
(or MOSFET) can be used, provided the ON resistance is reasonably low
and leakage current is small.

From a cost point of view, it would be attractive to use the
709C type of operational amplifier as extensively as possible, as it is
currently one of the cheapest available. This choice of amplifier and a
value of 1000Ω for the potentiometers can be justified by the discussion
given below (4.6.1). The maximum potentiometer voltage is 3V, this value
being determined by the maximum voltage that can be applied to later
parts of the system, in particular the inverse resolver discussed in
Chapter 7. The dissipation in each potentiometer is 9 mW, this being
well within the manufacturer's maximum figure.

6.2.1 Consideration of input amplifiers

The circuit diagram for these voltage followers is shown in
Fig 6.1. Amplifier input bias current, having a value of 1.8μA (0.32μA)
at 10°C, results in a maximum voltage variation of ±225μV (±40μV) over
the range of any input potentiometer. Linearising the input offset
current drift to 5nA/°C (0.7nA/°C) results in maximum voltage drift (at
the mid point of the potentiometer) of ±12.5μV (± 1.75μV) over the
temperature range.
Fig 6.1 Voltage follower circuit diagram.

Fig 6.2 Inverting (or summation) amplifier circuit diagram.
The field effect transistors employed (2N4860) have an ON resistance $r_{ds(on)} = 40\Omega$. The change in amplifier input offset current due to drift, flowing in $r_{ds(on)}$ produces an offset voltage of $\pm 2\mu V$ at the temperature extremes.

The maximum input voltage drift of the 709C amplifier is rather high, being approximately $30 \mu V/°C$. This figure is not quoted in data sheets and has been obtained by private correspondence. The output voltage drift of each voltage follower is $\pm 0.3mV (\pm 0.1mV)$ over the temperature range.

The supply voltage rejection ratio, for the 709C amplifier, is $200 \mu V/V (25 \mu V/V)$. For supply voltages of $\pm 15V \pm 1\%$, this can result in a maximum offset voltage at the output of each amplifier of $\pm 60\mu V (\pm 7.5 \mu V)$.

To summarise, the total output offset voltage due to all causes is less than $\pm 600 \mu V (\pm 160 \mu V)$ for amplifiers $a_{x1}, a_{y1}, a_{x2}, a_{y2}$ and $a_{y7}$.

The input resistance of a voltage follower is approximately equal to its common mode resistance $R_{cm}$. The value of this is not given in data sheets for the 709C amplifier. From discussion with Fairchild applications engineers it is estimated to have a value of several megohms. In order that the input amplifiers do not overload when all their input analogue switches are open, a $2M\Omega$ resistor is connected between their inputs and ground. This results in negligible potentiometer loading.

The open loop voltage gain of the 709C amplifier decreases by approximately $0.2%/°C$. Applying this to the data sheet minimum
value of 15,000 (45000) at 70° C, and taking into account the load (1kΩ) of the next stage, the minimum open loop gain is approximately 14,700 (42000) for amplifiers $a_{x1}$, $a_{y1}$, and $a_{y7}$. The common mode rejection ratio is 65dB (90dB) for the temperature range 0°C to 70°C. This shows slight variation with temperature. Amplifier gain error is therefore less than 0.12% (0.01%). There is a slight improvement in these figures for amplifiers $a_{x2}$ and $a_{y2}$, since in the steady state their output load is very high.

6.2.2 Analogue switch considerations

The field effect transistors employed have a maximum ON resistance of 40Ω, and a maximum cut off current of 0.25nA at 25°C. The voltage drop across any FET in the ON state is negligible, since the input resistance of the following amplifiers is very high. When any one FET of a group, say Blx to B10x (Fig 5.1) is switched on, the leakage currents of all the OFF FETs of the group flow in the ON FET and the associated input potentiometer. In the worst case, the total leakage current is $9 \times 0.25 = 2.25\text{nA}$. Allowing for the temperature dependency of this current the error voltage produced is so small, compared to errors discussed earlier, that it can be ignored.

Transient effects due to gate-drain capacitances are negligible, these producing short duration pulses. For any FET turning ON the capacitance charges via $r_{ds(on)}$ and the effective potentiometer source resistance. For a transistor turning OFF, the capacitance discharges via the next transistor turning ON.

The drive circuit used for the FETs is shown in Fig 6.3. It is of a conventional form as described in most application reports and
Fig 6.3 Field effect transistor gate drive circuit.
texts 18,19. Fast switching speeds are not essential since the shortest acquisition time of any analogue switch is 35μs determined by the pulse duration of monostable MS6 (Fig 5.3).

A common drive circuit is employed for pairs of switches operated by logic signals B1 to B10, and A1 to A6. For switches AB1, AB2 and AB3 two input drive circuits are required, as shown by the dotted connection in Fig 6.2. Switches AB4 and AB5 use the same drive circuit as B8x(B8y) and B10x(B10y) respectively.

### 6.2.3 Further amplifiers employed in the X and Y channels (Fig 6.2)

Amplifiers \( a_x^3, a_x^4, a_x^5, a_x^6, a_y^3, a_y^4, a_y^5, a_y^6 \) and \( a_y^8 \) are sign inverting or summation amplifiers. These are required to produce either the cartesian co-ordinate voltage differences for the inverse resolver, or to update the sample and hold circuits S2X and S2Y. Table 4.1 shows the total offset voltage and gain error in these amplifiers. In the gain error column the larger values apply when the input and feedback resistors are matched to within 0.1%, the larger resistor being in the feedback path. High stability metal film resistors having maximum temperature coefficients of 50ppm/°C are employed for the input and feedback elements. The differential temperature coefficient for a pair of resistors is estimated to be 20ppm/°C.
Table 4.1 Total drift plus offset voltage and gain error in the amplifiers listed employing the 709C type operational amplifier.

From Table 4.1, the maximum total offset voltage in the X channel, due to amplifiers $a_{x1}$, $a_{x3}$ and $a_{x4}$ is $\pm 2.32\text{mV}$ ($\pm 0.7\text{mV}$). The same value applies in the Y channel except for the case of complex poles or zeroes where due to amplifiers $a_{y7}$ and $a_{y8}$, the total offset voltage is $\pm 3.63\text{mV}$ ($\pm 1.1\text{mV}$). These figures are small compared to the maximum input voltage (3V) and result in negligible locus displacement.

The maximum gain error in the X channel is +0.36%. In the Y channel, for complex poles or zeroes, the maximum total gain error including $a_{y7}$ and $a_{y8}$ is +0.6%. Representing these errors by equivalent offset voltages, in terms of the maximum input voltage, we obtain $+10.8\text{mV}$ and $+18\text{mV}$ for the X and Y channels respectively. Total gain error can be reduced by inserting potentiometers $P_{x2}$ and $P_{y2}$ at the inputs of
amplifiers $a_{x4}$ and $a_{y4}$ respectively (see Fig 4.2 and section 8.1).

From equation 3.18, the maximum angular error $\delta_0$ due to amplifiers $a_{x4}$ and $a_{y4}$ is approximately $+0.034^\circ$. The maximum angular error at any point in the locus is estimated to be $3\delta_0 = 0.1^\circ$. In setting initial conditions in the inverse resolver further gain error is introduced. This is discussed in Chapter 7.

6.3 Effect of amplifier slewing rates

The typical slewing rate value for the 709C operational amplifier is 0.25V/μs, using the standard lag compensation circuit. With this compensation the typical noise voltage, for a voltage follower amplifier having a source resistance of 1KΩ, is approximately 0.01mV rms. A minimum value of slewing rate is not quoted and is estimated to be 0.1V/μs. The compensation circuit component values were altered to give an estimated minimum slewing rate of 0.3V/μs, noise increasing to a value of approximately 0.03mV rms. For the sign inverting and summation amplifiers this value of output noise is doubled and trebled respectively. Compared to the error voltages produced by amplifier offset voltage drift, noise and its variation with temperature can be ignored.

It was stated in section 5.3 that the period of monostable MS6 is determined by the worst slewing rate of any amplifier employed in generating the logic signal $G_o$. The maximum voltage to be handled by these amplifiers occurs when any of the input switches are connected to the outputs of sample and hold circuits S2X and S2Y. This voltage (7.5V) is determined by the dynamic range of the inverse resolver. (See Chapter 7). This yields a maximum settling time of 25 μs. The
pulse width of monostable MS6 is set to 35 $\mu$s, providing ample allowance for delays in gate G, and for the approximate nature of the estimated values given above.

6.4 Sample and hold circuits, S2X, S2Y

The sample and hold circuits, S2X and S2Y are required to retain their information for one excursion of shift register SRB from B1 to B11. For a logical '1' in any stage of the shift register where an input pole or zero is being interrogated, it is necessary

(i) to set initial conditions in the inverse resolver, this taking a time of 0.5ms.

(ii) to allow the inverse resolver to operate and the required angle to be computed. For the sine/cosine loop period chosen the 'compute' time can be a maximum of 2ms.

The maximum time spent in the eleventh stage of SRB before updating to a new trial point is 5ms. Hence the maximum total excursion time of SRB is 30ms. when all poles and zeroes of the instrument are used.

Fig 6.4 shows the basic circuit of the sample and hold circuits employed. They are of a simple type employing a single FET and a relatively inexpensive FET differential amplifier (Analogue Devices 40K). Up to a point, drift due to leakage currents and offsets due to the gate driving waveform can be reduced by increasing the value of the storage capacitor $C_{st}$. For a given sampling time this imposes higher current requirements from the preceding amplifier and for the FET switch. The former can be achieved readily enough, if required, by the inclusion of discrete component Class B amplifiers in the output of the driving amplifiers $a_{x2}$, $a_{y2}$.
Fig 6.4  Basic circuit diagram of sample and hold circuits S2X and S2Y.

Fig 6.5  Circuit diagram of S2X and S2Y, showing Class B output stage and additional components $T_a$ and $R_a$. 
If MOSTs are employed in the circuit of Fig 6.4, their generally higher drain leakage currents worsen the performance in the hold condition. The use of two MOSTs in a bootstrapping arrangement\textsuperscript{21} in place of each JFET reduces leakage current by at least one order of magnitude.

An alternative to the type of sample and hold circuit used is the track/store unit usually found in hybrid computers\textsuperscript{22}. This requires precision input and feedback resistors, and gives a polarity inversion. For short acquisition times, the track/store unit imposes high current capability requirements in both its own and its preceding amplifiers. More sophisticated versions employing two amplifiers\textsuperscript{23,24,25} remove this requirement of the preceding amplifier.

For the amplifier employed in each of the sample and hold circuits S2X and S2Y, the maximum offset voltage drift is ±20 μV/°C and the maximum input current is −20pA at 25°C. The JFETs are 2N4860's having a minimum value of $I_{DSS}$ of 20mA, maximum drain leakage current of 250pA(c50pA) at 25°C, $C_{GD} = 8pF$, $r_{ds(on)} = 40\, \Omega$.

At 30°C, the maximum current in the storage capacitor, $C_{ST}$, in the hold mode, is 0.75nA(0.15nA) since there are two FET switches at the input of S2X and S2Y. For a value of $C_{ST} = 0.1\, \mu F$, this current results in a maximum voltage drift of 112 μV(22 μV) in a time of 15ms. This time is the maximum that can elapse in computing the angle from the first trial point to the starting pole. When a true point in the locus has been found, a further 15ms will have elapsed before updating the sample and hold circuits S1X and S1Y, resulting in a further error of 112μV.

The most suitable dielectric materials for capacitors employed in analogue computers are Teflon (PTFE) and Polystyrene\textsuperscript{16,26,27}. Teflon capacitors have the highest working temperature range to be found in plastic capacitors, but are very expensive. They have similar electrical characteristics to polystyrene, i.e. very high insulation resistance and
very low dissipation factor. Since high temperature operation is not called for in this application, polystyrene capacitors are employed.

When considering drifts in sample and hold circuits the effects of capacitor dielectric absorption must be taken into account. From an approximate model developed by Dow\textsuperscript{28,29} the lowest value of polarisation time constant for polystyrene has a value of 40\,ms with an effective capacitance $C_\parallel$ of $1.2 \times 10^{-4} \times C_{ST}$

The largest voltage change applied to the storage capacitor occurs when switching to a new starting pole, having just completed a previous branch of the locus. This voltage change can be approximately 10\,V. Thus in the first iteration time (30\,ms) the capacitor voltage will change by approximately 630 \,\mu V due to dielectric absorption. Although the effect is not too serious for S2X and S2Y, it was decided that for sample and hold circuits S1X and S1Y this should be reduced. Hence the sampling time when registering a starting pole is set to 0.1s (MS4 in Fig 5.3) ensuring that $C_\parallel$ has charged to 92\% of the input voltage. The secondary time constant, given by Dow as 0.58\,s, has an equivalent capacitance of $1.93 \times 10^{-4} \times C_{ST}$. For a 10\,V voltage change, the capacitor voltage will have changed only by approximately 120 \,\mu V due to both time constants after the first iteration.

Considering next errors due to offset voltage, we note that if the amplifier is balanced at 20\,°C, the maximum offset voltage produced over the temperature range is $\pm 200$ \,\mu V ($\pm 150$ \,\mu V). Supply voltage variations ($\pm 1\%$) contribute an output offset voltage of $\pm 150$ \,\mu V ($\pm 100$ \,\mu V). Offset voltage as a function of time is $\pm 1.15$\,mV ($\pm 0.25$\,mV) per month.
A further source of offset voltage error is capacitive coupling via $C_{GD}$ of the gate signal to the storage capacitor which occurs when the FET is turning off. For the FET quoted, the maximum value of $C_{GD}$ is $8\,\text{pF} \left( V_{GS} = -10\,\text{v} \right)$. With an effective mean gate drive of $15\,\text{v}$, and allowing $2\,\text{pF}$ for strays this yields an offset voltage of approximately $-1.5\,\text{mV}$. This can be reduced considerably by connecting an antiphase drive via a compensating capacitor, to the storage capacitor. This was not incorporated so as not to increase the number of "adjust on test" procedures to be carried out on the instrument.

During the initial condition and compute modes of the inverse resolver, the outputs of amplifiers $a_{x6}$ and $a_{y6}$ are varying. Considering the $X$ channel, this variation will alter the charge on $C_{ST}$ via the drain source capacitance, $C_{DS}$, of transistor $T_2$. For the case when all poles and zeroes of the instrument are being used there are twenty applications of charge to $C_{ST}$, in each iteration. To avoid the resulting displacements of the trial point that occur during iterations the additional transistor $T_a$ and resistor $R_a$ are employed (see Fig 6.5).

In the hold mode of the sample and hold circuit, the drain source capacitance of $T_a$ and the resistor $R_a$ act as a short time constant differentiating network, thus preventing build up of charge on $C_{ST}$.

The minimum values of gain and common mode rejection ratio for the 40K amplifier are $5 \times 10^4 \left( 2 \times 10^5 \right)$ and $66\,\text{dB} \left( 74\,\text{dB} \right)$ respectively. Connected as a voltage follower, the maximum total gain error of this amplifier is $\pm 0.1\% \left( \pm 0.04\% \right)$. With the maximum value of $x$ or $y$ of any starting pole being $3\,\text{V}$, this represents an error voltage $\delta E = \pm 3\,\text{mV} \left( \pm 1.2\,\text{mV} \right)$.

As stated earlier, the maximum voltage change applied to the sample and hold circuits is $\pm 10\,\text{V}$ occurring when a new starting pole is
interrogated. The 709C amplifiers employed for \( a_x^2 \) and \( a_y^2 \) (which connect to S2X and S2Y respectively) have an estimated maximum output current capability of 8mA at this voltage. A value of 3300\( \Omega \) for resistor \( R_1 \) (Fig 6.4) when added to \( r_{ds(on)} \text{max} \) maintains the current to well below this value. The time constant \( R_1C_{ST} \) is very much less than the sampling time of 0.1s. The maximum voltage change applied to S2X or S2Y at the end of any iteration is the search vector magnitude \( \Delta s \).

Hence if resistor \( R_2 \) is put equal to 390\( \Omega \), \( (R_a = 500\Omega) \) the maximum output current capabilities of \( a_x^6 \) and \( a_y^6 \) are not exceeded. The maximum time constant \( \left[ R_2 + r_{ds(on)} \right] C_{ST} \) is 43 \( \mu s \) and setting the pulse duration of MS12 to 0.5ms ensures adequate charging of the storage capacitor.

The amplifiers employed for S2X and S2Y have an output current capability of 5mA. In order to operate satisfactorily the subsequent sample and hold circuits S1X and S1Y, Class B common emitter output stages were added to the amplifiers employed in S2X and S2Y. The overall circuit diagram for these sample and hold circuits is shown in Fig 6.5.

6.5 Sample and hold circuits S1X, S1Y (Fig 6.6)

As discussed in Chapter 4, drift in these circuits must be less than \( \Delta s \varepsilon \pi/360 \) in the time for one iteration, where \( \varepsilon \) represents the maximum allowable angular error.

If the sampling time is short when registering a starting pole, the first two polarisation time constants for polystyrene can result in a 'drift' of 700 \( \mu V \) in the first iteration period. For small values of search vector magnitude \( \Delta s \), extra iterations will occur until the drift per iteration has reduced to a suitable value. For this reason the
Fig 6.6 Circuit diagram of sample and hold circuits SLX and SLY.
sampling time is set to 0.1s, reducing considerably the effect of the first polarisation time constant (40ms). The maximum drift for the first iteration is approximately 120 μV.

In Fig 6.6 the FET employed (2N4849) has basically the same characteristics as the 2N4860 used in S2X and S2Y, except that the minimum value of $I_{DSS}$ is 50mA and $r_{ds(\text{on})\text{max}}$ is 25 Ω. The amplifier is the Analogue Device type 40K. For a storage capacitor value of 0.5 μF, the maximum drift due to leakage current is less than 23μV (5 μV) in the time for one iteration. The maximum total drift is therefore 143 μV yielding a minimum value for $A_\Delta s$ of 13 mV.

Values of amplifier offset voltage and gain error are the same as those given in section 6.4. Feedthrough of the gate drive signal via $C_{GD}$ contributes an offset voltage of 240 μV. The outputs of the preceding sample and hold circuits change once per iteration and then only by a small amount ($\Delta A\Delta s$). Drain source capacitance coupling effects are therefore negligible.

For these sample and hold circuits, the FETs are operated when storing either the value of the starting pole or a true point in the locus. For the latter case, the sampling time is required to be short in order to achieve an overall low computation time. If we let this time be 1ms (set by MS11, Fig 5.4), then making $(R + r_{ds(\text{on})\text{max}})^{C_{ST}}$ equal to 125 μs ensures adequate charge of the storage capacitors. A suitable value of $R$ is 220Ω. For a possible maximum input voltage change of 10V, the peak current in the FET is 45mA. For the small value of time constant employed there are no dissipation difficulties.
6.6 Discriminator gate G

The discriminator gate has to operate for the two cases:

(i) When the starting pole is interrogated by its respective switch in the group B1 to B10. (See Fig 5.1 and 5.2)

(ii) When the B group of switches interrogate any input lines that are connected to the outputs of the sample and hold circuits S2X and S2Y.

In both channels case (i) is the more critical due to the inclusion of $a_{x2}$ and S2X in the X channel and the corresponding elements in the Y channel. From table 6.1 and section 6.4 the maximum equivalent offset voltage in both channels is within the range ±23mV. The discriminator gate threshold voltage $\Delta V_G$ is set to approximately ±28mV at both inputs.

The discriminator gate circuit is shown in Fig 6.7. It gives a logical '0' output when both inputs are within the range ±$\Delta V_G$ in any combination. A logical '1' output is obtained when either or both inputs are outside the range ±$\Delta V_G$ in any combination. Further the system does not give a false logical '0' output when the two input voltages are each greater than $\Delta V_G$ but differ in magnitude by an amount less than $\Delta V_G$.

Choosing the ratio $R_F/R_I$ to be 20 sets $\Delta V_G$ equal to ±25mV. If both inputs are within the range ±23mV, the output voltage of each amplifier is within the range ±0.46V. Hence the feedback silicon transistors and $T_4$ are nominally non-conducting, and the collector voltage of $T_5$ is approximately zero volts, i.e. logical '0'. If input 1 falls to -28mV, transistors $T_{1b}$ and $T_4$ conduct and the output
Fig 6.7 Discriminator gate (G) circuit diagram.
of \( T_5 \) goes high. If this input rises to 28mV, transistors \( T_{1a}, T_3 \) and \( T_4 \) conduct and again the output of \( T_5 \) is at logical '1'. For input 2, the operation is similar.

The resistors labelled \( R_a \) in Fig 6.7 are included to limit the collector currents in their associated transistors. The resistors labelled \( R_a \) ensure that collector leakage current is low when the associated transistor is in the OFF state. Reverse voltage breakdown of the base emitter junction of \( T_5 \) is avoided by means of the diode \( D_1 \). The value of \( R_1 \) is decided by the output current capability of the preceding amplifiers \( a_x \) and \( a_y \), which also connect to the inverse resolver.

The saturation collector current of \( T_4 \) is approximately 1.5mA. The minimum value of \( h_{FE} \) for the transistor is 50, giving a maximum base current of 30 \( \mu A \) for saturation. For transistors \( T_{1b} \) or \( T_{2b} \) the minimum value of \( h_{FE} \), at a collector current of 30 \( \mu A \), is approximately 30, yielding a base current of 1 \( \mu A \). Thus at the threshold limit an input change of 1.5mV switches the output from logical '0' to logical '1'.

The response of the system is mainly governed by the time constant \( 2C_{in}R_1 \), where \( C_{in} \) is the input capacitance of each feedback transistor in the OFF state. This is only of importance at input levels close to the threshold value. The value of \( C_{in} \) including strays is estimated to be at worst 20pF, giving a delay of approximately 4 \( \mu s \), for an input voltage of 1.5mV in excess of the threshold value. This is well within the margin of excess time allocated to the pulse width of monostable MS6. (see section 6.3).
At high input levels, the feedback transistors can be heavily saturated. The storage time when switching off is low compared to the time elapsed (35 μs) before the discriminator gate output is again required.
7.1 The inverse resolver and resolver

In the inverse resolver the cartesian co-ordinate voltage differences between a trial point and successive poles and zeroes are transformed to successive values of polar co-ordinates. The resolver generates cartesian co-ordinates from the polar co-ordinates $\Delta s$ and $\theta$.

These transformations can be implemented in several ways. Electro-mechanical methods such as the servo-positioned sine-cosine potentiometer and the induction type resolver can have high accuracies but are slow in operation. The latter type has the further disadvantage of requiring very accurate modulation and demodulation. In the all-electronic methods, one of the commonest types found in conventional analogue computers consists of sine and cosine diode function generators with coefficient multipliers and a quadrant selector. Different forms of function generator can be employed, for example level detecting comparators switching the inputs to a summation amplifier. These methods all require careful adjustment of diode (or comparator) conduction levels and amplifier gain. Other methods are the digital generation of sine and cosine functions, followed by a digital-to-analogue converter.

A method employed in hybrid computers, and used in this study, consists of two mode controlled integrators and a sign reversing amplifier connected to form a simple harmonic motion loop. This arrangement has a high speed of operation, but disadvantages associated with electronic switching and non ideal amplifiers are encountered.
The basic method of operation of the inverse resolver/resolver has been given in Chapter 2, section 2.3.2. The complete circuit is shown in Fig 7.1 and the required modes of operation are listed below.

The right hand column indicates the input states of the analogue switches, the entry "1" indicating those switches that are closed.

<table>
<thead>
<tr>
<th>Inverse resolver</th>
<th>Switches a</th>
<th>b</th>
<th>c</th>
<th>a</th>
<th>b</th>
<th>c</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Initial conditions representing the cartesian co-ordinate voltage differences to be set in integrators X and Y</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>2. The loop to be set to the &quot;compute&quot; mode. The comparator, which is described later, operates when the required angle is computed.</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Resolver</th>
<th>Switches a</th>
<th>b</th>
<th>c</th>
<th>a</th>
<th>b</th>
<th>c</th>
</tr>
</thead>
<tbody>
<tr>
<td>3. Initial condition representing the search vector magnitude Δs, to be set in the Y integrator</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>4. The loop to be set to the &quot;compute&quot; mode, for a time proportional to the angle to be resolved.</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>5. When the angle is resolved, the integrators to be switched to the &quot;hold&quot; mode.</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
The principal sources of error in the circuit of Fig 7.1 are:

(i) Finite switch resistance and its variation, non-equality of input and feedback resistances, and unequal integrator time constants.

(ii) Offset voltages produced by capacitive feedthrough of the gate drive signal to the integrator capacitor, when turning off switches.

(iii) Leakage currents, and amplifier bias current, offset current and offset voltage variation with temperature.

(iv) Non ideal amplifier frequency response.

7.1.1 Amplifier and analogue switch characteristics

To avoid repetition in the sections that follow the relevant characteristics of the amplifiers and MOSTs employed are given below.

(i) Integrator amplifiers

From considerations of the hold facility required of the integrators and to reduce input bias current effects when switching from the initial condition to the compute mode, the amplifiers chosen were FET input types (Analogue Devices 40K). These are relatively inexpensive. Their characteristics are as follows:
Voltage gain (Minimum)  
Worst case value: $5 \times 10^4$  
Typical value: $(2 \times 10^5)$

Input offset voltage change for a temperature range of $\pm 10^\circ C$ about ambient  
Worst case value: $\pm 200 \mu V$  
Typical value: $(\pm 150 \mu V)$

Input offset voltage change for $\pm 1\%$ variation of supply voltage  
Worst case value: $150 \mu V$  
Typical value: $(100 \mu V)$

Input bias current  
Worst case value: approx. $-30 pA$ at $30^\circ C$

Input offset current  
Worst case value: Approx. $\pm 15 pA$ at $30^\circ C$.

Input impedance  
Worst case value: $10^{11} \Omega / 3.5 \text{pF}$

Unity gain small signal frequency response  
Worst case value: $4 \text{MHz}$

\textbf{(ii) Metal oxide semiconductor transistors (Mullard, BSV81)}

Drain source on resistance ($V_{GS} = 5V, V_{DS} = 0V, T=25^\circ C$)  
Worst case value: $50 \Omega$ maximum

Drain source 'off' resistance ($V_{GS} = -5V, V_{DS} = 10V$)  
Worst case value: $10^{10} \Omega$ minimum

Drain cut-off current ($25^\circ C$)  
Worst case value: $1 nA$ maximum

Gate-drain capacitance  
Worst case value: $0.5 \text{pF}$ maximum

The MOSTs, in the circuit shown in Fig 7.1, are connected in a shunt series arrangement to reduce leakage current effects. When any series MOST switch is OFF, its drain terminal is connected to the amplifier virtual earth point, whilst its source and substrate are connected to a grounded MOST that is ON. Hence $V_{DS}$ is almost zero volts. For these conditions the value of leakage current is reduced by at least one order of magnitude.
An additional benefit resulting from the shunt-series configuration in this circuit is that the drain and source of each MOSFET are in the steady state, at approximately zero volts. Hence the gate drive signal can be a fixed voltage excursion. Further, a higher input signal voltage can be handled, the limit being determined by the maximum allowable peak gate voltage, instead of the "continuous gate voltage".

The maximum allowable "peak gate voltage to all other electrodes" \( V_{G-N} \) for the MOSFETs employed is \( \pm 15 \) Volts. To ensure that this value is not exceeded at the instant of switching any MOSFET, it is necessary to limit the output voltage of each amplifier in the inverse resolver and amplifiers \( a_x^4 \) and \( a_y^4 \). This is achieved by connecting two series combined silicon zener diodes (7.5V) between each output and ground (not shown in circuit diagram). For a \( \pm 5 \) Volts gate drive voltage, the maximum peak gate-source voltage is 13.2V.

The maximum voltages applied to the inverse resolver occur for transfer functions having complex poles, e.g. see Fig 4.2. When plotting the locus branch from pole \( P \), the maximum cartesian co-ordinate voltage differences occur when determining the angles to the complex pole \( Q \). If the locus is confined to the left hand of the s-plane and it is decided that the voltage ordinate of the locus on the y axis shall not be greater than the maximum value of the starting pole, \( V_y \), then the maximum \( X \) and \( Y \) inputs to the inverse resolver are \( V_y \) and \( 2V_y \) respectively. Hence the peak voltage occurring in the inverse resolver is \( \sqrt{(2V_y)^2 + V_y^2} \) and must have a value less than 8.2 volts; \( V_y \sqrt{2} \) is taken to be not greater than 7.5 Volts, i.e. \( V_y \leq 3 \) Volts. This value decides the voltage applied to the input potentiometers (Chapter 6). When plotting the locus of a pole at the origin, the maximum value of the
Fig 7.1 Circuit diagram of the inverse resolver/resolver.
locus along the X axis is 7.5 Volts. This same value applies in the y axis in the case of a double pole at the origin.

7.2 Discussion of errors arising in the inverse resolver

The two modes of operation of the inverse resolver are now considered, taking into account the sources of error listed in section 7.1

7.2.1 Errors in the inverse resolver in the initial condition setting mode

(i) $r_{ds(on)}$, and non-equality of input and feedback resistances

$r_{ds(on)}$ appears in the circuit between the input and feedback resistances summing junction and the amplifier input terminal. Its effect is to reduce the amplifier open loop gain, by a negligible amount.

The effect of non equal input and feedback resistance can be considered as a gain error in each channel. This has been considered already in Chapter 3, section 3.2.2 where it was shown that this could result in a maximum angular error of $\alpha/2$ rad; $\alpha$ being the difference between the gain errors in the two channels. Employing high stability metal film resistors matched to 0.1%, with the lower valued one of a pair connected in the feedback path in each amplifier, the angular error is $-\alpha/2$rad. = $-0.034^\circ$. This value includes a differential temperature coefficient of resistance of 20ppm/°C. Hence the angular error at any point in any locus is estimated to be within $-0.1^\circ$.

(ii) Effect of offset voltage produced by capacitive feedthrough

Including stray capacitance, the maximum value of drain-gate capacitance will be about 5pF. For a feedback capacitance of 0.03μF and gate drive signal of ±5V, the output offset voltage produced when turning
off a series MOST is approximately 1.7mV. This is reduced considerably by feeding an antiphase capacitive signal to the virtual earth point. Offset voltages at the output of each integrator can be considered as being present at the initial condition inputs of the inverse resolver. This has been considered in Chapter 3, section 3.1

(iii) Effect of leakage current, amplifier input current, offset current and voltage drift.

Amplifier offset current temperature dependency is negligible compared to offset voltage drift in the initial condition setting mode. The two amplifiers, being connected as unity gain, sign inverting amplifiers, have maximum output offset voltages of ±0.7mV (±0.5mV) at the extremes of temperature and supply voltage. These offset voltage drifts are constant at any temperature and can be regarded as offset voltages applied to the inverse resolver inputs. Their effect is the same as offset voltage discussed in Section 3.1. The drain cut-off current of the "off" transistors can be ignored.

(iv) Effect of non-ideal amplifier frequency response

This is of little importance in this mode. For the amplifiers employed, the minimum value of slewing rate is 6V/μs. This would only be considered if the time spent in the initial condition setting mode were very short.

7.2.2 Errors occurring in the inverse resolver in the compute mode

(i) Effects of unequal resistors \(R_x, R_y\), unequal capacitors \(C_x, C_y\) and non unity gain in the sign inverting amplifier

The general differential equation for the simple harmonic motion
(SHM) loop shown in Fig 7.2 in terms of a general dependent variable \( z \) is

\[
\dot{z} + \frac{(1 + \delta)}{R C x y} z = 0
\]

The frequency of the SHM loop is given by

\[
f_{\text{SHM}} = \frac{1}{2 \pi} \sqrt{\frac{(1 + \delta)}{R C x y}}
\]

(7.1)

The actual value of \( f_{\text{SHM}} \) is not critical; the frequency of the clock generator operating the angle counters can be adjusted such that the counters cycle once in a time of \( 1/f_{\text{SHM}} \). However, differences in the time constants of the two integrators, or non unity gain in the sign inverting amplifier produce amplitude errors that result in angle determination errors.

Fig 7.2 shows the voltages at the output of each amplifier in the compute mode resulting from the applied initial condition voltages \(-V_x\) and \(-V_y\). The angle condition detected by the comparator is

\[
V_y \cos \omega t = \frac{1}{\omega C R y} V_x \sin \omega t
\]

Substituting \( \omega = 2 \pi f_{\text{SHM}} \)

\[
\tan \omega t = \frac{V_y \sqrt{R C (1 + \delta)}}{V_x R C x y}
\]

For the given initial conditions, the correct angle should be given by:

\[
\tan \omega t = \frac{V_y}{V_x}
\]

(7.2)
Putting $R_y = R_x(1 + \alpha_1)$, $C_y = C_x(1 + \alpha_2)$ and $\delta$ non zero, the actual angle is given by:

$$\tan(\omega t + \delta \phi) = \frac{V_y}{V_x} (1 + \alpha)$$

(7.3)

where $\alpha = \alpha_1 + \alpha_2 + \delta$ for small $\alpha_1$, $\alpha_2$ and $\delta$

From equations (7.2) and (7.3) we obtain:

$$\delta \phi = \tan^{-1} \left( \frac{\alpha V_y}{V_x} \right)$$

(7.4)

$$1 + \left[ \frac{V_y}{V_x} \right]^2 (1 + \alpha)$$

This equation is the same as equation (3.18) and the conclusions arrived at in section 3.2.2 also apply here. Briefly, for small $\alpha$, the maximum value of $\delta \phi$ is $\alpha/2$ occurring when $V_y = V_x$.

To ensure small angular error, the relevant components should be matched to within 0.1%. The ON resistances of the MOSTs $T_{3x}$ and $T_{3y}$ should be matched to within a few ohms. A suitable value for $R_x$ and $R_y$ is therefore 10,000$\Omega$. For a frequency $f_{\text{SHM}}$ equal to 500Hz, a nominal value for $C_x$ and $C_y$ is 0.03\mu F.

The value for $\alpha$ is approximately $\pm 0.17\%$, resulting in a maximum value for $\delta \phi$ of $\pm 0.05^\circ$. At any point in the locus, the maximum total angular error is estimated to be $\pm 0.15^\circ$.

The variation of $r_{\text{ds(on)}}$ with temperature for the MOSTs employed is approximately 0.5%/°C. For high stability metal film resistors and polystyrene capacitors the variations are 50ppm/°C and 150ppm/°C respectively. By employing the same type of resistor and capacitor in the clock generator timing circuits, temperature effects are
minimised. A change of SHM loop frequency relative to the clock frequency results in the locus plotted being not exactly the 180° locus.

(ii) Effect of offset voltage produced by capacitive feedthrough when switching on transistors $T_{3x}$ and $T_{3y}$.

For a total drain–gate capacitance of 5pF (including strays) the output offset voltage generated, when switching on a series MOST, is approximately $-1.7\text{mV}$ in each integrator.

There is some cancellation between the offset voltage produced at the end of the initial condition mode, where $V_G$ for $T_{1x}$ and $T_{1y}$ excurses through $-10\text{V}$, and the offset voltage generated at the start of the compute mode. Employing compensating antiphase capacitive signals the residual offset voltages can be made very small. These also can be regarded as offset voltages present at the initial condition inputs.

(iii) Effect of leakage current, amplifier input current, input offset current and voltage drift

The total leakage current at the input to, say, the X integrator is the sum of the drain cut-off currents of $T_{1x}$, $T_{4x}$ and $T_{5x}$. For the shunt series connection shown in Fig 7.1 these currents and the amplifier input bias current are so small compared to the effects of input offset voltage drift that they can be ignored.

Consider a single integrator initially balanced at room temperature in the initial condition setting mode. At a different temperature, input offset voltage drift results in an input offset voltage that is constant at this new temperature. When switched to
the 'compute' mode, this offset voltage, \( v \), causes the integrator output voltage to increase at a rate of \( v/CR \) volts/sec. The voltage \( v \) can therefore be represented by a generator of emf \(-v\), connected via a resistor \( R \) to the input (virtual earth) of the amplifier. For the type of amplifier used, \( v \) can have a maximum value of \( \pm 350 \mu V \) (\( \pm 250 \mu V \)) at the extremes of temperature and power supply variation.

Fig 7.3 shows the amplifier offset voltage drifts \(-v_x\) and \(-v_y\) represented by equivalent input voltages. The following equations result:

\[
y = (V_y + v_x) \cos \omega t - (V_x - v_y) \sin \omega t - v_x
\]

\[
x = (V_y + v_x) \sin \omega t + (V_x - v_y) \cos \omega t + v_y
\]

It is observed that:

(a) the total offset voltage in one integrator can be considered as an offset voltage present in the initial condition of the other integrator. The effect of this type of offset voltage has already been considered in section 3.1

(b) Each integrator has a direct voltage at its output equal to the input offset voltage of the other integrator. Considering the \( x \) integrator output, this would lead to errors if the gain at points in the locus were calculated. For the \( y \) integrator, this direct voltage will lead to angular errors since it will alter the comparator threshold. This will be considered again later.
-\((1+\delta)\) + \(6\)

\[ V_x \cos \omega t \]

\[ \frac{(1+\delta)}{\omega R C_x} V_y \sin \omega t \]

\[ -\frac{1}{\omega R C_y} V_x \sin \omega t \]

**Fig 7.2** Inverse resolver outputs in terms of circuit components and initial condition voltages.

-\((1+\delta)\)

**Fig 7.3** Representing amplifier offset voltages by equivalent input generators \((-v_x, -v_y)\) applied to the inverse resolver.
(iv) Effect of non-ideal amplifier frequency response

Appendix A1 shows an approximate analysis for this case. For a SHM loop the results agree with the more general treatment by Dow.\textsuperscript{35} The slight change of frequency that occurs is unimportant, since angle determination is carried out by a frequency adjustable clock generator. More significantly the analysis shows that the damping factor $\zeta$ can be negative, having a value of approximately $-8$ for the amplifiers and circuit components employed. Since the inverse resolver does not operate for more than one cycle the maximum error is approximately 1.6%. This would introduce errors if the gain at points in the locus were calculated.

As shown in Appendix A2, the preferred method of increasing $\zeta$ if required, is to include some damping. This was not included in the instrument since experimental results showed a higher value for $\zeta$ than that given above. This is to be expected since it is unlikely that the amplifiers employed had their minimum gain-bandwidth value. Capacitor leakage resistance will also tend to reduce $\zeta$, but when using polystyrene types this effect is negligible.

(v) Effect of gate drive feedthrough when switching from compute to hold

The temporary hold mode of the inverse resolver, when the correct angle has been determined, is only of importance if the value of gain at points in the locus is to be determined. Offset voltages produced at
the outputs of the two integrators by capacitive feedthrough of the switching waveform can be reduced by means of an antiphase capacitive drive to the amplifier input.

(vi) Errors due to the sign inverting amplifier

Effects of gain error have been considered in section 7.2.2(i). The output offset voltage at a given temperature, arising from input offset voltage drift, acts as an input voltage applied to the X integrator. This type of error has been considered in (iii) above where the equations given apply here with \( v_y = 0 \). The same general conclusions apply, namely that this offset voltage behaves in effect as an error in the Y integrator initial condition. The direct voltage occurring at the output of the Y integrator alters the comparator threshold and introduces an error. In order to reduce this effect the operational amplifier type LM308A was employed. This has a maximum offset voltage drift of \( 5 \mu V/^\circ C \) \((1 \mu V/^\circ C)\) and minimum supply voltage rejection ratio of 96dB(110dB).

7.3 Discussion of errors arising in the resolver circuit

The three modes of operation of the resolver are considered here, taking into account the sources of error listed in section 7.1.

7.3.1 Errors occurring in the resolver in the initial condition mode

(i) \( r_{ds(on)} \), and non equality of input and feedback resistors \( R_{3y}, R_{4y} \)

As discussed when dealing with the inverse resolver, the effect of finite \( r_{ds(on)} \) is negligible since the input resistance of the operational amplifier employed is very high. Non unity gain due to
unequal resistors alters slightly the search vector magnitude and is unimportant.

(ii) Offset voltage due to capacitive feedthrough of gate driving signal at termination of initial condition mode.

After initial conditions have been applied, transistors $T_{5x}$ and $T_{5y}$ turn off and the gate drive signal is coupled, via the respective gate-drain capacitances and strays, to the integrator capacitors $C_x$ and $C_y$. As a result offset voltages $v_x$ and $v_y$ are produced at the outputs of the X and Y integrators. In the compute mode the output of these integrators will be $(\Delta s + v_y)\sin\omega t + v_x\cos\omega t$ and $(\Delta s + v_y)\cos\omega t - v_x\sin\omega t$ respectively. $v_y$ adds to the search vector magnitude and is unimportant. The effect of terms involving $v_x$ is to rotate the effective search vector heading by an angle $\delta \phi = v_x/(\Delta s + v_y)\,$rad., for small $v_x$. The first trial point $P$ will be displaced from the true locus as shown in Fig 7.4. When computing the sum of the angles to poles and zeroes, the principal contribution to the phase error will be the angle $\delta \phi$ (ignoring all other sources of error). If $P$ lies outside the phase error counter aperture $\epsilon$, then extra iterations will be executed until the trial point phase error is less than $\epsilon$. For any one instrument the value of $\delta \phi$ will be constant.

An alternative method of interpreting the change of search vector heading gives an approximate indication of the resulting number of additional iterations that may occur. For $\Delta s \gg v_x$, successive trial points are close to the true locus. The change in heading angle being small, the terms $v_x\cos\omega t$ and $v_x\sin\omega t$ are almost constant between one iteration and the next. Thus these errors can be considered as being
similar to fixed offset voltage errors in sample and hold circuits S2X and S2Y. As a worst case we can add the voltage \( v_x \) to the offset voltages present in S2X and S2Y. It is noted that the above errors do not result in extra iterations being taken in finding the second 'true' point.

(iii) Effect of leakage current, amplifier input current, input offset current and voltage drift

Numerical values here are the same as in the inverse resolver, where, at the extremes of temperature range, offset voltages of \( \pm 700 \mu V \) \((\pm 500 \mu V)\) can be present at the output of each integrator. The effect of these is the same as offset voltage due to capacitive feedthrough discussed in (ii) above.

(iv) Effect of non-ideal amplifier frequency response

As in the case of the inverse resolver, amplifier frequency response is of no importance in the initial condition setting phase.

7.3.2 Errors occurring in the resolver in the compute mode

(i) Effect of unequal resistances \( R_x, R_y \) unequal capacitances \( C_x, C_y \) and non unity gain in the sign inverting amplifier.

It is noted that the circuit is identical to that of the inverse resolver in the compute mode. Putting \( v_y = \Delta s \), \( v_x = 0 \) in Fig 7.2 yields the following x and y resolver components:

\[
x = \Delta s \cos \omega t
\]

\[
y = \frac{(1 + \delta)}{R_x C_x \omega} \Delta s \sin \omega t = \sqrt{\frac{R_x C_x (1 + \delta)}{R_y C_y x}} \Delta s \sin \omega t
\]
Putting \( C_y = C_x(1 + \alpha_1) \)
\[ R_y = R_x(1 + \alpha_2) \]

then for \( \alpha_1, \alpha_2 \) and \( \delta \ll 1 \)
\[ y = (1 + \alpha) \Delta \sin \omega t, \text{ where } \alpha = \frac{\alpha_1 + \alpha_2 + \delta}{2} \]

The \( x \) and \( y \) components are shown in Fig 7.5. The angular error \( \delta \phi \), of the resultant vector from its correct direction is:

\[ \delta \phi = \frac{\alpha \sin \omega t \cos \omega t}{1 + \alpha \sin^2 \omega t} \]

Therefore \( \delta \phi_{\text{max}} = \frac{\alpha}{2} \text{ radian.} \)

Ignoring other sources of error \( \delta \phi \) is very nearly the measured phase error at the first trial point. The set-off direction will be successively changed per iteration until the phase error is less than \( \varepsilon \). In finding further true points in the locus the phase error due to \( \delta \phi \) progressively decreases. For the same component tolerance as given in section 7.2.2(i) \( \delta \phi_{\text{max}} = 0.05^\circ \) and no extra iterations would be required in finding the first true point in the locus.

(ii) Effect of offset voltages produced by capacitive feedthrough when switching on transistors \( T_{3x} \) and \( T_{3y} \).

These voltages have the same effect as the offset voltages produced at the end of the initial condition setting phase. As explained when dealing with the inverse resolver, there is some cancellation of these voltages.
Fig 7.4  Representation of offset voltages generated in the inverse resolver at termination of initial condition mode.

Fig 7.5  Resolver components in the compute mode.
(iii) Effect of leakage current, amplifier input current, input offset current and voltage drift

As discussed in section 7.2.2(iii) the total offset voltages can be represented by generators of emf $-v_x$ and $-v_y$ connected via resistors $R_x$ and $R_y$ to the virtual earth point of the $x$ and $y$ integrators respectively. The maximum values of $v_x$ and $v_y$ are $\pm 350\mu V$ for the temperature range $10^\circ C$ to $30^\circ C$. The integrator outputs are

$$x = (\Delta s + v_x)\sin\omega t - v_y\cos\omega t + v_y$$

$$y = (\Delta s + v_x)\cos\omega t + v_y\sin\omega t - v_x$$

Points to note are:

(a) $v_x$ adds to the search vector magnitude and in this respect is unimportant.

(b) The effect of $v_y$ is to rotate the effective search vector by an angle equal to $v_y/(\Delta s + v_x)$. This is similar to the effect of offset voltage due to capacitive feedthrough at the end of the initial condition mode, (see section 7.3.1(ii)).

(c) Direct voltages, $v_y$ in the $x$ channel, $v_x$ in the $y$ channel, are fed to the locus updating circuits. These voltages behave as if they were offset voltages present in the sample-and-hold circuits $S2X$ and $S2Y$ respectively. It is noted that they do not contribute extra iterations in finding the second 'true' point.
(iv) Effect of non-ideal amplifier frequency response

As shown in Appendix A1 the integrator outputs are of the form $\Delta sc k^\theta/\omega \cos \omega t$ and $\Delta sc k^\theta/\omega \sin \omega t$, where $k$ is a constant for the given circuit. Thus the search vector magnitude varies slightly with $\theta$, but the vector direction is not changed. As shown in Appendix A2 the effect described can be partially compensated for by connecting a capacitor across the input resistor of each integrator.

(v) Errors due to the sign inverting amplifier

Effects of gain error have been considered in section 7.3.2(i). Offset voltage acts as an input voltage applied to the X integrator. This type of error has been considered in (iii) above, where the equations given apply here with $v_y = 0$. The same general conclusions apply in this case.

7.3.3 Errors occurring in the resolver in the hold mode

When the required values of $\Delta sc \cos \theta$ and $\Delta s \sin \theta$ have been computed, the resolver is switched to the 'hold' mode, where the input to each integrator is ideally open-circuited. The integrator outputs will be $\Delta sc \cos \theta + v_y'$, and $\Delta s \sin \theta + v_x'$, where $v_y'$ and $v_x'$ result from capacitive feedthrough of the gate drive signal, and droop due to leakage currents at the amplifier inputs. Again these voltages can be considered as being generated in the sample-and-hold circuits S2X and S2Y. They result in extra iterations in finding the first true point in the locus.

If the total drain-gate capacitance including strays is $5pF$, $C_x$ (and $C_y$) = $0.03\mu F$, and the gate drive voltage is $\pm 5V$, the output
voltage offset in each integrator is \(-1.7\text{mV}\). If required this can be considerably reduced by a suitable antiphase capacitive signal. The total leakage current is the sum of the drain cut-off currents of \(T_{1x}, T_{3x}, T_{5x}\) for the \(X\) integrator and \(T_{1y}, T_{3y}, T_{5y}\) for the \(Y\) integrator. As discussed earlier these currents are very low; for a hold time of 1ms the estimated maximum voltage change is \(20\text{\mu V}\). With the input virtually open-circuited, offset voltage due to input offset voltage drift introduces no additional error as temperature varies.

7.4 Noise considerations

Assume a noise voltage generator applied to the input of the \(X\) integrator (Fig 7.3). Since the simple harmonic motion loop never operates for a longer period than one cycle a steady state analysis of noise, based on the system frequency response, is not applicable. An approach that can be employed is one used for linear time varying systems\(^{36}\) which enables the mean square response of a system, \(q^2(t_2,t_1)\) to be determined at a time \(t_2\), due to noise applied continuously from a time \(t_1\) to \(t_2\). The mean square response is given by:

\[
\overline{q^2}(t_2,t_1) = \frac{1}{2\pi} \int_0^{\infty} \phi(\omega) |Y(j\omega, t_2,t_1)|^2 d\omega \quad (7.1)
\]

where \(|Y(j\omega, t_2,t_1)|^2\) is the sum of the squares of the system frequency responses at a time \(t_2\) due to a sinusoidal and cosinusoidal input applied at time \(t_1\).

and \(\phi(\omega)\) is the noise power spectral density.

Consider the SHM loop to be ideal, having a transfer function

\[
\omega^2/(s^2 + \omega^2),
\]

where \(\omega\) is the loop frequency. For a sinusoidal input of
unit amplitude \((\sin pt)\) the outputs \(V_{ox}, V_{oy}\) of the \(x\) and \(y\) integrators respectively are given by:

\[
V_{ox} = \frac{k}{1 - k^2}(\cos \omega t - \cos k \omega t)
\]

\[
V_{oy} = \frac{k}{1 - k^2}(\sin \omega t - \frac{1}{k} \sin k \omega t)
\]

where \(k = p/\omega\).

For a unit amplitude cosinusoidal input \((\cos pt)\) the outputs of the two integrators are:

\[
V_{ox} = \frac{1}{1 - k^2}(\sin \omega t - k \sin \omega t)
\]

\[
V_{oy} = \frac{1}{1 - k^2}(\cos k \omega t - \cos \omega t)
\]

A digital computer program was developed to calculate the value of \(|Y(j\omega, t_2, t_1)|^2\) at the output of each integrator at different frequencies. The results for some values of \(t_2\) are shown in Fig 7.6a and 7.6b. If in the range \(k = 0.01\) to \(k = 100\) we assume a white noise spectral density, \(N\) volts\(^2\)/unit bandwidth, then the maximum value for the area under any of the curves is not greater than about \(10^4\pi N\) volts\(^2\).

From equation 7.1, the effective mean noise voltage is therefore \(\approx 70E\), where \(E = \sqrt{N}\) = the input noise voltage per \(\sqrt{\text{unit bandwidth}}\). For the amplifier employed in the \(X\) integrator, the average value of \(E\) is \(3 \times 10^{-8}\) V/Hz\(^{1/2}\) in the frequency range represented by \(k = 0.01\) to 100. Thus the maximum effective noise has a value \(\approx 2.1\mu V\) at the output of each integrator. This is very low in value and can be ignored.

Similarly noise associated with the \(Y\) integrator amplifier and the sign inverter contribute little extra noise. At low frequencies (<5Hz) the amplifier noise starts to increase. From Fig 7.6b, the low frequency noise is doubled when \(t = 0.5\tau\). Again this is not serious compared to the errors introduced from other sources previously discussed.
Fig 7.6 Graphs of $|Y(j\omega, t_2, t_1)|^2$ vs. $k$ for different values of $t_2$.

(a) Output of X integrator
(b) Output of Y integrator.
7.5 MOST gate drive circuit

The drive circuit employed for each pair of shunt series arranged MOSTs is shown in Fig 7.7. When the input rises to logical '1', the three transistors conduct. The collector voltage of \( T_2 \) rises to approximately +5V, turning on the series MOST. The collector voltage of \( T_3 \) falls to approximately -5V switching off the shunt MOST.

High speed switching transistors are used in order to maintain angle computation errors within the limits given in Chapter 5, section 5.4.1. The transistor switching characteristics supplied by the manufacturers are as follows:

**BSX 19**

\[
t_{\text{on max}} = 12\text{ns}, \quad I_C = 10\text{mA}, \quad I_{B1} = 10\text{mA}
\]

\[
t_{\text{f max}} = 15\text{ns}, \quad I_C = 10\text{mA} \quad I_{B2} = 10\text{mA}
\]

\[
t_{\text{s max}} = 10\text{ns}, \quad I_C = I_{B1} = I_{B2} = 10\text{mA}
\]

where \( I_{B1} \) and \( I_{B2} \) are the forward and reverse base currents respectively.

**2N2411**

\[
t_{\text{on max}} = 25\text{ns}, \quad I_C = 10\text{mA}
\]

\[
t_{\text{off max}} = (t_f + t_s) = 100\text{ns}, \quad I_C = 10\text{mA}, \quad I_{B1} = 2.5\text{mA}, \quad I_{B2} = 2\text{mA}
\]

Applying the Ebers and Moll\textsuperscript{37} equations to the above data, approximate worst case values of transistor time constants can be evaluated. For the BSX19 transistor, the rise (and fall) time constant \( \tau_r \) is 25ns and the desaturation time constant \( \tau_s \) is 14ns. The estimated time delay time \( t_d \) is 4ns. These values are used to determine the switching times of transistor \( T_1 \) and \( T_3 \) in the circuit of Fig 7.7. The calculations are unnecessary for \( T_2 \) since this transistor is operating very closely to the manufacturers' test conditions.
Fig 7.7 MOST gate driving circuit.
The MOSTs in Fig 7.1 have maximum values of ON and OFF times of 20ns and 50ns respectively. These are not quoted in the data sheets and have been given as estimated maximum values by the manufacturers.

The following switching times apply to the circuits of Fig 7.7 and 7.1:

<table>
<thead>
<tr>
<th>Transistor</th>
<th>$T_1$</th>
<th>$T_2$</th>
<th>$T_3$</th>
<th>MOST</th>
</tr>
</thead>
<tbody>
<tr>
<td>On time (ns)</td>
<td>20</td>
<td>25</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>Off time (ns)</td>
<td>50</td>
<td>100</td>
<td>54</td>
<td>50</td>
</tr>
</tbody>
</table>

Consider the shunt series arrangements of MOSTs in the circuit of Fig 7.1. For any series MOST the total time between the logic signal '1' appearing at the input to the gate drive circuit and the closing of the switch is 65ns. For the associated shunt MOST the time elapsed before turning off is 115ns. When the logic signal falls to '0', the total time before the series switch turns off is 200ns and for the allied shunt switch the turn-on delay time is 224ns.

To each of the above time delays the author recommends the addition of a further time delay of 40ns to allow for strays and for the approximate derivation of some of the switching times. In Chapter 5, section 5.4.1, when calculating the time delay $t_1$ at the start of the compute mode, a value of 155ns was taken as the delay before the analogue switch operated. From the above, this is the time delay before the shunt MOSTs turn off. The time delay between the operation of the series and shunt switches of a pair is of little importance - in the compute mode the circuit is effectively in a hold condition for this time.

The outputs R and S connect respectively to the virtual earth points of the X and Y integrators. These outputs are provided only in the gate drive circuits used for generating signals $a$ (and $\overline{a}$) and $b$ (and $\overline{b}$) in Fig 7.1. That is, antiphase capacitive signals are
employed to cancel the voltage offsets produced at the end of the initial condition mode and at the start of the compute mode in the inverse resolver and resolver. The arrangement was not employed in the circuit generating signal $c$ (and $\bar{c}$) in order to reduce the number of adjustments to be carried out. The offset voltages produced when switching to the hold mode are only of concern in the resolver circuit, where they behave as offset voltages generated in sample and hold circuits $S2X$ and $S2Y$.

7.6 The comparator circuit

The correct angle is registered in counters 1 and 3 (see Chapter 5) when the output voltage of the inverse resolver $Y$ integrator is zero and has a negative rate of change with time. The minimum amplitude of this 'sinusoidal' voltage is determined by the voltage separation allocated to double poles. This separation, which must be greater than the threshold of discriminator gate $G$, is set to $40\text{mV}$. The minimum zero crossing point rate of change of voltage occurs only at the start of the computation when the set-off direction is being determined. At the first trial point the smallest amplitude of the $Y$ integrator output is the search vector magnitude $\Delta s$.

Fig 7.8 shows the complete comparator circuit. The value of the input resistor $R$ is specified by the maximum output current capability of the $Y$ integrator amplifier. The diodes $D_1$ and $D_2$ prevent overloading of the pre-amplifier at high input levels. The pre-amplifier is needed in this application for satisfactory operation of the type LM206 comparator unit. The operational amplifier selected for this purpose is the type $\mu A702A$ chosen specifically for its wide bandwidth and low cost. For the values of frequency compensation components shown in Fig 7.8 the minimum bandwidth is $4\text{MHz}$, the voltage gain being
Fig 7.8 Comparator circuit diagram.
approximately 12. The time difference between the input and output zero
crossing points is therefore approximately 40ns for small inputs. For
large inputs, when the diodes conduct, this delay will be slightly reduced
due to the approximate step nature of the voltage at the amplifier input.

In a limiting amplifier it is usual to find the clamping diodes
connected in the feedback path of a sign inverting amplifier. This
was not done here since the resulting closed loop gain variations of
the amplifier at different input levels could result in instability.
Employing high speed switching, low capacitance (1pF max) diodes, and
allowing 4pF for strays, the input time constant is less than 10ns.

The type LM206 comparator unit was chosen for its high speed
of response and output compatibility with the 74 series of TTL elements.
Appendix (A3) gives an approximate analysis for the time response of
this unit for an input ramp of C volts/sec at the zero crossing point.
In Fig A3.6 the correct zero crossing is shown at Q. The logic
threshold voltage for the subsequent inverter gate is indicated. It
is seen that for \( C = 1.5 \times 10^3 \text{V/s} \) (corresponding to \( V_{in} = 40\text{mV} \)) the time
difference between Q and R is approximately 10ns. When \( V_{in} \) is 400mV,
\( C = 15 \times 10^3 \text{V/s} \), the time difference is 35ns. As \( V_{in} \) increases, the
comparator unit input approaches a step function, and the time difference
remains approximately the same.

From Appendix (A3) the time delay before the comparator unit
output begins to change, for a ramp input, is less than 8ns. Thus the
total delay between the input voltage to the pre-amplifier crossing zero
and the output of the LM206 reaching the logical '1' threshold is
approximately 95ns. The maximum delay in the inverter gate and
monostable circuit is 45ns, yielding an overall delay of 140ns. Adding
a further 60ns, to account for the approximate nature of the analysis, gives an overall delay time of 200ns.

The maximum offset current and offset voltage drifts of the \( \mu A702A \) amplifier are \( 10nA/^\circ C \) (\( 2nA/^\circ C \)) and \( 10\mu V/^\circ C \) (\( 2.5\mu V/^\circ C \)) respectively. Supply voltage rejection ratio is \( 200\mu V/V \) (\( 75\mu V/V \)). Offset current flowing in the input resistor \( R \) contributes to a total equivalent offset voltage of \( \pm 310\mu V \) (\( \pm 66\mu V \)) at the extremes of temperature and supply voltage. From sections 7.2.2(iii) and 7.2.2(vi) a maximum direct voltage of \( 450\mu V \) (\( \pm 270\mu V \)) can be present at the output of the \( Y \) integrator. The total equivalent offset voltage to the comparator circuit is therefore \( \pm 760\mu V \) (\( \pm 336\mu V \)). Now the minimum zero crossing point rate of change of voltage with time is \( 125 V/s \) (when \( V_{in} = 40mV \)) which corresponds to a rate of change of voltage with angle of \( 690\mu V/\text{degree} \). The above total offset voltage results in an angular error of the first trial point of approximately \( 1.1^\circ (0.5^\circ) \). For angle computations from this trial point, the angular error is reduced since \( V_{in} = \Delta s = 150mV \). At the fourth trial point in the locus, where the lowest value of \( V_{in} \) is approximately \( 4 \Delta s \) (\( = 600mV \)) the angular error is less than the angle counters precision.

At the maximum input voltage (7V peak), the output of the pre-amplifier has to change at a rate of \( 0.22V/\mu s \) at the zero crossing point. This requirement is achieved with the \( \mu A702A \) with the compensation circuits shown. A temperature controlled differential amplifier (\( \mu A727B \)), although considerably more expensive than the \( \mu A702A \) would be ideal for its bandwidth and offset current and voltage characteristics. However its slewing rate is not quoted in data sheets. Persistent enquiries indicate that a value better than \( 0.1V/\mu s \) is not to be expected. A possible solution is to use both amplifiers in cascade within the feedback loop.
The total effective noise referred to the input of the pre-amplifier is approximately 40μV^2. Compared to the offset voltages that are produced this can be neglected.
8.1 Total analogue errors

Table 8.1 gives a quantitative listing of all errors occurring in the analogue sections of the system for the temperature range 10°C to 30°C and supply voltage variation of ±1%. These errors are divided into four categories:

(i) Errors that can be considered as offset voltages at the initial condition inputs to the inverse resolver, $V_{IC}$.

(ii) Errors that result in incorrect angle determination, $\delta \theta$.

(iii) Errors that can be considered as occurring in the sample and hold circuits S2X and S2Y, $V_{S2}$.

(iv) Errors occurring in sample and hold circuits S1X and S1Y, $V_{S1}$.

Error values in the X and Y channels are denoted by $x$ and $y$ respectively. Where applicable, the listing gives maximum worst case values followed by typical values shown in brackets. In each case the values apply for the temperature range and supply voltage variation given above. For each type of error, and respective comment, reference is made to the relevant sections of the thesis.

The maximum total worst case and typical positive and negative error values are given at the end of each column in Table 8.1. In each
case these are obtained by adding all positive values in a column assuming negative values in that column are zero, and vice versa.

The overall worst case when the error voltages in all columns are directly added gives equivalent voltage errors of 49.3mV (35.0mV) in the Y channel and 40.8mV (27.5mV) in the X channel. The quadrature sum of these voltages is 64mV (44.0mV) which is greater than the value allocated in section 6.1.

8.2 Modifications

One of the major sources of error in each channel is amplifier gain error. In Fig 5.2, amplifiers $a_x^2$ and $a_y^2$ are used only once per branch of the locus, that is when setting the output voltages of sample and hold circuits S2X and S2Y to the voltage co-ordinates of the starting pole. The removal of these amplifiers is to be recommended, resulting in the improved figures given in Table 8.2. The sampling time (0.1s) of S2X and S2Y is so long that the increase in time constant, (due to the potentiometers source resistance plus analogue switch resistance) can be ignored. The retention of the analogue switches at the inputs of S2X and S2Y is advised. Direct connection of the input multiplexers to the sample and hold circuits will result in increased drift due to leakage current.

A considerable improvement results from inserting variable resistors $P_{x2}^2$, $P_{y2}^2$ as shown in Fig 5.2. In the X channel, $P_{x2}^2$ is used to equalise the gains from the output of S2X and the input of $a_{x1}$ to the output of $a_{x4}^4$. Similarly $P_{y2}^2$ is employed to equalise the gains of the respective circuits in the Y channel. It is noted that this gain adjustment is not so effective in the overall Y channel due to the inclusion of amplifiers $a_{y7}^7$ and $a_{y8}^8$ when double poles are set up.
The results from this modification, including the removal of amplifiers $a_{x2}$ and $a_{y2}$, are given in Table 8.2.

A final modification incorporated in the instrument is the inclusion of variable resistors $P_{1x}$, $P_{1y}$ shown in Fig 5.2. These are adjusted to give unity gain from the input of $S1X$ ($S1Y$) to the input of $S2X$ ($S2Y$), the inputs from the resolver being disconnected and connected to ground. The resultant overall channel errors are given in Table 8.2.

The phase error aperture, $x$, chosen in section 6.1 is ±1.15°. From section 5.4.2, the angular accuracy of the instrument is ±$(x + k)$ where $k$ is the counter error and equals ±0.54. From Table 8.2, the maximum angular error contributed by the analogue sections of the system is estimated to be ±0.25° at any point in the locus. Summing these errors, the overall maximum instrument angular error is less than 2°.

The reduction of errors due to the modifications discussed above suggest an adjustment of the earlier specification. Retaining the original value for $\Delta s (=150mV)$, and noting that the worst case total sum of error voltages $e_o$ is roughly 30mV, the value of $E (= e_o / \Delta s)$ is 0.2. From Fig 5.11, a suitable value of phase error aperture is ±0.81°. The overall angular error of the instrument reduces to ±1.6°.

In Table 8.2 the values for $e_o$ are derived from worst case maximum and typical values at the extremes of temperature and power supply variation. In each column all errors have been added assuming no cancellation occurs. This is a very pessimistic case. The search vector magnitude $\Delta s$ was made variable over a range of 50mV to 200mV by means of a front panel potentiometer. At the temperature at which the instrument's amplifiers have been balanced, satisfactory operation should
be achievable at the lower value. At the limits of the temperature and power supply ranges the system should work successfully for a value of Δs less than 150mV.

8.3 Design of logic networks 1 and 4 (see Fig 5.8)

Having established the allowable phase error aperture, the logic networks for Fig 5.8 can be designed. An aperture of ±0.81° corresponds to a count of ±9 digits. The corresponding truth tables for logic networks 1 and 4 are given on page 170. For a phase error between -1 and -9 digits, the output of logic network 1, \( Z_{n1} \), must be at logical '0'. For a phase error between 0 and +9 digits, the output of logic network 4, \( Z_{n4} \), must be at logical '1'. The following Boolean expressions are obtained:

\[
Z_{n1} = \overline{D_o + C_o B_o A_o}
\]

\[
Z_{n4} = \overline{D_o C_o + D_o B_o}
\]

The resulting logic network diagrams are shown in Fig 8.1.
<table>
<thead>
<tr>
<th>Circuit element or operating condition</th>
<th>Type of error</th>
<th>$V_{IC}$</th>
<th>$\delta \theta$</th>
<th>$V_{S2}$</th>
<th>$V_{S1}$</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>$a_{x1}$, $a_{y1}$, $a_{x4}$, $a_{y4}$, $a_{x7}$, $a_{y8}$</td>
<td>Offset</td>
<td>±2.32</td>
<td>±3.63</td>
<td></td>
<td></td>
<td>Results in locus displacement. Extra iterations in finding first and second true points in the locus. (3.1), (3.2.1)</td>
</tr>
<tr>
<td>(6.2.3)</td>
<td>Gain</td>
<td>+10.8</td>
<td>+18.0</td>
<td></td>
<td></td>
<td>Estimated to be $+0.1^\circ$ at any point in the locus. (3.2.2)</td>
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<tr>
<td>$a_{x4}$, $a_{y4}$</td>
<td>Gain</td>
<td></td>
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<td>+0.34° per angle measured</td>
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<tr>
<td>(6.2.3)</td>
<td>Offset</td>
<td>±0.6</td>
<td>±0.6</td>
<td>±0.6</td>
<td>±0.6</td>
<td>No locus displacement. Extra iterations in finding first true point. (4.2)</td>
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<tr>
<td>$a_{x2}$, $a_{y2}$</td>
<td>Gain</td>
<td>±3.6</td>
<td>±3.6</td>
<td>±3.6</td>
<td>±3.6</td>
<td>Ditto (4.1.3)</td>
</tr>
<tr>
<td>(6.2.1)</td>
<td>Offset</td>
<td></td>
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<td>±2.0</td>
<td>±2.0</td>
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<td>Circuit element or operating condition</td>
<td>Type of error</td>
<td>$V_{IC}$</td>
<td>$\phi$</td>
<td>$V_{S2}$</td>
<td>$V_{SL}$</td>
<td>Comments</td>
</tr>
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<tr>
<td>S2X, S2Y (6.4)</td>
<td>Offset</td>
<td></td>
<td>$\pm 0.35$</td>
<td>$\pm 0.35$</td>
<td></td>
<td>No locus displacement. Extra iterations in finding first and second true points in the locus. 4.1.1(i) and (ii)</td>
</tr>
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<td>Capacitive feedthrough offset</td>
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<td>$-1.5$</td>
<td>$-1.5$</td>
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<tr>
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<td>Gain</td>
<td></td>
<td>$2\delta V_x = \pm 6.0$</td>
<td>$2\delta V_y = \pm 6.0$</td>
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<tr>
<td></td>
<td>Drift plus dielectric absorption</td>
<td></td>
<td>$-0.34$</td>
<td>$-0.34$</td>
<td></td>
<td>Locus displaced. Extra iterations for first point only. 4.1.1 (iii)</td>
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<td>S1X, S1Y (6.5)</td>
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<td>$\pm 0.35$</td>
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<td>Locus displaced. Extra iterations for first point only. 4.1.2(i) and (ii)</td>
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<td>Gain</td>
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<td>$\pm 3.0$</td>
<td>$\pm 3.0$</td>
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<td></td>
<td>Drift plus dielectric absorption</td>
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<td>$-0.14$</td>
<td>$-0.14$</td>
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<td>Negligible locus displacement. No extra iterations. 4.1.2 (iii)</td>
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<td>Circuit element or operating condition</td>
<td>Type of error</td>
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<td>$\delta \phi$</td>
<td>$V_{S2}$</td>
<td>$V_{S1}$</td>
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<td><strong>Inverse Resolver</strong></td>
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<td>Initial condition setting mode.</td>
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<td>Unequal input and feedback resistances (i)</td>
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<td>Estimated to be $-0.1^\circ$ at any point in the locus. 3.2.2</td>
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<td>$\pm 0.7$</td>
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<td>Locus displaced. Increase in number of iterations for first and second true points. 3.1</td>
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<td>Amplifier offset voltage, leakage current etc (iii)</td>
<td>$\pm 0.5$</td>
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<td>Ditto</td>
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<td><strong>Inverse Resolver</strong></td>
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<tr>
<td>Compute Mode</td>
<td>$R \neq R_y, C \neq C_y$ plus gain error in inverting amplifier. (i)</td>
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<td>*Can be ignored. Tend to cancel. Also compensation is employed. 3.1</td>
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<td>$\pm 0.35$</td>
<td>Variation of comparator threshold</td>
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<td>$\pm 0.02$</td>
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<td>3.1</td>
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<td>Type of error</td>
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<td>$\delta \phi$</td>
<td>$V_{S2}$</td>
<td>$V_{Sl}$</td>
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<td><strong>Resolver</strong></td>
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<td>+0.7sin$\phi$</td>
<td>No displacement of locus. Due to errors in compass, contributes to extra iterations for first true point.</td>
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<td>Amplifier offset voltage, leakage current etc. (iii)</td>
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<td>(0.5sin$\phi$)</td>
<td>7.3.1(ii)</td>
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<td>$R = R_x \neq R_y$, $C = C_x \neq C_y$ plus gain error in inverting amplifier. (i)</td>
<td></td>
<td></td>
<td>-1.7cos$\phi$</td>
<td>-1.7sin$\phi$</td>
<td>Alters heading of search vector by 0.05° which is negligible.</td>
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<td>7.3.2(i)</td>
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<td>Can be ignored. Tends to cancel. Also compensation is employed. 7.3.1(ii)</td>
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<td>Amplifier offset voltage, leakage current etc. (iii)</td>
<td></td>
<td></td>
<td>(0.25cos$\phi$)</td>
<td>(0.25sin$\phi$)</td>
<td>Locus not displaced. Due to errors in compass, contributes to extra iterations in finding first true point.</td>
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<td>Offset voltage in inverting amplifier. (iv)</td>
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<td>(0.25)</td>
<td>(0.25)</td>
<td>4.1.1(i) and 7.3.1(ii)</td>
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<td>(v)</td>
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<td>(0.1sin$\phi$)</td>
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<td>Type of error</td>
<td>( V_{IC} )</td>
<td>( \delta \phi )</td>
<td>( V_{S2} )</td>
<td>( V_{Sl} )</td>
<td>Comments</td>
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<td>+18.8</td>
<td>+18.9</td>
<td>+3.4</td>
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<td>Worst Case</td>
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<td>( \pm 0.084^\circ )</td>
<td>-11.7</td>
<td>-11.8</td>
<td>-3.8</td>
</tr>
<tr>
<td>Totals</td>
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<td>(+20.3)</td>
<td></td>
<td>(+13.2)</td>
<td>(+13.2)</td>
<td>(+1.5)</td>
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<td>(-1.9)</td>
<td>(-2.3)</td>
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<td>(-6.0)</td>
<td>(-6.0)</td>
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Locus not displaced.
Contributes to extra iterations in finding first true point.

4.1.1(i)
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<th>$V_{IC}$</th>
<th>$\delta\theta$</th>
<th>$V_{S2}$</th>
<th>$V_{SL}$</th>
<th>Worst case totals</th>
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<td>$-3.8$</td>
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<td>$+20.3$</td>
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<td>$+1.5$</td>
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<td>$M_1$</td>
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<td>$-1.4$</td>
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Modification $M_1$ — removal of amplifiers $a_{x2}$ and $a_{y2}$.  

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<th>$V_{ic}$</th>
<th>$\delta V$</th>
<th>$V_{s2}$</th>
<th>$V_{s1}$</th>
<th>Worst case totals</th>
<th>$\sqrt{x_1^2 + y_1^2}$</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$x$ mV</td>
<td>$x$ mV</td>
<td>$x$ mV</td>
<td>$y$ mV</td>
<td>$x$ mV</td>
<td>$y$ mV</td>
<td>$x_1$ mV</td>
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<tr>
<td>$+ 3.6$</td>
<td>$+12.0$</td>
<td>$- 3.4$</td>
<td>$- 4.8$</td>
<td>$+25.6$</td>
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<td>$42.8$</td>
<td>Total locus displacement:</td>
</tr>
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<td>$M_2$ and $M_1$</td>
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<td>$y = +14.7$ mV, $-8.2$ mV</td>
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<td>$[+ 1.4]$</td>
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<td>$[- 1.8]$</td>
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<td>$+10.0$ mV, $-3.4$ mV</td>
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<td>$x = + 6.8$ mV, $-7.0$ mV</td>
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<td>$+ 2.4$ mV, $-3.0$ mV</td>
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<td>Angular error as before $\pm 0.25^\circ$</td>
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<td>$M_3$, $M_2$</td>
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<td>Less iterations taken</td>
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<td>and $M_1$</td>
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<td>Same displacement and angular error as above</td>
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<td>$(- 8.1)$</td>
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</table>

Modification $M_1$ — removal of amplifiers $a_{x2}$ and $a_{y2}$.

" $M_2$ — inclusion of variable resistors $P_{x2}$ and $P_{y2}$

" $M_3$ — " " " " " $P_{x1}$ " "$ P_{y1}$
Truth tables for logic networks 1 and 4.

<table>
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<th>( Z_{n4} )</th>
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<td>+15</td>
<td>0</td>
<td>1 1 1 1</td>
<td>0</td>
</tr>
</tbody>
</table>

- 170 -
Fig 8.1  Logic diagrams for networks 1 and 4.
**CHAPTER 9**

**COMMISSIONING AND RESULTS.**

**9.1 Setting up procedure**

Below are given the procedures to be carried out in order to put the constructed instrument into operation. Since signal transmission in some circuits occurs only at specific times in the computation, it is necessary to set some of the analogue switches to a permanently closed state. Several disconnections have to be made and a connecting link should be fitted at the requisite point in the circuit in any commercial machine. These connecting links are indicated in the circuit diagrams by crossed circles: \(-\bigcirc-\).

**9.1.1 Amplifier output zero setting.**

(i) Disconnect the control logic feedback paths \(G_o, Q_r\) and \(Q'\) (Fig 5.3) and also the recirculation pulse line.

(ii) Disconnect the output lines of monostable MS4 and MS8 (point V) and connect these lines to logical '1', i.e. +5V.

(iii) Disconnect inputs \(X'\) and \(Y'\) of amplifiers \(a_{x5}\) and \(a_{y5}\) (Fig 5.2) respectively from the resolver circuit. Connect these inputs to signal ground.

(iv) Set up the front panel switches for a pair of complex poles. This connects the first potentiometer wiper to the junction of switches \(A_{lx}\) and \(B_{lx}\) (Fig 5.2) and the second potentiometer wiper to the junction of \(A_{ly}\) and \(B_{ly}\).

(v) Set the first two input potentiometers to a dial reading of 0.15.
(vi) Set the potentiometers' supply voltage to zero.

(vii) Switch on, and after allowing fifteen minutes as a warming-up period operate the start button. This sets the Al output derived from shift register SRA (Fig 5.3) to the logical '1' state. SRB is non-operative since the input of MS5 is connected to logical "1". There is now a transmission path via $a_{x2}$, $S2X$, $a_{x5}$, $a_{x6}$ and the corresponding elements in the Y channel.

(viii) In the X channel adjust amplifier outputs to zero volts in the order stated above.

(ix) Repeat the procedure for the respective circuit elements in the Y channel.

(x) Disconnect the junction of S1X and $a_{x4}$ from S2X (Fig 5.3) and connect this junction to signal ground.

(xi) Connect the input of MS5 to the output of MS4 and connect the remaining outputs of MS4 to logical '0'.

(xii) Operate the start button. This sets the Bl output of SRB to logical '1', thus closing analogue switches Blx and Bly. A1x and Aly are open.

(xiii) Adjust for zero output voltage the remaining amplifiers (except $a_{y7}$ and $a_{y8}$) in the following order:

$A_{x1}$, $A_{x3}$, $A_{x4}$, $A_{y1}$, $A_{y3}$, $A_{y4}$, X integrator, Y integrator, sign inverter and pre-amplifier. The comparator (LM206) is adjusted to be just at the logical '1' level.

Zero setting of amplifiers $a_{y7}$ and $a_{y8}$.

The circuit connections given above are retained.

(i) Disconnect the normally grounded 'Preset B2' input of shift register SRB and connect to logical '1'.

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(ii) Operate the stop button. Only analogue switch AB1 is now closed, connecting amplifier $a_{y7}$ to the wiper of the second potentiometer.

(iii) Adjust the output of $a_{y7}$ to zero volts.

(iv) Adjust the output of $a_{y8}$ to zero volts.

(v) Re-connect the 'Preset B2' input of SRB to ground.

9.1.2 Gain setting procedure.

The circuit connections of section 9.1.1 are retained.

(i) Connect the grounded input of amplifier $a_{x4}$ to the input of amplifier $a_{x1}$ (Fig 5.2). Re-connect all outputs of MS4.

(ii) Restore the input potentiometers' supply voltage, and set the first potentiometer to a known voltage.

(iii) Operate the start button and adjust variable resistor $P_{x2}$ until the output of $a_{x4}$ is zero.

(iv) Adjust variable resistor $P_{x1}$ for unity gain from the input of SIX to the output of $a_{x6}$.

(v) Repeat the above procedures for the respective elements in the Y channel, with the known voltage being set up on the second input potentiometer.

(vi) Re-connect all broken links in the system with the exception of the control logic feedback paths, i.e. $G_o$, $Q_r$ and $\overline{Q'}$, and the recirculation pulse line.

9.1.3 Cancellation of capacitive feedthrough voltages in the inverse resolver and resolver

For this adjustment a test circuit is required consisting of a six stage shift register (SRT) and one NAND gate (see Fig 9.1). The shift line of SRT is connected to a pulse generator set to a
frequency of approximately 100Hz. The first stage of SRT can be set to logical '1' by means of the switch shown.

(i) Disconnect line V from the output of MSI8 and connect instead to the first stage of SRT.

(ii) Disconnect lines T and U (Fig 5.5) from the outputs of MSI1 and gate 25 respectively. Connect these lines to the points shown in Fig 9.1.

(iii) Disconnect the X and Y inputs of the inverse resolver (Fig 5.2) from amplifiers $a_{x4}$ and $a_{y4}$. Connect these inputs to ground.

(iv) Connect the $A_s$ input of the Y integrator to ground.

(v) Set the first stage of SRT to logical '1' and switch on the pulse generator. This sets the inverse resolver successively to the initial condition, compute and hold modes. These are followed by the same modes for the resolver. Viewed on a d.c. coupled oscilloscope the outputs of the X or Y integrators will appear as in Fig 9.2. For the inverse resolver the two potentiometers in the gate driving circuit of input V (Fig 7.6) are adjusted until the outputs of the X and Y integrators are as small as possible in the compute phase. The adjustment is carried out as follows:

(vi) Adjust the potentiometer that is coupled to R until the output of the X integrator (viewed on the oscilloscope) is zero at the start of the compute phase. i.e. the waveform appears sinusoidal in nature. This means that all the offset voltage is being generated in the Y integrator.

(vii) Transfer the oscilloscope to the output of the Y integrator.

(viii) Adjust the potentiometer, that is coupled to $S$, until the output of the Y integrator is zero at the start of the
Fig 9.1 Test circuit for cancellation of capacitive feedthrough voltages.

Fig 9.2 Typical waveforms at the outputs of the X or Y integrators.
(ix) Increase the CRO sensitivity and repeat (vii) and (viii) until the integrator outputs are as small as possible.

(x) Carry out the same procedure for the resolver, employing the potentiometers in the gate driving circuit connected to line U.

(xi) If necessary repeat all the above steps until the residual waveforms in the compute phases are as small as possible. In practice a residual amplitude of less than 0.1mV peak-to-peak is readily achieved.

(xii) Remove the test circuit and re-connect all broken links in the system, including the logic feedback paths G_o, Q_r, Q'.

The instrument is now operational.

9.1.4 Adjustment of internal clock generator frequency (2.048MHz).

(i) Set up the front panel switches and the first input potentiometer for a single pole at the origin.

(ii) Connect the CRO X and Y inputs to the respective instrument outputs, i.e. the outputs of sample and hold circuits S1X and S1Y respectively.

(iii) Operate the start button. The instrument should plot a line.

(iv) Adjust the clock generator trimmer capacitor (see Fig 5.13) until the line is horizontal, increasing the CRO 'Y' deflection sensitivity as required.

(v) The instrument is now correctly adjusted for plotting 180° loci.
9.2 Results.

At room temperature (22°C) the drift in the sample and hold circuits was measured and found to be:

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Measured drift</th>
<th>Calculated drift at 30°C</th>
</tr>
</thead>
<tbody>
<tr>
<td>S2X</td>
<td>0.9μV in 30ms</td>
<td>224μV (44μV) in 30ms</td>
</tr>
<tr>
<td>S2Y</td>
<td>1.7μV in 30ms</td>
<td>&quot;</td>
</tr>
<tr>
<td>S1X</td>
<td>1.0μV in 30ms</td>
<td>23μV (5μV) in 30ms</td>
</tr>
<tr>
<td>S1Y</td>
<td>0.2μV in 30ms</td>
<td>&quot;</td>
</tr>
</tbody>
</table>

After allowing for the increased drift at 30°C, the results obtained are well within the calculated typical values. The larger value of drift in sample and hold circuit S1X, compared to S1Y, is due to the amplifier employed having a high input current. Nevertheless this input current is just within the maximum value quoted by the manufacturer (20pA at 25°C).

Capacitive feedthrough of the gate driving signal resulted in an offset voltage less than 1mV in S2X and S2Y, and not greater than 0.1mV in S1X and S1Y.

The drift in the resolver circuit in the hold mode was found to be 7mV. Allowing for the increase in this value at 30°C, the result obtained is well within the estimated value (20μV) given in section 7.3.3. Capacitive feedthrough of the gate driving signal at the end of the compute mode resulted in offset voltages of 1.1mV and 1.2mV at the outputs of the X and Y integrators respectively.

The switching times of the MOSTs and their associated gate driving circuits were, in the main, within the calculated values given
For the worst measured case, the results were as follows:

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Measured value</th>
<th>Calculated value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Closing time of series analogue switch</td>
<td>55ns</td>
<td>65ns (105ns)</td>
</tr>
<tr>
<td>Opening time of shunt analogue switch</td>
<td>120ns</td>
<td>115ns (155ns)</td>
</tr>
<tr>
<td>Opening time of series analogue switch</td>
<td>180ns</td>
<td>200ns (240ns)</td>
</tr>
<tr>
<td>Closing time of shunt analogue switch</td>
<td>220ns</td>
<td>224ns (264ns)</td>
</tr>
</tbody>
</table>

The values shown in brackets are the values resulting from the addition of a further 40ns as recommended in section 7.6. Thus it is reasonable to assume that over the range of production spread of the transistors and MOSTs, switching times will be within these values. The switching times of the MOSTs were within the maximum values estimated by the manufacturers (measured turn-on time = 15ns, measured turn-off time = 40ns).

In the comparator circuit particular attention has to be given to ensuring correct earthing and power supply decoupling of the pre-amplifier in order to prevent instability. The total delay time between the input of the pre-amplifier and the output of the monostable, for a square wave input of 200mV peak-to-peak amplitude was 120ns. This is within the calculated value (140ns) given in section 7.6, and well within the recommended value of 200ns that allowed for the approximate nature of the analysis used.
9.3 Loci displayed on the cathode ray oscilloscope

Plate 1 to Plate 18 show CRO displays of various root loci obtained with the constructed instrument. The values given in the transfer functions are readings from the input potentiometers calibration dials. For all loci shown the search vector magnitude was less than 100mV. The phase error aperture was set to ±0.8°.

When a locus has a pronounced change in direction in any of its branches more iterations are taken by the system in searching for the new direction. This is shown up on the CRO by an increase in the spot brightness.

Plate 1 shows the locus of a pole at the origin. The vertical line represents the y axis.

In Plate 2 the vertical line is the locus of a double pole at the origin. For this case it is necessary to separate the two poles by an amount greater than the discriminator gate G threshold. The double pole is set up as a complex pair, having x and y potentiometers set to dial readings of zero and 0.01 respectively. The CRO deflection sensitivity for this locus is 2V/cm.

By adjusting the clock generator frequency such that for a single pole at the origin the line plotted lies at an angle slightly greater than 180° (say 180.5°), break points occurring in loci can be detected. This is shown in Plate 3 where the root locus of two single poles on the real axis has been obtained.

Plate 4 shows the expected locus for a triple pole on the real axis, at the point x = -0.15. As with double poles these have been separated by a dial reading of 0.01. Plate 5 shows the effect of moving one of the poles to the point x = -0.5. Plate 6 shows how
a zero can be employed to bring the locus away from the unstable right hand half of the s-plane.

Plates 7, 8 and 9 show the effect of moving the relative pole positions in a system having a complex pair of poles and a single pole in its transfer function. Plate 8 shows the locus used as an example in Chapters 3 and 4.

Plate 10 shows the plot of a system with a particularly difficult breakpoint, the true locus being shown in the inset.

Plate 11 is the root locus for a system having a double pole and two single poles on the real axis in its transfer function. The introduction of a zero (at x = -0.7) changes the shape of the locus to that shown in Plate 12.

Plates 11 and 13 illustrate the effect of adding a pair of complex zeroes to a system. The branches of the locus associated with the double pole are radically influenced by the presence of the zeroes.

Plates 14 and 15 show the effect of moving the position of one pair of poles. The marked changes which result illustrate the difficulties which may be encountered in attempting to "sketch" a locus.

The loci given in Plate 15 through to Plate 18 have the same denominator in their transfer functions. The effect of adding pair(s) of complex zeroes to the system depicted by Plate 15 is clearly shown. In Plate 18 the full capability of the constructed instrument is being exploited, i.e. six poles and four zeroes.
PLATE 1

\[ F(s) = \frac{1}{s} \]

PLATE 2

\[ F(s) = \frac{1}{s^2} \]
PLATE 3

\[ F(s) = \frac{1}{s(s + 0.5)} \]

PLATE 4

\[ F(s) = \frac{1}{(s + 0.15)^3} \]
Plate 5

\[ F(s) = \frac{1}{(s + 0.5)(s + 0.15)^2} \]

Plate 6

\[ F(s) = \frac{(s + 0.3)}{(s + 0.5)(s + 0.15)^2} \]
\[ F(s) = \frac{1}{(s + 0.6)[(s + 0.6)^2 + 0.8^2]} \]
PLATE 9

\[ F(s) = \frac{1}{s \left[ (s + 0.5)^2 + 0.33^2 \right]} \]

PLATE 10

\[ F(s) = \frac{s + 0.3}{s^2} \]
PLATE 11

\[ F(s) = \frac{1}{(s + 0.15)^2(s + 0.3)(s + 0.5)} \]

PLATE 12

\[ F(s) = \frac{(s + 0.7)}{(s + 0.15)^2(s + 0.3)(s + 0.5)} \]
PLATE 13

\[ F(s) = \frac{\left( (s + 0.5)^2 + 0.5^2 \right)}{s^2(s + 0.3)(s + 0.45)} \]

PLATE 14

\[ F(s) = \frac{1}{s^2(s + 0.3)(s + 0.45)\left( (s + 0.6)^2 + 0.3^2 \right)} \]
PLATE 15

\[ F(s) = \frac{1}{s^2(s + 0.3)(s + 0.45)\left[(s + 0.4)^2 + 0.3^2\right]} \]

PLATE 16

\[ F(s) = \frac{\left[(s + 0.1)^2 + 0.2^2\right]}{s^2(s + 0.3)(s + 0.45)\left[(s + 0.4)^2 + 0.3^2\right]} \]
PLATE 17

\[ F(s) = \frac{[s + 0.8]^2 + 0.7^2]}{s^2 (s + 0.3)(s + 0.45)(s + 0.4)^2 + 0.3^2} \]

PLATE 18

\[ F(s) = \frac{[s + 0.8]^2 + 0.7^2][s + 0.5]^2 + 0.8^2}{s^2 (s + 0.3)(s + 0.45)(s + 0.4)^2 + 0.3^2} \]
Plate 1 appears to show an almost perfect trace. However if the y gain of the CRO is increased, the plot which results is shown in Plate 19. The phase error aperture set by the phase error comparison circuit (section 5.2.7) is indicated, and it is seen that the locus is lying within a phase error band better than ±0.2°. This result is to be expected since the phase error at any point, even if it is less than the phase error aperture (ε) is still added to the contents of counter 1 and modifies the heading of the next trial point. The process is shown in more detail in Fig 9.3, where an exaggerated phase error aperture is shown (±20°). For a single pole at the origin the set off direction is determined precisely, since the angle computation phase consists only of the subtraction of π from counter 1. Assume an offset voltage exists that plots the first trial point just within the phase error aperture (a₁).

From (a₁) the angle to the pole is determined, and the first phase error $\varphi_1 = -\varphi - \pi = -200^\circ - 180^\circ = -20^\circ$ being equal to $\varepsilon$, point a₁ is displayed on the CRO. However counter 1 now contains the angle 160°. To the x and y co-ordinates of point a₁ are now added the values $\Delta s \cos 160^\circ$ and $\Delta s \sin 160^\circ$ respectively to generate a point b. To b is added the offset voltage to give a new trial point b₁. This point is within the phase error aperture, but its phase error is added to the contents of counter 1 to give a further trial point c₁. Continuing in this fashion the result shown in Fig 9.3 agrees with the plot shown in Plate 19.

Plate 10 illustrates the effect of finite phase error aperture at a breakpoint. Fig 9.4 shows the correct 180° locus and the 179° and 181° phase angle loci. It is seen that there is a high sensitivity region in the vicinity of the breakpoint. Assume
PLATE 19. Root locus for a single pole at the origin, showing that the locus is lying well within the phase error aperture.

X deflection = 0.5V/cm, Y deflection = 10mV/cm.
Fig 9.3. Diagram showing successive plotted locus points $a_1$, $b_1$, $c_1$, etc lying well within the phase error aperture.
the instrument phase error aperture $\epsilon$ is $\pm 1^\circ$. From the double pole at the origin the top branch of the locus will tend to follow the $179^\circ$ contour. This is because, from a true point in the locus, a subsequent new trial point will lie outside the circle. By successive iterations the system corrects for phase error until the tip of the search vector is within the phase error aperture.

The search vector continues along the branch in this fashion until a point such as A is reached. From A a trial point B is taken at the last computed heading. At B the phase error is less than $\epsilon$, the search vector heading will hardly alter and thus a subsequent trial point C is plotted. The process continues, the plot moving almost on a straight line until a trial point falls outside the phase error aperture. At this point (having crossed the $180^\circ$ phase angle locus) the phase error is reversed so that the search vector now swings away from the circle. Since each successive phase error is still very small the system iterates many times until the trial point comes within the aperture at the point Q. The remainder of the $181^\circ$ locus is then plotted.

Similarly, the lower branch of the locus associated with the double pole will tend to follow the $181^\circ$ contour until it reaches a trial point at $N'$. Again many iterations are executed to bring the trial point within the phase error aperture. The system then plots the remainder of the $179^\circ$ locus.

Even if the phase error aperture were zero it would not be possible to plot the complete locus. Fig 9.5 illustrates the breakpoint procedure described earlier and shows how, even with a finite phase error aperture, it is possible to plot a close approximation to the complete locus.
Fig 9.4. Phase angle loci for a system having a transfer function \( \frac{s + a}{s^2} \), showing position of trial points in the \( \pm 1^\circ \) phase error aperture.

Fig 9.5. Diagram showing phase error band (shaded) when system is adjusted for plotting \( 181^\circ \) loci.
If with the error of ±1°, the clock generator frequency is set so that the system plots the 181°±1° locus, the top branch from the double pole at the origin swings round inside the circle and terminates on the zero. This is provided that the search vector magnitude is not too large. The lower branch swings outside the circle and plots a locus within the shaded area lying outside the circle. Alternatively the 179°±1° locus can be similarly obtained. Thus the smaller the phase error aperture, the nearer to the true 180° contour will be the plotted locus. In Plate 10, the phase error aperture is 0.8°.

Plate 9 is exhibiting the effect of plotting 181° loci. The 181° locus has a less pronounced curve in the lower branch than in the upper branch which dips more towards the horizontal axis. This accounts for the increase in brightness in the upper branch of the locus.

Due to the time taken in storing the voltage co-ordinates of the starting poles there is an increase in brightness at these points. Also when a branch of a locus terminates on a zero or has a value that exceeds the dynamic range of the instrument, there is an increase of brightness due to the time taken before switching to the next pole.
DISCUSSION AND CONCLUSIONS.

The work has demonstrated that an effective and useful tool can be constructed, the photographic plates obtained speak for themselves. The fact that the root locus of a system having six poles and four zeroes can be displayed in roughly nine seconds indicates the power of special purpose computers.

The work provides for the first time an analysis of certain errors that arise in automatic root locus computers employing adaptive hybrid techniques. The design considerations given make it possible to design an instrument to any specification.

In passing it is interesting to note that the behaviour of the system shows similarities to that observed in beam-rider missiles. The plots shown in Plate 19 and Fig 9.3 exhibit a type of "hunting" which is a characteristic of such systems.

The performance of the constructed instrument falls within the design criteria and compromises that have been proposed. The limitations that occur are to be expected within the context of the design specification. The fact that the system has no precedent implies that the specification has been of an exploratory nature.

A small change in gain in a control system does not have much effect upon its performance, but at a breakpoint this change has a marked effect in the root locus. The fact that the instrument's performance is limited in high sensitivity regions is of little importance.
The limitations arising from system errors are:

(i) The instrument has limited angular accuracy (gain error contributing partly to this).

(ii) An approximation to the shape of the locus is obtained at breakpoints.

(iii) There is a minimum value to the search vector magnitude resulting in a minimum spot density.

(iv) The locus is displaced from its true position.

All these limitations can be reduced at increased cost, by employing better quality circuit elements. The system phase error aperture can be reduced by adding extra counter stages and increasing the clock frequency. For this to be effective delays in the logic circuits, gate driving circuits and the comparator have to be reduced.

With the current availability (in limited variety) of Schottky TTL elements, and compatible TTL to MOST level shifting integrated circuits, shorter delays can be easily achieved but at increased cost. Reference 38 describes a very fast zero crossing point detecting comparator which employs an expensive operational amplifier. The counter circuits employed are capable of operating at clock frequencies up to about 10MHz and should not require any changes. A further reduction in logic circuit delays could be achieved by employing emitter coupled logic elements, but this would result in extensive replacement of circuits.

Within the present year integrated circuit sample and hold circuits to which storage capacitors are added externally have become available. These circuits are directly operated from TTL voltage levels. Although a little more expensive than the type
employed in the constructed instrument the extra price adequately off-sets the additional wiring cost in any commercial instrument. The only disadvantage is that, to date, the manufacturers cannot quote a value for offset voltage drift in this unit.

Additional features that can be added to the basic instrument are the determination of gain, $K$, at points in the locus and the facility for plotting root loci of systems having pure time delay. It can be shown that at a breakpoint, the value of $K$ passes through a maximum. Comparing the value of gain measured at a true point with the value obtained at the previous true point in the locus, provides an alternative breakpoint procedure.

With the recent drastic price reductions of digital integrated circuits an all digital version of the root locus computer becomes attractive. The equivalent operations of storing the values of the starting poles and updating the locus can be carried out very rapidly. Moreover problems associated with offset voltage drift and gain error do not arise and there are no adjustments on test to be carried out. From work recently carried out in the field of digital integrators by R.E.H. Bywater and P.K. Warrick (Department of Electronic and Electrical Engineering, University of Surrey) under the direction of Professor W.F. Lovering, a digital version of the inverse resolver/resolver is available. With these integrators, specifically designed for use in a simple harmonic motion loop, a frequency of 400Hz with 12 bit amplitude precision is achievable.

The instrument described in this thesis has been patented jointly by the author, Dr. S.E. Williamson and Professor W.F. Lovering, and was successfully demonstrated at the 1971 Physics Exhibition.
A costing independently arrived at by an interested manufacturer supports the author's estimate of a market price of approximately £1,200 for a commercially produced instrument.
Effect of non-ideal amplifier frequency response in computing amplifiers employed in a simple harmonic motion loop.

A1.1 The Integrator

From Fig A1.1 assuming the amplifier input impedance is very high, we have:

\[
\frac{v_i(s) - v_x(s)}{v_o(s)} = \frac{[v_x(s) - v_o(s)]sC}{R}
\]  (A1.1)

\[
v_o(s) = -A(s)v_x(s)
\]  (A1.2)

If the open loop gain of the amplifier is defined by a first order lag (which is true for the amplifiers employed in the present application), then

\[
A(s) = \frac{K}{1 + s\tau_a}
\]  (A1.3)

where \( K \) is the open loop gain at very low frequencies, and \( \tau_a = 1/2\pi f_a \); \( f_a \) being the frequency where \( |A| = K/\sqrt{2} \).

From equations A1.1, A1.2 and A1.3:

\[
\frac{v_o(s)}{v_i(s)} = \frac{-K}{s^2\tau_a + s(K\tau + \tau + \tau_a) + 1}
\]  (A1.4)

where \( \tau = CR \).

For \( K \gg 1 \):

\[
\frac{v_o(s)}{v_i(s)} \approx \frac{-K}{s^2\tau_a + sK\tau + 1}
\]  (A1.5)
A1.2 The sign inverting amplifier Fig(A1.2)

Adopting the same procedure as above, and assuming $K \gg 1$
we obtain

$$\frac{v_o(s)}{v_i(s)} = \frac{-K_i}{K_i + 2s \tau_i} \quad (A1.6)$$

where $K_i$ is the amplifier open loop gain at very low frequencies,
and $\tau_i = 1/2\pi f_i$; $f_i$ being the frequency where the open loop gain
magnitude is $K_i/\sqrt{2}$.

A1.3 Approximate analysis of effect of amplifier frequency response
in a simple harmonic motion loop Fig(A1.3)

Applying the results obtained in sections A1.1 and A1.2
above, to the circuit of Fig A1.3:-

$$V_o(s) = V_i(s) \left[ \frac{-K^2 K_i}{(K_i + 2s \tau_i)(s^2 \tau_a + s K + 1)^2} \right] \quad (A1.7)$$

At the summing point $V_o(s) = V_i(s)$, and re-arranging equation (A1.7)

$$V_o(s) \left\{ 1 + \frac{K^2}{\left[ \frac{1 + 2s \tau_i}{K_i} \right]^{1/2} \left( \frac{s + s \tau_a}{s + s K + 1} \right)^{1/2}} \right\} = 0 \quad (A1.8)$$

Extracting the roots of the quadratic expression in $s$:

$$2s = - \frac{K}{\tau_a} \pm \frac{K}{\tau_a} \left( 1 - \frac{4\tau_a}{K^2 \tau} \right)^{1/2}$$

For $K \gg 1$, and $K^2 \gg \tau \tau_a$ we obtain

$$\left( \frac{s^2 + s K + 1}{\tau_a \tau_a} \right)^{1/2} \left( s + \frac{K}{\tau_a} \right) \left( s + \frac{1}{K \tau} \right) = \frac{K}{\tau_a} \left( 1 + \frac{s \tau_a}{K} \right) \left( s + \frac{1}{K \tau} \right)$$

Substituting in equation A1.8

$$V_o(s) \left\{ 1 + \frac{1}{\left[ \frac{1 + 2s \tau_i}{K_i} \right]^{1/2} \left( \frac{s + s \tau_a}{s + s K + 1} \right)^{1/2}} \right\} = 0$$
The damping factor $\zeta$ is zero for the case

$$\tau = \tau_a + \frac{\tau_i K}{K_i}$$

From equations A1.9 and A1.10

$$\zeta = 2\pi f_{\text{SHM}} K \left[ 1 - \frac{K}{K_i} \cdot \frac{f_{\text{SHM}}}{f_i} - \frac{f_{\text{SHM}}}{f_a} \right]$$

Alternatively

$$\zeta = 2\pi f_{\text{SHM}} \left[ 1 - \frac{f_{\text{SHM}}}{f_i} - \frac{f_{\text{SHM}}}{f_{\text{al}}} \right]$$

where $f_{\text{il}}$ and $f_{\text{al}}$ are very nearly the frequencies where the open loop gains of the amplifiers concerned have fallen to unity.

For the amplifiers employed in each integrator (Analog Devices 40K), $f_a = 20\text{Hz}$, and the minimum value of $K$ is $5 \times 10^4$.

For the sign inverter amplifier (LM308A) $f_i = 5\text{Hz}$ and $K_i(\text{min}) = 5 \times 10^4$.

For a value of $f_{\text{SHM}} = 500\text{Hz}$, equation A1.11 gives a value for $\zeta$ of approximately $-8$.

The solution of equation A1.9 is of the form: $V_o(t) = Ae^{8t}\cos\omega t$

where $A$ is the initial condition value. After one period (2ms) $V_o \approx 1.016A\cos\omega t$, i.e. the amplitude error after one cycle $\approx +1.6\%$. 

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Fig Al.1  Integrator circuit diagram.

Fig Al.2  Inverting amplifier circuit diagram.

Fig Al.3  Connection for simple harmonic motion loop.
Methods of reducing effects due to non-ideal amplifier

d frequency response

A2.1 Capacitive compensation in each computing element

Considering the integrator circuit shown in Fig A1.1, if a capacitor C = τa/(1 + K)R is connected across the input resistor R, the second order term in the transfer function is removed. The resulting transfer function is:

\[
\frac{v_o(s)}{v_i(s)} = \frac{-K}{1 + sτ_x + sτ(1 + K)} = \frac{-K}{1 + sKτ} \tag{A2.1}
\]

where τ, τa and K have been defined in Appendix A1.

If the sign inverting amplifier were perfect, the damping factor for the SHM loop would be positive having a value of 1/Kτ (= 2πf_{SHM}/K) which is low.

At any one frequency the sign inverting amplifier can be made to have zero phase shift by connecting a capacitor C_i of suitable value across the input resistor R.

Letting τ_x = C_x R, K_i = the d.c. open loop gain, τ = the amplifier time constant, the transfer function for the sign inverting amplifier is:

\[
\frac{v_o(s)}{v_i(s)} = \frac{-K_i(1 + sτ_x)}{s^2τ_xτ_i + s(τ_x + 2τ_i) + K_i + 2} \tag{A2.2}
\]

Translating to the frequency domain and re-arranging;
\[ \frac{v_o(j\omega)}{v_i(j\omega)} = \frac{-K_i(1 + j\omega\tau_x)}{(K_i + 2 - \omega^2\tau_x\tau_l) \left[ 1 + \frac{j\omega(\tau_x + 2\tau_i)}{K_i + 2 - \omega^2\tau_x\tau_l} \right]} \]  \\

At an angular frequency \( \omega_o \), the phase shift is zero if the imaginary parts of equation A2.3 are equal; from which

\[ \tau_x = \pm \sqrt{\frac{K_i^2 - 8\tau_i^2\omega_o^2}{2\omega_o^2\tau_i}} \]

\[ K_i \pm K_i \left[ 1 - \frac{4\tau_i^2\omega_o^2}{K_i^2} \right] \]

Hence

\[ \tau_x = \frac{K_i}{\omega_o^2\tau_i} \quad \text{or} \quad \frac{2\tau_i}{K_i} \]  \\

The first value is invalid since the gain at the frequency \( \omega_o/2\pi \) will be approximately \( K_i/2 \) (from equation A2.3). The second value is frequency independent due to the approximation made in the Binomial expansion.

The method of capacitive compensation applied to the elements of the SPM loop calls for three adjustments to be made. The method that follows is considered superior, and requires only one adjustment control.
A2.2 Insertion of damping in the simple harmonic motion loop

Fig A2.1 shows the SHM loop where a fraction $k$ of the output of the first integrator is connected to the sign inverting amplifier.

For a summation amplifier having inputs $v_1$ and $v_2$, the transfer function is

$$\frac{v_o(s)}{v_1(s)} = \frac{-K_i}{K_i + 3s\tau_i} (v_1 + v_2)$$

(A2.5)

where as in section A.1, $K_i$ and $\tau_i$ are the open loop low frequency gain and 'break' time constant respectively.

For the circuit of Fig A2.1:-

$$V_o(s) = \left[ \frac{K^2}{(s^2\tau_a + 2K\tau + 1)^2} - \frac{kkK}{s^2\tau_a + 2K\tau + 1} \right] \frac{K_i}{K_i + 3s\tau_i} V_i(s)$$

(A2.6)

At the summing junction $V_o(s) = V_i(s)$

Using the same method and approximations of section A1.3, (i.e. $K >> 1$, $K^2 >> \tau_a$, $K >> \tau_a$, $K >> \tau_i$) we obtain the differential equation:

$$V_o(s) \left( s^2 \left( 1 + \frac{k\tau_a}{K\tau_a} + \frac{3k\tau_i}{K_i\tau} \right) \right) + \frac{s}{\tau^2} \left[ \frac{s^2}{K} - \frac{3\tau_i}{K} - \frac{2\tau_a}{K} + k \left( \frac{\tau_a}{K^2} + \frac{3\tau_i}{KK_i} \right) \right]$$

$$+ \frac{1}{\tau^2} \left( 1 + \frac{1}{K^2} - \frac{K}{K} \right) = 0$$

(A2.7)
For the damping term to be zero:

\[ k \left[ \tau + \frac{\tau_a}{K^2} + \frac{3\tau_i}{K^2 Ki} \right] = \frac{3\tau_i}{Ki} + \frac{2\tau_a}{K} - \frac{2\tau}{K} \]

For the present application \( \tau >> \frac{\tau_a}{K^2}, \tau >> \frac{\tau_i}{Ki} \)

hence

\[ k = \frac{3\tau_i}{Ki} + \frac{2\tau_a}{K\tau} - \frac{2}{K} \]  \hspace{1cm} (A2.8)

Employing the values given in section A1.3, and putting \( \tau = 1/2\pi500 \text{ sec} \), \( k = 0.007 \).

In equation A2.7, the coefficient of \( s^2 \) is very closely equal to unity, and the simple harmonic motion loop frequency is given by \( f_{\text{SHM}} = 1/2\pi \). Thus equation A2.8 can be re-written in the form:

\[ k = \frac{3f_{\text{SHM}}}{Ki f_{\text{SHM}}} + \frac{2f_{\text{SHM}}}{K f_{\text{SHM}}} - \frac{2}{K} \]  \hspace{1cm} (A2.9)
Fig A2.1 Connection for simple harmonic motion loop with damping.
A3.1 Delay Time ($t_{d_r}$) for a ramp input

The step response of the LM206 comparator is shown in Fig A3.1. We assume that the delay time, $t_d$, at the input is due to a simple first order lag at the input, shown by the idealised diagram of Fig A3.2.

For an input step from $+100$ mV to $-2$ mV, the comparator threshold ($=0$ V) is reached in a time $t_d$ of approximately 30 ns. (see Fig A3.1). Thus the input time constant ($=\tau$) is calculated to be 7.7 ns. Employing this value of $\tau$ in determining delay time for different voltage overdrives, gives values agreeing closely with those shown in Fig A3.1.

For an input ramp of $C$ volts/sec, the output response of the input network is given by

$$V_i(s) = \frac{C}{s^2(s + \frac{1}{\tau})}$$

i.e. $$V_i(t) = C(e^{-t/\tau} + \frac{t}{\tau} - 1) \quad (A3.1)$$

In the present application, the maximum output voltage of the SHM loop is 7 volts peak, having a zero crossing rate of change of voltage equal to $7\omega_{SHM}$. This is pre-amplified by a gain of 12 before being applied to the comparator. Therefore $C = 84\omega = 0.25$ V/us.

The pre-amplifier output is limited to be in the range $\pm 2.5$ V by the action of the input diodes (see Fig 7.7).
From Fig A3.3, \( V_{\text{in}} \) reaches the nominal comparator threshold in a time \( t_1 = \frac{V_x}{C} (=10\mu\text{s}) \). Since \( t_1 \gg \tau_1 \) equation (A3.1) can be written as

\[
V_i(t) = Ct \left( \frac{t}{\tau} - 1 \right)
\]  

(A3.2)

The time \( t_2 \), for the true comparator input to fall by \( V_x \) volts is obtained from equation (A3.2):

\[
V_x = Ct_2 = Ct \left( \frac{t_2}{\tau} - 1 \right)
\]

i.e.

\[
t_{\text{dr}} = t_2 - t_1 = \tau
\]

Thus for a ramp input, the delay time between the true zero crossing point and the instant that the effective comparator input (Fig A3.2) is zero is \( = 7.7\text{ns} \).

A3.2 Rise time response for a ramp input

In Fig A3.1, it is observed that the rise time of the output is independent of the voltage overdrive value. We can thus represent the comparator as a high gain amplifier, (the output of which is limited to +5V) driving a resistance capacitance network (see Fig A3.4). From the time response curves of Fig A3.1, the output time constant \( \tau_0 \) (\( = \tau_{\text{eq}} \hat{e}_{\text{eq}} \)) is approximately 30ns. The gain, \( K \), of the LM206 comparator is typically 40,000, and the input threshold voltage, \( e \), is approximately 0.1mV.

For an input voltage ramp of \( C \) volts/sec, the output voltage, \( V_o \), in Fig A3.4 is given by:

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The output voltage, $v_0(t)$, of the equivalent generator rises at a rate of $KC$ volts/sec until it reaches a value of +5V and remains constant. Thus equation (A3.3) applies for a time $t = 5/KC$ secs. At the time $t$, we represent the constant value by saying that the generator output is still rising at $KC$ volts/sec, but is now in series with a secondary generator that is falling at a rate of $KC$ volts/sec (see Fig A3.5). By superposition the overall time response is obtained using equation A3.3.

Fig A3.6 shows the time response of the LM206 comparator for two values of input voltage rate of change $C$. The comparator output is initially adjusted to be at +5V, when the input is at zero volts. This introduces an input bias of approximately 0.1mV.

The switching threshold of the gate connected at the comparator output is indicated in Fig A3.6. When the $Y$ integrator output voltage magnitude is at its minimum value (40mV) the value of $C$ is $15 \times 10^2$ V/s. The difference between the true zero crossing point time $Q$, and the time the gate threshold is reached, $R$, is approximately 10ns. When $C = 15 \times 10^3$ V/s, the time difference be between $Q$ and $S$ is 35ns. As $C$ becomes larger, the input tends to a step function and the time difference remains approximately the same.
Fig A3.1  Time response of LM206 comparator for various input overdrives.

Fig A3.2  Representation of the LM206 comparator by an input network $R_{eq}, C_{eq}$ followed by a 'perfect' comparator.
Fig A3.3. Diagram depicting the voltages occurring in Fig A3.2.

Fig A3.4. Representation of the comparator output by a limiting amplifier followed by a RC network.

Fig A3.5. Representing the comparator generator limiting action by two superimposed voltages.
Fig A3.6 Time response of LM206 type comparator with different rates of change \((C)\) of applied input voltage.
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