Dopant activation and carrier transport in ion beam synthesised SiGe

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Abstract

Ion implantation has been investigated as an alternative technique to epitaxial deposition for the synthesis and doping of strained Si$_{1-x}$Ge$_x$ alloy layers. Use of an all-implanted process has the potential to overcome many issues and difficulties of doping, reproducibility and yield in the commercial production of SiGe heterostructure devices.

Samples with different germanium peak concentrations, $x$ (0 $\leq$ $x$ $\leq$ 15) were synthesised by implantation of Ge$^+$ into bulk Si, and were heavily doped with boron or with arsenic ($10^{20}$ cm$^{-3}$). Some layers were also post-amorphised by Si$^+$ implantation. Room temperature sheet resistance and Hall mobility were measured using the Van der Pauw method. Depth profiles were obtained using Secondary Ion Mass Spectroscopy (SIMS) and Spreading Resistance Profiling (SRP), to determine dopant distribution and sheet carrier concentration, respectively. The re-grown material quality of selected samples was investigated using cross-sectional Transmission Electron Microscopy (XTEM).

As a general trend, an increase in sheet resistance and a decrease in Hall mobility was observed with increasing germanium peak concentration in the ion beam synthesised layers. However, a speculative approach used to propose values and trends in drift mobility ($\mu_D$) suggested some improvements compared to bulk Si. Some confidence in the values of $\mu_D$ proposed is given by corresponding values of the Hall scattering factor, $r_H$, which are consistent with values reported in the literature for similar germanium content and layer thickness. Electrical junction depths were reduced in the synthesised layers compared to bulk Si.

Evidence from transmission electron microscopy (TEM) and electrical measurements shows that the highest germanium peak concentrations used exceed the critical threshold for production of strained SiGe layers after solid phase epitaxial growth (SPEG) in accordance with Paine's experimental model of strain relaxation in ion beam synthesised SiGe layers. It is proposed that estimated trends in $r_H$ may provide a useful source of evidence for strain relaxation.

Furthermore, use of ion beam synthesised SiGe leads to a reduction in diffusion of both boron and arsenic, compared to bulk-Si. This is attributed to the formation of BGe pairs and/or boron-interstitial (BI) clusters, and GeAs precipitates and/or As$_4$V clusters, which are also responsible for reduced carrier activation in the synthesised layers. In the As-doped samples, this trend differs from findings reported in the literature for deposited strained SiGe layers. Silicon post-amorphisation improves the carrier activation in As-doped samples; hence it is postulated that end-of-range (EOR) defects act as a barrier to arsenic enhanced diffusion.

It is concluded that an all-implanted route to the production of strained, doped SiGe layers is worth incorporating into commercial device manufacture.
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List of abbreviations and symbols

a/c - amorphous/crystalline
at % - atomic percentage
CVD - Chemical Vapour Deposition
EOR - End-Of-Range
HBT - Heterojunction Bipolar Transistor
IBS - Ion Beam Synthesis(ed)
LPCVD - Low Pressure Chemical Vapour Deposition
MBE - Molecular Beam Epitaxy
MOS - Metal Oxide Semiconductor
$\mu_D$ - drift mobility
$\mu_H$ - Hall mobility
$N_S$ - carrier concentration
$r_H$ - Hall scattering factor
$R_H$ - Hall coefficient
$R_p$ - projected range
$R_s$ - sheet resistance
RTA - Rapid Thermal Annealing
SIMS - Secondary Ion Mass Spectroscopy
SPEG - Solid Phase Epitaxial Growth
SRP - Spreading Resistance Profiling
TDD - Threshold Damage Density
TED - Transient Enhanced Diffusion
TEM - Transmission Electron Microscopy
UHV/CVD - Ultra High Vacuum/Chemical Vapour Depositions
$X_{el}$ - electrical junction depth
XTEM - Cross-Sectional Transmission Electron Microscopy
Chapter 1

1. Introduction

During the last thirty years, the microelectronic industry has used silicon as the principal semiconductor for the manufacturing of integrated circuit; both for its physical and chemical qualities, and for its adaptability to industrial processes and device manufacture. For several reasons, silicon is well suited to be used in this field. It is very abundant (~60% of the earth’s crust), and its oxide (SiO$_2$) is very stable and which provide both good quality Si/SiO$_2$ interfaces in Metal Oxide Semiconductor (MOS) devices and potentially provide protection to any underlying devices fabricated. Moreover it has a very convenient energy gap (1.12 eV) and devices fabricated in silicon are capable of operating at temperatures of up to almost 200°C [1].

Originally, germanium (Ge) was utilized as the dominant semiconductor electronic material for devices [1], but its relatively small band gap (0.67 eV) does not allow device operation at temperatures higher than about 90°C, because of the thermal generation of intrinsic carriers and associated high leakage currents [2]. Furthermore Ge does not have a stable oxide (GeO$_2$ is soluble in water, and it dissociates at about 800°C) and therefore is not convenient for MOS device fabrication.

Currently, silicon technology appears to have an even more promising future with the increasing adoption of SiGe [3]: Ge and Si are totally miscible in any proportion to form Si$_{1-x}$Ge$_x$ (0 ≤ x ≤ 1) alloys. The SiGe material system potentially has great technological importance for high performance electronic and optoelectronic devices [4]. Several silicon semiconductor companies are now developing SiGe technology to add to their standard metal-oxide-semiconductor (MOS) and heterostructure bipolar transistors (HBT) processes [5]. The advantage of using SiGe alloy for HBTs or field effect transistor silicon based devices, lies in the ability to engineer the band
structure, control dopant diffusion and in particular for MOS devices, enhance the free carrier transport properties in the active region of the devices as well as reduce the parasitic resistance of the various passive components of the circuits [6].

During recent years, device grade structures [3], with relatively low defect densities and abrupt Si/Si\textsubscript{1-x}Ge\textsubscript{x} interfaces, have been grown on silicon substrates using molecular beam epitaxy (MBE) and chemical vapor deposition (CVD) [4, 7]. Schüppen in 2001 [8] achieved in MOS devices, under research controlled conditions impressive high frequency performance of better than 150 GHz cut-off frequency (\(f_t\)) and 180 GHz maximum oscillation frequency (\(f_{\text{max}}\)). In 1999 John et al. [9] produced high performance (70 GHz \(f_t\)) low complexity non-selective Si/SiGe epitaxy devices with good low noise figures. However, control of these deposition techniques for high volume production of SiGe layers, although already in commercial production, is very expensive [3].

As an alternative technique to the epitaxy route for the synthesis of SiGe alloy and SiGe/Si heterostructures, several authors [10, 11, 12] have proposed ion implantation of high dose Ge\textsuperscript{+} (generally in the order of \(10^{16}\) ions/cm\textsuperscript{2}) into single crystal silicon in order to produce Si\textsubscript{1-x}Ge\textsubscript{x} graded interface alloy layers with germanium concentration up to 20% depending on the specific dose and implantation energy used. Under these conditions of high dose, an amorphous layer may be formed, whose thickness will depend upon the energy of the implant as well as the power loading during the implantation. Thus a thermal process step has to be introduced in order to obtain solid phase epitaxial growth (SPEG) and defect annihilation in the layer.

Ion implantation is a well-adapted standard technique and is fully compatible with existing planar processing technology. It also offers some unique advantages as compared with other techniques, such as good control of energy and dose which can be readily adjusted to achieve a specific concentration and depth profile. Since it is a non-equilibrium process, all elemental species can be implanted and buried layers achieved without recourse to thermodynamics (diffusion); since the slowing down of the ions is a random process, implant syntheses of Si/SiGe/Si heterostructures produce graded interfaces, which is potentially useful for application in bipolar transistors, as this introduces a built-in electric field which increases the velocity of the carriers in the base region of the devices; ion implantation is also a low contamination doping technique, and isotopically pure implanted atoms as well as
high alignment beams can be achieved. Moreover, the process is scalable, and concentration depth profiles can be modelled and reproducible [12, 3]. Application of ion implantation has led to the fabrication of both NMOSFETs [3] and PMOSFETs [11], using a strained Si$_{1-x}$Ge$_x$ channel, showing higher transconductance in the Si$_{1-x}$Ge$_x$ transistors as compared to Si control devices [9]. There remain, however, some fundamental issues to be addressed, related to the impact of high dose implant defects on the mobility and life-time in both p and n doped all-implanted heterojunction devices.

The research presented here is the first test of an all-implanted process for the synthesis and doping of strained Si$_{1-x}$Ge$_x$ alloy layers with various Ge contents (x) [13, 14]. In particular, the research was designed to find optimal processing conditions to (a) minimise the sheet resistance, (b) maximise the percentage activation of the B and As used as dopants, and (c) maximise the carrier mobility in SiGe test structures, with the aim of achieving lower parasitic resistance and higher operating frequency in SiGe heterostructure MOS devices.

These aims were addressed using ion implantation to synthesise and dope SiGe layers while systematically varying implantation parameters and annealing conditions. Materials were tested using the Van der Pauw (VdP) method and Hall effect measurement technique was used to perform electrical measurements of sheet resistance and Hall mobility. Spreading Resistance Profiling (SRP) was used to determine the percentage of free carrier activation. Secondary Ion Mass Spectroscopy (SIMS) was used to determine the atomic concentration depth profiles of B and As, in order to investigate dopant diffusion. Cross-sectional Transmission Electron Microscopy (XTEM) was used to assess the crystal quality of the synthesised alloy and to determine the number and the location of extended defects.

Chapter 2 presents a detailed discussion of crystal defects in Si and SiGe alloys, as well as properties of SiGe and SiGe/Si heterostructures, including a description of electron and hole mobilities. A discussion of relevant papers published in the literature is reported in Chapter 3. In Chapter 4, experimental details of ion beam synthesis and doping are described, as well as the techniques of analysis used to characterise the material. In Chapters 5 and 6 are reported the electrical results for B and As, respectively. Chapter 7 contains a general discussion of the findings.
presented in Chapters 5 and 6. Finally, the main conclusions and suggestions for future work are presented in Chapter 8.
Chapter 2

2. Background theory

2.1. Introduction

In this chapter, some key structural and electrical properties of SiGe alloys are introduced. In section 2.2 a description of the crystal defects, which can be formed in Si and in SiGe, alloys will be given. In section 2.3 the relevant properties of SiGe alloy will be examined and in section 2.4, structural properties of Si$_{1-x}$Ge$_x$/Si heterostructures will be discussed, with a particular focus on lattice mismatch and strain relaxation models for ion beam synthesised (IBS) SiGe alloys. In section 2.4.4, the electrical properties of strained SiGe layers will be reviewed, including band structure and transport properties.

2.2. Crystal Defects in Si and Si alloys

Silicon and germanium are thermally stable in air at room temperature and at atmospheric pressure and they can be mixed to form continuous solid solutions of composition Si$_{1-x}$Ge$_x$ with 0 $\leq$ x $\leq$ 1. Germanium and silicon have the same crystal structure and form alloys with a diamond crystal structure. The diamond structure consists of a face centred cubic (FCC) lattice with a two-atom base. The unit cell is shown in Figure 1 and contains four lattice sites and eight atoms [15].
The tetrahedral bonding between atoms in the diamond structure is a characteristic of the directional covalent bonding found in Group IV of the periodic table. An important difference between Si and Ge is the value of their covalent radii (half the distance between two consecutive atoms in the covalent crystal): 1.17 Å for Si and 1.22 Å for Ge. Silicon and germanium have lattice constants of $a_{Si}=5.431$ Å and $a_{Ge}=5.657$ Å, respectively.

Single crystal silicon, typically contains imperfections which may be point, planar, or volume defects, and which locally disturb the regular arrangement of the atoms which may significantly modify the properties of the material [16].

2.2.1 Point defects

All the atoms in a perfect lattice are, ignoring thermal vibrations, located on specific atomic sites. In a “pure” Si crystal there are only two possible types of point defects that can be formed: silicon vacancies and interstitials. The vacancy is formed by the removal of an atom from an atomic site and the interstitial by the introduction of an atom into a non-lattice site. Vacancies and interstitials can be produced by plastic deformation and by high-energy particle irradiation. In addition, “intrinsic” point defects may be introduced into the crystal by effect of temperature: for all temperatures above 0K there is a thermodynamically stable concentration of point defects [16]. The introduction of $n$ vacancies or interstitials in the Si lattice produces a change in the free energy ($\Delta F$) of the structure:
\[ \Delta F = nE_f - T \Delta S \]

Eq. 2.1

Where \( E_f \) is the formation energy of one defect and \( \Delta S \) is the change in entropy of the crystal, \( T \) is the temperature and \( n \) the number of defects. The equilibrium fraction of defects which correspond to a condition of minimum free energy, is given by [16]:

\[ n_{eq} = n_t \exp \left( -\frac{E_f}{kT} \right) \]

Eq. 2.2

where \( n_t \) is the total number of atomic sites and \( k \) is the Boltzmann's constant. Experimental values of the vacancy formation energy \( E_{f}^{v} \), which is required to remove one atom from the lattice structure and place it on the surface, are \( \sim 1 \) eV \( (1.6 \times 10^{-19} \text{ J}) \) for face cubic centred crystals such as Si and SiGe (see section 2.3).

The interstitial formation energy \( E_{f}^{i} \), which is required to remove one atom from the surface and place it into an interstitial site, is typically between 2 to 4 times \( E_{f}^{v} \), although ionic charges and valence effects may change this balance [16]. The rate at which a point defect moves from site to site in the lattice structure is proportional to \( \exp (-E_{m}/kT) \), where \( E_{m} \) is the defect migration energy.

Impurity atoms such as carbon, oxygen or hydrogen in a Si crystal are considered "extrinsic" point defects and they play an important role in the physical and mechanical properties of a semiconductor. Impurity atoms may be found in two different types of site: (a) substitutional, in which an atom in the lattice structure is replaced by the impurity atom and (b) interstitial, in which the impurity is sitting in a non-substitutional position [16].

Energy is required to form those defects which will cause local distortion in the lattice; the amount of distortion and therefore the amount of additional energy introduced in the lattice by the defects, depends on the distance between the atoms in the lattice and the effective radius of the atom introduced. When the local electric charge in the lattice is changed by the removal or the addition of atoms, to conserve an overall neutrality the vacancies must occur either (a) in pairs of opposite sign which form divacancies known as Schottky defects, or (b) in association with
interstitials of the same ion, known as Frenkel defects or (c) they combine to form simple complex or clusters [16].

2.2.2 Planar defects

A perfect lattice can be described as a stack of identical atomic layers arranged in a regular sequence. A stacking fault is a local region in the crystal where the regular sequence has been interrupted. The change in sequence can be the result of removing or introducing an extra layer which does not belong to the continuing patterns of either the lattice above or below the fault [16]. The presence of stacking faults can play an important role in the plasticity of the crystal and they can be also produced by sliding process (see paragraph 2.2.3). The associated energy per unit area of fault is called the stacking-fault energy which in Si and in Ge has a value of \( \equiv 50 \text{ mJ m}^2 \) [16]. Planar defects may also be associated with secondary defects or dislocations, which form during thermal processing of ion implanted material.

2.2.3 Volume defects

Volume defects can be precipitates, inclusions or dislocations which may also form during thermal processing of the material. In the absence of dislocations, the sliding of one plane past an adjacent plane is a rigid co-operative movement of all the atoms from a position of perfect registry to another. The shear stress required for this process to occur, is proportional to the shear module (\( \mu \)) and to the shear translation of the two rows away from the low-energy equilibrium position (equation given in ref. [16]). When dislocations are present, they can follow two types of movements: (a) glide motion in which the dislocation moves in the surface which contains both its line and the Burgers vector and (b) climb motion in which the dislocation moves out of the glide surface normal to the Burgers vector [16] (explained further). Glide of many dislocations result in slip, which is the most common manifestation of plastic deformation in crystals. Si and SiGe as well as all the face-centred cubic crystals have four \{111\} planes with three \{110\} directions in each and therefore they have twelve \{111\}\{110\} slip systems [16]. The geometry of a perfect or total dislocation is a line-defect bounding a slipped region of crystal. A circuit of 5 atoms square enclosing this line drawn around the atoms, (which would close in "perfect" material) have a closure failure as shown in Figure 2; this closure failure is called Burgers vector of the dislocation, when drawn around the dislocation core X [22].
For a total dislocation, the Burgers vector is a lattice translation vector and its value is constant even if the line direction of a given dislocation may vary arbitrarily (a convention for the determination of the sign of the Burgers vector is to draw the circuit of the dislocation from start S to finish F in the direction of a right-handed screw, RH-called FS/RH convention). A total dislocation cannot end within the bulk of the crystal, but must terminate at an interface with a non-crystal; this interface generally is a free surface, but may also be an interface with amorphous material or at a node with another defect, or upon itself to form a loop [22]. If the defect density is relatively low and interaction between dislocations is therefore unlikely, they will have to terminate at the nearest free surface; this requires the presence of threading dislocations which move across the layer from the interface to the surface. In general, each misfit dislocation is associated with a threading defect at each end, unless the misfit dislocation grows sufficiently to terminate at the wafer edge or for example at a mesa feature. The propagation of misfit dislocations occurs by lateral propagation of the threading arm [22]. The character of a misfit dislocation is defined by the relationship between its line direction $\mathbf{u}$ and its Burgers vector $\mathbf{b}$. When $\mathbf{b}$ is parallel or antiparallel to $\mathbf{u}$ the defect is known as screw dislocation; when $\mathbf{b}$ is perpendicular to $\mathbf{u}$, the defect is known as edge dislocation. In intermediate configurations, the dislocation is said to be mixed character. A dislocation has a self-energy associated with the distortion it produces in the surrounding substrate which
arises both inside and outside the dislocation core [22]. The dislocation core energy is not well known, but depends on both the type of material (nature of interatomic bonding) and the Burgers vector and character of the dislocation. The dimension of the core for elemental semiconductors has been estimated theoretically and experimentally by Hirth and Lothe in 1982 [23] to be its diameter (of the order of magnitude of the Burgers vector). The Burgers vector of a total dislocation is the minimum lattice translation vector in a given class of crystal structure and for the FCC structure of Si, SiGe and Ge, this minimum vector is \(\frac{a}{2} \langle 011\rangle\) [22].

Total dislocations can be dissociated into *partial dislocations*. A partial dislocation is a dislocation in which the Burgers vector is not a lattice vector. A common partial dislocation in FCC structures corresponds to a stacking fault along the \(\langle 111\rangle\) directions with a Burgers vector of \(\frac{a}{6} \langle 112\rangle\) or \(\frac{a}{3} \langle 111\rangle\) and they are called Shockley and Frank partials, respectively. Only the Shockley partial can glide within \(\langle 111\rangle\) planes [8]. Hull et al. [22] characterized the different partials according to the angle \(\theta\) between their line directions \(u\) and Burgers vectors \(b\). For dissociation from the \(\theta = 60^\circ\) \(\frac{a}{2} \langle 011\rangle\) total dislocation, the two \(\frac{a}{6} \langle 112\rangle\) partials have \(\theta = 30^\circ\) and \(\theta = 90^\circ\), respectively.

### 2.3. Properties of SiGe alloy.

The Si-Ge phase diagram was determined by Stöhr et al. [17] using thermal and X-ray analysis and is shown in Figure 3. The two lines represent the equilibrium phases between the solid phase delimited in the diagram by the upper line and the liquid phase (delimited by the lower) as a function of temperature and germanium concentration. The region between the lines represents a large range of solid-liquid coexistence phases, which make the SiGe alloy a system with strong segregation; Since Si has a much higher melting temperature (1412°C) compared with Ge (940°C), the preparation of a homogeneous solid solution from the molten phase is not easy, as the Si strongly segregates [18]. Ion beam synthesis, being a non-equilibrium technique, is therefore a very convenient method for the preparation of SiGe alloys, albeit only thin films layers; typically of thickness ranging between 10 to 400nm.
Although, Si and Ge have the same crystal structure and are completely miscible in any proportion [18], the difference between their lattice constants (see section 2.2), results in the larger lattice constant of the Si$_{1-x}$Ge$_x$ alloys (depending on germanium concentration) compared to bulk Si, causes a biaxial compressive strain between the silicon substrate and an epitaxially grown SiGe layer.

2.4. Properties of Si$_{1-x}$Ge$_x$/Si heterostructures.

M.J. Shaw et al [19] showed that the fundamental origins of strain in heteroepitaxy are from two sources: (a) the difference in lattice parameters, and (b) differential thermal expansion coefficients, between epitaxial deposited layer(s) and the substrate.

A precise and comprehensive determination of bulk lattice parameters and densities across the whole Si$_{1-x}$Ge$_x$ alloy system is the work presented by Dismukes et al. in 1964 [20]. Table 1 lists the lattice parameters of Si$_{1-x}$Ge$_x$ alloys at 25$^\circ$C for intervals of 5 at. % Ge [18]. These data reveal a small negative deviation from Vegard’s law [21], which estimates the alloy lattice parameter by linear interpolation between the values for pure Si and pure Ge, according to the relationship:

![Figure 3 Phase diagram of the SiGe alloy system between the melting point of elemental Si and Ge (from ref. [18]).]
where \( a(x) = 0.0069 \text{ nm} \), for \( x = 0.5 \) (see Table 1). This is a parabolic fitting of the data of Dismukes et al. for the \( \text{Si}_{1-x}\text{Ge}_x \) lattice parameter as a function of Ge content \( x \) as reported by H.-J. Herzog in 1993 [18].

<table>
<thead>
<tr>
<th>( x ) (at. % Ge)</th>
<th>( a(x) ) (nm)</th>
<th>( \Delta )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0.54310</td>
<td>.....</td>
</tr>
<tr>
<td>5</td>
<td>0.54410</td>
<td>-0.0004</td>
</tr>
<tr>
<td>10</td>
<td>0.54522</td>
<td>-0.0014</td>
</tr>
<tr>
<td>15</td>
<td>0.54624</td>
<td>-0.0026</td>
</tr>
<tr>
<td>20</td>
<td>0.54722</td>
<td>-0.0041</td>
</tr>
<tr>
<td>25</td>
<td>0.54825</td>
<td>-0.0051</td>
</tr>
<tr>
<td>30</td>
<td>0.54928</td>
<td>-0.0062</td>
</tr>
<tr>
<td>35</td>
<td>0.55038</td>
<td>-0.0065</td>
</tr>
<tr>
<td>40</td>
<td>0.55149</td>
<td>-0.0067</td>
</tr>
<tr>
<td>45</td>
<td>0.55261</td>
<td>-0.0068</td>
</tr>
<tr>
<td>50</td>
<td>0.55373</td>
<td>-0.0069</td>
</tr>
<tr>
<td>55</td>
<td>0.55492</td>
<td>-0.0063</td>
</tr>
<tr>
<td>60</td>
<td>0.55609</td>
<td>-0.0060</td>
</tr>
<tr>
<td>65</td>
<td>0.55727</td>
<td>-0.0055</td>
</tr>
<tr>
<td>70</td>
<td>0.55842</td>
<td>-0.0053</td>
</tr>
<tr>
<td>75</td>
<td>0.55960</td>
<td>-0.0048</td>
</tr>
<tr>
<td>80</td>
<td>0.56085</td>
<td>-0.0027</td>
</tr>
<tr>
<td>85</td>
<td>0.56206</td>
<td>-0.0023</td>
</tr>
<tr>
<td>90</td>
<td>0.56325</td>
<td>-0.0019</td>
</tr>
<tr>
<td>100</td>
<td>0.56575</td>
<td>.....</td>
</tr>
</tbody>
</table>

Table 1. Lattice parameter \( a(x) \) of \( \text{Si}_{1-x}\text{Ge}_x \) alloys for \( x \) from 0 to 100 at.% in 5% steps [18]

Because the discrepancy between the linear prediction and experimental data is of the order of 0.1%, it is reasonable to approximate \( a(x) \), at room temperature, using the linear form:

\[
a(x) = 0.5431 + 0.0227x \text{ nm} \quad \text{Eq. 2.4}
\]

In the context of this project, if we consider a thin epitaxial layer (= 1 \( \mu \text{m} \) alloy on silicon substrate), with lattice parameter \( a_l \) deposited on an infinite substrate with lattice parameter \( a_s \), which is elastically accommodated and with equal thermal expansion coefficients, then the elastic strain \( (\varepsilon_0) \) in the epitaxial layer is given by the expression:
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\[ \varepsilon_0 = \frac{2(a_l - a_s)}{(a_l + a_s)} - \frac{(a_l - a_s)}{a_s} \quad \text{Eq. 2.5} \]

When we consider the linear form instead of the parabolic fitting model the estimated elastic strain may differ by no more than (7%) [22]. Therefore, from the equation reported in [23], the elastic strain for a Si_{1-x}Ge_x epilayer on a Si substrate is given by:

\[ \varepsilon_0(x) = 0.0409x \quad \text{Eq. 2.6} \]

Elastic properties of SiGe alloy are generally described by two parameters: (i) the Poisson ratio (\(\nu\)) and (ii) the shear modulus (\(\mu\)). In the approximation of the ideal condition (elastic isotropy), \(\nu\) and \(\mu\) are proportional to the elastic constant of the alloy (\(C_{ij}\)), which defines the balance between the strains and the stresses in a distorted material [23].

2.4.1 Strain related phenomena (lattice mismatch)

The lattice mismatch strain is the driving force for several phenomena that control the equilibrium state of heterostructures and it can be accommodated by several mechanisms. The most important of these in the current context are (b) plastic relaxation via misfit dislocations and (c) elastic distortion of the thin film epitaxial layer, both of are shown in Figure 4. Additional mechanisms are interdiffusion across the epilayers/substrate interface and roughening of the surface especially in the case of a thin epilayer, typically less than 20 nm [22]. The latter will not be discussed here because they are not relevant to IBS SiGe, being typical phenomena during epitaxial deposition by CVD or MBE.
Figure 4 Schematic illustration of mechanisms for accommodation of lattice mismatch strain: (b) plastic relaxation via misfit dislocations and (c) elastic distortion of epitaxial layer (from ref. [25]).

Figure 4 shows (a), the difference in lattice constant between a silicon layer and the SiGe epitaxial layer, (b) the formation of a relaxed SiGe layer with formation of misfit dislocations; in this case, some bonds at the interface are missing or distorted, allowing the epilayer to relax towards its bulk lattice parameter. Finally Figure 4 (c) shows the case of coherent bonding across the interface which is achieved by elastic distortion of the epilayer (strained layer, also known as pseudomorphic or coherent). In this case, in the plane of the interface, the lattice parameter of the epitaxial layer is distorted so as to assume the lattice spacing of the substrate atoms. Perpendicular to the interface, the epilayer lattice parameter relaxes to form a tetragonal distortion of the unit cell [22]. The magnitude of the strain increases with the degree of mismatch between the lattice parameters of substrate and epilayer, as well as the thickness of the epilayer. Freund [30] found that for a given combination of substrate and epilayer, there will be a critical thickness ($h_c$) of the epilayer beyond which the level of strain is no longer balanced by the bonds at the interface. Beyond $h_c$, lattice mismatch strain is usually accommodated by the formation of misfit dislocations creating a relaxed layer (also known as unstrained or dislocated).
2.4.2  **Thermal mismatch**

SiGe alloys generally have temperature-dependent lattice parameters, from the thermal expansion coefficients which are temperature dependent [22]. The linear thermal expansion coefficients $\alpha(x, T)$ for Ge$_x$Si$_{1-x}$ alloys have been measured by Wang and Zheng [24]. The values of $\alpha(x, T)$ showed a non-linear relationship with Ge fraction and temperature, except in the range 0-800°C, where a linear interpolation between $\alpha_{Si}$ and $\alpha_{Ge}$ can be made with a confidence of 30% [22].

Although thermal mismatch strains are relatively small compared with the lattice mismatch strains, Cristiano et al [25], found that they can become relevant when a thick epitaxial layer is formed. In this case, lattice mismatch strains relax with the formation of misfit dislocations at the crystal growth temperature, but thermal stresses during the cooling down process can lead to the formation of further dislocations (partial/total) [22].

2.4.3  **Models of strain relaxation for SiGe/Si heterostructures.**

There are several models, involving the calculation of the critical thickness $h_c$, which describe whether strain in a lattice mismatched Si$_{1-x}$Ge$_x$ heterostructure results in misfit dislocations or is accommodated elastically. All of these models compare the energy of the strain which is relaxed by formation of misfit dislocations, with the energy associated with the dislocations. In particular, Hull [26] showed that when the relaxed strain energy is greater than the energy of the defect, formation of misfit dislocations are energetically favoured and the critical thickness correspond to the balance of those two terms.

*Matthews-Blakeslee* in 1974 [27] analysed the net force on a threading dislocation in relation to the primary stresses acting on the dislocation itself [22]. An illustration of these stresses is given in Figure 5. $\sigma_n$ is the lattice mismatch stress which induces the formation of misfit dislocations by lateral propagation of the threading arm (see Figure 6), thus relaxing the lattice strain along its free lattice parameter [22]. However, the threading dislocation has an internal energy which arises due to the strain induced by the surrounding SiGe crystal, and that produces a restoring stress $\sigma_T$ which inhibits the growth of the misfit dislocation. In addition, for partial misfit dislocations (which are mutually inhibited by the interaction of their crystal stress fields and which are driven apart on their common $\{100\}$ planes inducing a line of stacking fault between them on the same plain [26]), there is also a restoring force...
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due to the energy of the stacking fault, $\sigma_{sf}$. Therefore, the “excess stress”, $\sigma_{ex}$, is given by the following expression [22]:

$$\sigma_{ex} = \sigma_a - \sigma_T - \sigma_{sf} \quad \text{Eq. 2.7}$$

Figure 5 Schematic illustration of the Matthews-Blakeslee model of critical thickness (from ref. 22)

Matthews et al [27] determined the value $\sigma_{ex}$ as a function of epilayer thickness. Figure 7 shows an example of the variation of $\sigma_{ex}$ as a function of thickness of the Si$_{1-x}$Ge$_x$ epitaxial layer for an alloy composition with $x=0.25$. When $\sigma_{ex} < 0$, the introduction of misfit dislocations increases the energy of the system. When $\sigma_{ex} = 0$, the thickness of the layer, $h = h_c$ where $h_c$ is the critical thickness. When $\sigma_{ex} > 0$ the formation of misfit dislocation will be energetically favourite.
The Matthews-Blakeslee [27] also introduce a prediction for the critical thickness for the SiGe layer as a function of Ge content for different values of $\alpha$ (factor which describes the core energy of the dislocation), reported in Figure 8.

For lower growth temperatures the experimental values diverge from the theory, with larger critical values being recorded as the growth temperature decreased. Other parameters, like the kinetic of the misfit dislocation generation [22], have to be taken into account to predict the formation of misfit dislocations; those are not discussed here, as this project involved the synthesis of SiGe/Si heterostructures by ion
implantation and not by epitaxial growth and therefore they are not relevant in this content.

Paine et al. in 1991 investigated alloy layers formed by Ge\(^+\) implantation and presented a model [28] which enabled the author to predict the critical Ge\(^+\) dose above which strain relaxation will occur during solid phase epitaxy regrowth of ion beam synthesised Si\(_{1-x}\)Ge\(_x\)/Si and Si\(_y\)Ge\(_{1-y}\)/Ge\(_y\) alloy layers. The model was tested experimentally by implanting Ge\(^+\) into Si at 200keV and Si\(^+\) into Ge at 150keV. In this section, only Si\(_{1-x}\)Ge/Si heterostructures where Ge\(^+\) has been implanted into Si will be examined. Paine et al. [28] found that for low dose Ge implants, the lattice mismatch (which varies with depth) can be entirely elastically accommodated during solid phase epitaxial growth (SPEG) and the resulting epitaxial layer is free of defects. In the case of IBS SiGe the Matthews-Blakeslee model [27]. has to be modified due to (i) the absence of a well-defined compositional interface which make the calculation of the position of a defect in the strain layer more complex and (ii) the compositional profile has to be considered when calculating the amount of strain that can be accommodated elastically in the regrown material [28]. In previous experimental work Hirth et al. found [29] that relaxation of IBS Si\(_{1-x}\)Ge\(_x\) on Si during SPE involves 90° α/6(112) partial bounding stacking faults. Because the value of the critical thickness depends on the type of defects, the formation of stacking faults, together with the formation of misfit dislocations are considered in Paine's model. A stacking fault normally is bound at one end by the free surface of the material and at the other end by a partial dislocation with a Burgers vector of \(b = \alpha/6<112>\) which lies in the (001) plane. Considering stacking faults lying parallel to the \(\{111\}\) plane, the Burgers vectors of the possible bounding partials are: \([\bar{1}12]\), \([\bar{1}21]\) and \([\bar{2}11]\) ([28]). In addition, Paine found that the line direction of a partial dislocation lies in the <110> plane, the first mentioned partial dislocations will lie at an angle of 90° to the \([\bar{1}10]\) line direction (edge type dislocations), while the latter will make an angle of 30° [28].

In the analysis of the critical thickness associated with abrupt interfaces, the component of strain which generate misfit dislocations, lies at the interface between substrate and strain layer. In the case of Ge implanted into Si the stable position in the film at which the forces acting on the defect (which cause it to move along its glide plane), are balanced. The analysis only indicates the location of a defect in a graded layer without verifying whether the formation of the defect is energetically
favoured [28]. Moreover, the analysis assumes that the SiGe layer is fully regrown and therefore, the defect can be anywhere in the strain gradient moving along its glide plane (see Figure 9).

![Schematic view of the position of the force-balanced defect which lies on a \{111\} glide position](image)

Figure 9. Schematic view of the position of the force-balanced defect which lies on a \{111\} glide position (from ref. [28]).

The Paine theory involves the presence of three forces acting on the dislocation which force it to move along the glide plain:

1. An image force \( F_{im} \) (per unit length) due to the presence of the free surface which acts to pull the dislocation towards the surface and is inversely proportional to depth:

\[
F_{im} = \mu \cos(\alpha) \frac{b_e^2}{4\pi(1-\nu)} \left[ b_e^2 + (1-\nu) b_s^2 \right]
\]

Eq. 2.8

Where \( \mu \) is the shear modulus, \( b_e \) and \( b_s \) are the edge and screw components of the Burgers vector, \( \nu \) is the Poisson's ratio, and \( \alpha \) is the angle (54°) that the wafer plain makes normal to the surface and the \{111\} plane [28].

2. If the dislocation is a partial which bounds a stacking fault, there will be an additional force \( F_{sf} \) (per unit length), due to the surface energy of the stacking fault, \( \gamma \), acting to pull the partial dislocation along the glide plane towards the surface [28]:

\[
F_{sf} = \gamma
\]

Eq. 2.9
(3) A third force $F_{p k}$ (per unit length), due to the lattice mismatch, will act (against the balance of the previous two forces) to move the dislocation along the glide plain away from the surface:

$$F_{p k} = b_0 \sigma_0 (\gamma) \sin \alpha$$  \hspace{1cm} \text{Eq. 2.10}

Where:

$$\sigma_0 = \frac{2\mu(1+\nu)}{(1-\nu)} E_{\alpha}^{\text{proj}} \exp \left( - \frac{(y - R_p)^2}{2\Delta R_p^2} \right)$$

$\varepsilon_0$ is a constant of proportionality relating strain to composition, $R_p$ and $\Delta R_p$ are the mean projected range and the deviation from the projected range which describe the Gaussian implant distribution for a given implant energy, implanted specie and substrate. The position of the defect will be at the depth where the three forces are balanced: $F_{jm} + F_{sf} = F_{pk}$. In Figure 10 shows the depth distribution of the forces acting on the dislocation with two positions where the forces are balanced. One position is closer to the surface which represents a non-stable equilibrium of the defect and another one deeper into the substrate, which is to the depth at which the defect is stable. This latter is referred as $x_d$ and it is shown in Figure 11.
Figure 10. Schematic representation of the forces acting on the defect (from ref. [28]).

Figure 11. Defect position ($x_d$) for the three types of strain relieving defects as a function of the peak concentration of Ge implanted into $\langle 001 \rangle$ Si at 200keV (from ref. [28]).
Chapter 2

Background Theory

Paine’s model uses $x_d$ as a parameter to define the position of the amorphous/crystalline interface with respect to the surface before SPEG. The thickness of the regrown layer with non-abrupt interfaces is then $(x_d - y)$. According to Freund [30] the work done to create a unit length of dislocation is $W_{disl}$. When the partial dislocation is bound to a stacking fault lying on the $\{111\}$ plane, the work ($W_{fault}$) to produce a stacking fault across the SiGe layer also has to be considered [28]:

$$W_{fault} = \frac{2(x_d - y)}{\cos(\alpha)} \quad \text{Eq. 2.11}$$

Where $y$ is the stacking fault energy of 60mJ/m$^2$ for Si [28]. The work to introduce the defect has to be balanced by the work done by the layer stresses, which vary with position in the layer and therefore are a function of $y$:

$$W_{layer} = -b \sin(\alpha) \int_{y=x_d}^{y=x_f} \sigma(y) dy \quad \text{Eq. 2.12}$$

In order to calculate the position $y_c$, when the a/c-interface reaches the critical strain energy and a particular defect is energetically stable, the equation $W_{disl} + W_{fault} + W_{layer} = 0$ must be considered [28]. In calculating the critical dose, as a function of implant energy, Pain et al [28] used $\mu = 7.96 \times 10^6$ Pa, $\nu = 0.28$, $\gamma = 60$ mJ/m$^2$ (for the 30°, 90° and 60° dislocations) and tabulated implant profile data for $R_p$ and $\Delta R_p$ for implanted energies between 50 and 200keV Ge. The curve in Figure 12 shows the critical Ge peak concentration as a function of implant energy, for various defects.
Paine et al. [28] compared the data in Figure 12 with plan-view TEM data, and showed that the strain energy model can be used to predict the formation of strain relaxation defects, although they failed to predict the formation of misfit dislocations, in layers with greater than ~3 at% Ge peak concentration. According to Figure 12, 60° dislocations should be present in samples implanted with Ge at 200keV and with a peak concentration of about 3%, however they found no defects in the samples. The explanation they give is that the model was over simplified as they did not include the effect of dislocation interactions and the kinetic constraints of glide and climb. Furthermore, tabulated implant profiles rather than actual profiles contributed to the difference between the predicted defect position and the actual [28].

2.4.4 Electronic properties

The SiGe alloys form a continuously variable system of silicon and germanium (see section 2.3) with a wide range of energy gaps. For strained Si$_{1-x}$Ge$_x$ layers the band structure is altered compared to pure Si or pure Ge by the built-in strain which is determined by the lattice constant of the substrate and the alloy’s composition. The values at room temperature for the energies of indirect bandgap for Si and Ge are
respectively 1.12 and 0.66 eV. For strained SiGe on Si the tetragonal distortion, caused by biaxial strain, shifts and splits the valence and conduction band edges and thus alters the energy gap [31].

In particular, strain has two main effects on the bands structure of Si$_{1-x}$Ge$_x$: (a) the hydrostatic strain causes a shift in the absolute energy position of the band and (b) the biaxial strain causes a split in degenerate bands [32]. Figure 13 shows a schematic representation of those two effects.

![Figure 13 Schematic representation of the effect of hydrostatic and biaxial strains on a triply degenerate band (from ref. [32]).](image)

In unstrained Si$_{1-x}$Ge$_x$ layers, the presence of Ge reduces the minimum of the bandgap energy from the value of pure Si. However, the decrease of the energy bandgap is not linear with increasing Ge fraction (x), as shown in Figure 14. In the case of strained Si$_{1-x}$Ge$_x$ on Si, a further reduction of the bandgap is observed, due to the biaxial strain which splits the degenerate conduction and valence bands [32].
Chapter 2

Background Theory

2.4.4.1 Electron and hole mobilities in the SiGe system

The carrier mobility investigated in this project describes, in conditions of low electric field and in the absence of a magnetic field, the linear relationship between an electric field $E$ and the carrier drift velocity $\bar{v}_d$ as follows [35]:

![Image of indirect energy bandgap as a function of germanium content for unstrained (solid curve) and strained (dashed curves) Si$_{1-x}$Ge$_x$ (from ref. [33]).](image)

The strain-induced changes in the conduction and valence bands in strained SiGe will also affect values of electron and hole mobility due to intra- and inter-valley scattering [34].
\[ v_d = \mu E \]  

Eq. 2.13

The carrier mobility \( \mu \) can also be expressed as a function of the electron charge \( e \), the effective mass \( m^* \) and the scattering time \( \tau_i \):

\[ \mu = \frac{e}{m^*} \tau_i \]  

Eq. 2.14

\( \tau_i \) represents all scattering mechanisms that a carrier encounters when it moves through a semiconductor in the presence of an electric field and \( \tau_i \) is the sum (within the limits of the wave-vector-independent relaxation time approximation [35]) of all the reciprocal scattering times associated with the respective scattering mechanisms.

\[ \frac{1}{\tau_i} = \sum \frac{1}{\tau_i} \]  

Eq. 2.15

The drift mobility of strained SiGe has four predominant scattering mechanisms: (1) nonpolar optical, (2) acoustic phonon, and (3) alloy, which are associated with the lattice, and for doped SiGe an additional scattering due to (4) ionised impurities. In particular, the alloy scattering mechanism arises from local fluctuations in the Coulombic potential due to local variations of composition [149]. Because these fluctuations are independent of temperature, the scattering relaxation time, is also independent of temperature and can be define as follow [149]:

\[ \frac{1}{\tau_{\text{alloy}}} = \frac{\pi}{\hbar} U^2 x(1-x)N(E) \]  

Eq. 2.16

where \( \tau_{\text{alloy}} \) is the alloy relaxation time, \( U \) the interaction potential, \( N(E) \) the density of states and \( x \) the germanium fraction. It has been demonstrated by Stroud et al [36] that the alloying effect (although the actual alloy scattering mechanism in the conduction band is small) is significant. To summarise, the relaxation time can be calculated by combining all the scattering mechanisms (see Eq. 2.15), under the following assumptions [149]: (a) optical scattering occurs inelastically, (b) the
acoustic scattering is perfectly elastic, (c) holes/electron scattering is isotropic and, (d) hole/electron degeneracy effects are small and hence hole-hole scattering is negligible. Furthermore, in order to calculate the mobility, the alloy scattering is assumed to be independent of temperature and that the scattering mechanisms only change due to distortion of the band structure.

The development of a theoretical model to predict experimental values of mobility in SiGe and channel mobility ($\mu_{ch}$) for MOS devices, is still at a early stage [35]; partly because most simulations refer to values of drift mobility ($\mu_d$), whereas experimental data mainly concern the determination of Hall mobility ($\mu_H$) and sheet resistivity ($R_s$), where Hall measurements involve the presence of a magnetic field which will affect the scattering mechanisms. The values of drift and Hall mobility are not identical, where:

$$\mu_H = r_H \mu_d$$

Eq. 2.17

$r_H$ is the Hall scattering factor and it is usually of the order of 1, but can be close to 2 in particular situations (e.g. in the case of room temperature hole mobility of pure Ge [37]). The Hall factor is also a function of temperature and doping concentration and knowledge of the appendance upon these parameters is fundamental for the development of theoretical models [35]. Another obstacle to the development of accurate mobility models concerns the difficulty in fabricating Si$_{1-x}$Ge$_x$ bulk crystal with homogeneous Ge content ($x$) and a controlled doping concentration over the complete range of $x$ (0 $\leq$ $x$ $\leq$ 1) in order to obtain a significant range of experimental data [38]. Currently, new epitaxy techniques have overcome this constraint, but no systematic mobility investigation on relaxed bulk-like Si$_{1-x}$Ge$_x$ epilayers has been performed to date because of the dominant technological interest in pseudomorphic strained layers [39]. In 1997 Bufler et al. [40] reported values of minority and majority electron mobilities for unstrained and strained Si$_{1-x}$Ge$_x$ alloys up to 30 at % Ge. They found the mobility was reduced with increasing Ge content at low doping concentrations by alloy scattering, which dominates over impurity scattering in this conditions [41]. At higher doping levels ($\geq 10^{20}$ cm$^{-3}$), the relative fraction of alloy scattering in the total scattering rate is reduced and the value of the mobility increased in strained SiGe compared to bulk Si [41].
In the work reported in this thesis, both direct measurements of Hall mobility and calculated values of drift mobility are discussed in relation to values of the Hall scattering factor reported in the literature (section 7.3.4) for $N_s=10^{20}$ cm$^{-3}$ and $0<x<15$. 
Chapter 3

3. Literature Survey

3.1. Introduction

Many researchers using various deposition techniques such as molecular beam epitaxy (MBE), ultrahigh vacuum chemical vapour deposition (UVCVD) and ion beam sputtering have investigated the formation and material properties of SiGe/Si heterostructures [42]. In the early 1990s, Selvakumar et al. [43, 44] adopted ion implantation to synthesise thin layers of SiGe alloy as result of an interest in investigating technologies compatible with integrated circuit (IC) manufacture, as an alternative to epitaxial deposition, which is difficult and expensive to integrate into silicon fabrication device technology. However, high dose Ge$^+$ implantation (typically $\sim 10^{16}$ ions/cm$^2$) is necessary to form the SiGe phase, which introduces residual defects, which degrade the quality of the crystal [45]. In this survey, a particular focus will be given to those defects (especially End Of Range, EOR) which are known to affect dopant diffusivity, in particular, boron diffusion.

One of the most powerful techniques to observe crystal defects is Transmission Electron Microscopy (TEM) [66, 46, 47], which is extremely useful in detecting very small defects such as EOR, which are of the order of few nm.

3.2. Ion beam synthesis of SiGe alloy by Ge$^+$ implantation.

Germanium implantation into silicon has been used over many years, especially to preamorphise silicon prior to dopant implantation, thus avoiding profile broadening due to channelling [48, 49]. Typical doses required to achieve amorphisation are of the order of $\sim 10^{15}$ Ge$^+/cm^2$ at energies between 100 and 200 keV, and annealing temperatures above 500°C are required in order to remove the damage to the implanted layer [52] by SPEG. However, these conditions are not suitable for the
purposes of SiGe synthesis, since the germanium peak concentration is far below 1 at \%.

One of the first syntheses of SiGe alloys was attempted by Krautle in 1975 [50], where SiGe alloy with \(\sim 10\) at \% Ge peak concentration was obtained by implanting germanium at 35 keV with doses up to \(3 \times 10^{16}\) Ge\(^+\)/cm\(^2\). Subsequently, in 1981, Mazey and co-authors [51] showed that, for germanium peak concentration higher than 14 at \%, a highly disordered structure was formed after solid phase epitaxial growth (SPEG), suggesting that relaxation of the SiGe layer had occurred with possible formation of dislocations. With the growing interest in SiGe material from the microelectronics industry for its bandgap engineering properties, together with the production problems in scaling epitaxial deposition processes and their high costs, ion implantation was proposed as an alternative method to MBE, UHV or CVD to produce Si\(_{1-x}\)Ge\(_x\) crystalline layers for device purposes [45, 52, 53].

Regrowth behaviour of IBS SiGe as a function of germanium content with Ge\(^+\) implanted at 200 keV was extensively investigated by Paine and co-workers [54, 124], The authors found that, during the initial stage of regrowth at \(\sim 590^\circ\)C, and until the advancing a/c interface into the SiGe layer reached a position where the germanium peak concentration was \(\sim 10\) at \%, the a/c interface was planar with a morphology characteristic of bulk-Si \{011\}. However, when a critical value of the germanium peak concentration was exceeded, the morphology changed from a planar to a faceted interface \{111\}. This transition was observed by the authors to appear in the vicinity of the projected range of the implanted Ge\(^+\). In addition, extended defects (appearing as “V” shaped stacking faults from XTEM analyses) were found in fully relaxed SiGe layers in association with the faceting of the a/c interface during thermal annealing. Furthermore, the authors reported that the regrowth rates of the SiGe alloys was lower than that of pure silicon. Subsequently, Paine and co-authors [55] proposed a theoretical model (see section 3.4.3) which predicts the critical dose above which strain relaxation occurs during solid phase epitaxy in ion beam synthesised (IBS) Si\(_{1-x}\)Ge\(_x\)/Si and Si\(_y\)Ge\(_{1-y}\)/Si\(_y\) alloy layers, under the assumption that the defects formed during relaxation were stacking faults bounded by 90\(^\circ\) partial dislocations, although this was not actually the case for the relaxed layers fabricated in their experiment. Critical thickness calculations for Ge\(^+\) implanted into silicon made by Elliman et al [56] and others [57, 58, 59, 60], based on the Paine's model, reported good agreement with experimental data over a wide range of implantation energies. In 1999 Cristiano and co-authors [61] presented an empirical model.
identifying, for each Ge+ implantation energy, a critical value of the germanium peak concentration, above which extended defects nucleate in the vicinity of the germanium depth profile and extend up to the surface. They also determined a critical value of elastic energy stored in the structures of ~ 300 mJ/m², above which IBS SiGe alloys relax, irrespective of the implantation energy. This model was successfully tested on single crystal SiGe alloy layers obtained by implanting Ge+ between 70 and 400 keV, followed by Si+ post-amorphisation and SPEG at 700°C, including those samples containing relaxation-induced defects. Finally, the authors compared the model to Paine’s theoretical model and with experimental data available in the literature. Figure 15 shows a comparison of the data presented by Cristiano et al. [61] (circles) and data published from other studies (other symbols). The solid line shows the critical germanium peak concentration as a function of implantation energy, above which the structures are relaxed (filled symbols).

![Figure 15 Critical peak Ge concentration versus implantation energy, assuming a critical value of elastic energy of 300 mJ/m². The figure also shows the predictions versus the Paine model (dashed line: theoretical prediction; dotted line: experimental results) and experimental results from other published works. Empty symbols: strained structure. Full symbols: relaxed structures (from ref. [61]).](image)

The Cristiano et al. model was taken into account in planning the range of germanium peak concentrations for each energy used in the work reported in this thesis for the synthesis of strained SiGe layers.
Elliman et al [56, 60, 62] also studied the effect of strain on the regrowth velocity of SiGe alloys during SPEG, by time resolved reflectivity (TRR). They found that the regrowth rate in strained SiGe alloys is lower than in bulk-Si. They also reported that the regrowth rate is stress related, comparing the same sample implanted with a dose of germanium above and below the relaxation threshold. In particular, they found that the regrowth velocity of relaxed SiGe alloy is lower than bulk Si. Similar results were found by the same authors in thin deposited SiGe layers.

However, more recently, Corni et al [58] suggested that in order to explain the reduce velocity of the a/c interface through the alloy region during SPEG, the contribution of the interface roughness together with strain has to be taken into account. In particular Elliman et al. [63] suggested that the roughness of the a/c interface is proportional to the concentration of germanium in the alloy.

Finally, several researchers [45, 64, 65] reported that in order to improve the crystal quality of the SiGe alloy layers, low temperatures (down to the temperature of liquid nitrogen) implants need to be adopted. These authors reported that for low temperature implants, the main effect was a significant reduction in the number of EOR defects (see section 3.3.1), whereas no effect was observed on those defects which are associated to the strain relaxation of the alloy.

3.3. Primary and secondary defects caused by ion implantation

In 1970 and subsequently in 1997, Mayer and co-authors and Baba et al., respectively [66, 67], suggested that the main problems related to ion implantation are radiation damage and lattice disorder. During ion implantation the ions slow down, making a number of collisions with the lattice atoms. During these collisions momentum is transferred from the bombarding ion to the lattice atoms, which may carry sufficient energy to break the atom-atom bond and, therefore, may displace an atom from its lattice site (typical values of displacement energy for silicon range between $E_d \approx 10-20$ eV/atom [68]) to form Frenkel pairs (vacancy and interstitial). The recoiled atom may itself have enough energy to displace other atoms and eventually to create a cascade of atom collisions within the crystal, which will result in a highly disordered structure. For a sufficiently high number of displaced atoms, it is possible to create an amorphous phase. The amount of energy deposited during nuclear collisions which is required to form an amorphous layer is called the Threshold Damage Density (TDD) [72]. After implantation, high temperature
annealing (between 500°C and 1000°C) is required to re-crystallise the material, although this process usually lead to the formation of extended defects (secondary defects). Many researchers have investigated the formation of extended defects [69, 70, 71], and a systematic analysis of these defects has been presented by Jones et al. [72] in 1988. As a result of a detailed TEM investigation of defects, following a wide range of species implanted into Si, at various doses, energy, annealing time and temperatures, Jones [72] identified five categories of secondary defects (see Figure 16).

Category I secondary defects, also known as "sub-threshold damage", are formed when the dose of the ions is insufficient to produce an amorphous layer (see Figure 16 I). These defects are located at a depth in the vicinity of the peak of the ion distribution ($R_p$) and they are mainly perfect dislocation loops lying on {111} planes [73]. The point defects left over after recombination with vacancies and interstitials will be, according to Jones, mainly interstitial clusters, which have been estimated by Sadana et al. to be $\sim 20$ Å in size [74]. In addition to the dislocation loops, silicon implanted with light ions, such as B⁺ or Ne⁺, and annealed at temperatures below 700°C, also shows "rod-like" defects which have a {311} habit.
plane [75]. In 1996, Cacciato et al. [76] suggested that dislocations may occur during annealing due to the condensation of Si interstitials which are released during the annihilation of damage created by ion implantation (mainly small Si clusters of displaced atoms) [76]. These dislocations were observed when the number of Si atoms displaced by the implant, was higher than a critical number varying with the mass of the implanted species from \( 1.5 \times 10^{16} \text{cm}^{-2} \) for \( ^{11}\text{B} \) to \( 2 \times 10^{17} \text{cm}^{-2} \) for \( ^{121}\text{Sb} \) [77].

Category II defects, also named End-Of-Range (EOR) defects, are formed when the damage density is above the TDD (see Figure 16 II) and they are associated with Solid Phase Epitaxial Growth (SPEG) of the amorphous Si formed during ion implantation. They are formed in the vicinity of the original amorphous-Si/crystalline-Si (a-Si/c-Si) interface in the implanted material [78]. A more detailed explanation of these is given in section 3.3.1.

Category III defects are associated with imperfect regrowth of an amorphous layer produced during implantation. The major type of category III defects are: "hairpin" dislocations, microtwins [79] and segregation related defects [80] which may coexist [72]. Early observations of type III defects were made by Glowinski et al. in 1975 [81]. After implantation of 270keV Si in Si (001) and annealing at 600°C for 2h and 800°C for 1h, a band of perfect dislocation loops with a \( a/2 \langle 110 \rangle \) type Burgers vector was found lying on the plane intermediate between \{111\} and \{110\} between 500 and 600Å (in correspondence with the a/c interface) and half-loop dislocations were found (hairpin) starting from the a/c interface and extending up to the surface of the sample. The half-loop dislocations were also found to be interstitial type with a Burger vector of \( a/2 \langle 110 \rangle \). These loops are either pure edge with a loop plane lying on one of the \{110\} planes (perpendicular to the wafer’s surface) or they lie on one of the \{310\} planes forming an angle of 71.6° with the wafer’s surface with a Burgers vector that forms an angle of 45° with the surface [81]. The authors also observed that some of the hairpin dislocations were located above their nucleation point in proximity of the a/c interface, suggesting that they might have climbed towards the surface and therefore they could be removed by using a longer annealing time or a higher annealing temperature. Indeed, this hypothesis was confirmed later by several authors [80, 82]. After implantation of \( \text{B}^+ \) and \( \text{BF}_2^+ \) into pre-amorphised Si and subsequent annealing at 950°C for 10s or at 1050°C for 10s, Carter et al. [80] found the hairpin dislocations to be slightly above and considerably above the a/c interface, respectively. A possible explanation for the nucleation of those defects was
also given by the authors: after implantation the damage clusters may aggregate to form small dislocation loops at and below the a/c interface. It is possible that small loops are truncated at the a/c interface, and the two ends of the truncated loops act as nucleating sites for the hairpin dislocations [80]. Defect-free regrown layers were also found after annealing temperature of 1100°C for 10s [89].

Category IV defects form when the damage density slightly exceeds the value of TDD (see Figure 16 IV), and a buried amorphous layer can be formed [72]. For example, for heavy ions (such as As, P, Ge) implanted at room temperature at E ≥ 200keV and doses ~ 10^{14} ions/cm^2, the amorphous layer is buried and two c-Si/a-Si interfaces are present [83]. During SPEG, defects are created at the depth where these two advancing interfaces meet and they consist of faulted and perfect dislocation loops lying on planes parallel to the surface for both \{111\} and \{100\} silicon substrates [84]; in addition, two bands of EOR defects are formed behind the c-Si/a-Si interfaces. Formation of category IV defects can be avoided by decreasing the implant energy, increasing the dose or decreasing the implant temperature, in order to form a surface amorphous layer [72].

Category V defects occur when the solid solubility of the implanted species in silicon at the annealing temperature is exceeded. Under these conditions, an amorphous layer may form (see Figure 16 V). These defects are associated with the formation of precipitates of the implanted ions or with the formation of a new phase (e.g. SiC in C⁺ implanted Si or SiAs in As⁺ implanted Si) [72].

### 3.3.1 End Of Range Defects

The origin and the behaviour of end of range defects during annealing have been controversial and one reason for the limited knowledge of these defects lies in their small sizes (10-50nm), making their identification difficult [78]. These defects do not form when category I defects are present (the damage density is below the TDD) and a possible explanation given by Jones [72] is because category I defects act as sinks for the excess interstitials. EOR defects have been assumed by several authors [78, 85], to be types of dislocation loops. Their evolution from point defects to extrinsic dislocation loops upon annealing has been demonstrated by Mauduit et al. [86] to occur via intermediate defects configuration (as well as category I defects), such as interstitial clusters, and \{113\} stacking faults; EOR defects can only be removed during high temperature (900-1000°C) anneals and by 900°C most of the dislocation
loops are either faulted with Burgers vector \( \frac{a}{3} [111] \), while a few are perfect dislocations with Burgers vector \( \frac{a}{2} [110] \) lying on \{111\} planes [86, 87]. Several authors [91, 88] showed that, for a given annealing condition, the depth position and the density of the EOR defects depend upon the implant parameters of dose and energy. In 1991 Jones et al. [88] suggested that the density of the EOR defects decreases with the implantation energy, and therefore with the thickness of the amorphous layer. In 1984 Narayan et al. [89] suggested that, when the amorphous layer is less than 100nm, the dislocation loops glide towards the surface during annealing. This hypothesis has been proved wrong by Maudit et al. [86] who demonstrate that most of the dislocation loops are faulted loops which cannot glide (see section 3.2.3), but they can only grow through the emission and capture of point defects. Moreover, the EOR defects have never been detected in the regrown layer, between the c/a interface and the surface [91]. In 1991 Meekinson et al. [90] suggested that the decrease of the loops density as the amorphous layer is made thinner is attributed to the reduced distance over which interstitials have to diffuse towards the surface. This behaviour has been explained, in contrast, by Jones et al. [88] using the “recoil interstitials model” based on TRIM calculation. This model considers the EOR defects as the result of the agglomeration of interstitial atoms available beneath the c/a interface after the amorphous layer is formed. However, this model does not explain the density of the EOR defects upon all the implantation parameters and in particular the dose [91]. Later, in 1993 Laânab et al. [91] presented a model called the “excess interstitial model” that affirms that the EOR defects are created by the precipitation of Si interstitial atoms (self interstitials) that do not recombine with vacancies in the vicinity of crystalline/amorphous (c/a) interface during the ramping up of the temperature during the anneal. This model, which takes into account the thermal recombination of the interstitials with the vacancies before clustering, has been successful in explaining the variation of the EOR densities with ion mass, ion dose, beam energy and substrate temperature [91]. In 1996 Omri et al. [106] conducted an experiment to investigate the effect of the formation of EOR defects in proximity of a “free surface”. The effect was studied by keeping the initial amount of self-interstitials atoms, available to form a population of EOR defects, constant while they were etching away part of the amorphous layer, reducing the distance to the surface, before annealing. The authors found that the presence of a free surface has no detectable effect on the nucleation and growth of EOR defects.
and therefore the supersaturation of Si self-interstitials atoms involved in the process is unaffected by the presence of this surface. However, they also observed that, during nucleation, the c/a interface acts as a diffusion barrier for the Si self-interstitial atoms and the defect clusters are the only sinks for Si-interstitials. Only when the regrowth of the amorphous layer is completed up to the surface, (typically for temperature ~ 500°C, but in this case few milliseconds at 1000°C), the remaining supersaturation of Si-interstitials can interact with the surface. Yet, when this occurs, most of the defects are already involved in the Ostwald ripening process (see section 3.4) for which the Si-interstitials supersaturation in equilibrium with the loops is already small (but still from around 10 to 3 times the equilibrium value) [106]. Based on the excess interstitials model, in 1995 Laanab et al. [92] introduced the concept of “threshold” for the appearance of the loops. The authors found that if the number of excess interstitials is less than \( N_t = 2.2 \times 10^{14} \) atoms/cm\(^2\), no loops are formed for the annealing condition used (1000°C for 10 s). This phenomenon was also observed when implantations have been performed at low temperature [93]. When the sample is implanted at low temperature (i.e. 100K) no self-annealing occur during implantation and the c/a interface is located deeper than for the same implantation at room temperature. As a result, the number of interstitials beneath c/a interface is reduced by several orders of magnitude [92].

3.4. **EOR defects and dopant “anomalous” diffusion.**

During thermal annealing of boron implanted crystalline silicon, “anomalous” diffusion compared to the diffusivity of boron in the equilibrium condition (\( \text{DB}^* \)) (where \( \text{DB}^* = 5.1 \times 10^{14} \text{ cm}^2/\text{sec} \)) occurs during annealing, where the tail of the boron profile shows increased diffusion which can be several orders of magnitude higher than that which is predicted by equilibrium simulations [78, 95]. This behaviour has been shown by Claverie et al. [78] to be transient (diffusion decreases with annealing time) and depth dependent (related to the implant energy). The behaviour is referred to as “transient enhanced diffusion” (TED). Several authors [96, 97, 98, 99, 100] have shown that B diffusion is driven by the large supersaturation of Si self-interstitial atoms released during the formation and dissolution during annealing, of end of range defects. Transient enhanced diffusion is only detected comparing the depth boron profiles with boron profiles after long times annealings at low temperatures (< 1000°C), when the diffusion process reaches the
equilibrium and no further diffusion occurs. Simulations of TED would be possible if the concentration, the depth and the time dependencies of the Si interstitials saturation were known and incorporated in simulation softwares. Modeled parameters would also be applicable to describe the diffusion of other dopant species [101]

3.4.1 Boron implanted into silicon.

One of the first report of boron TED in implanted Si was given by Michel et al. in 1987 [102] where B diffusion was enhanced by several order of magnitude compared to the “normal” diffusion after annealing at 800°C for 35 minutes, while essentially no additional diffusion enhancement was observed for longer annealing times. When the temperature was raised up to 900°C, further profile broadening due to TED was reduced within seconds. This behaviour, of which lower annealing temperatures give rise to an enhancement of boron diffusion over a longer period of time, has been confirmed since then [101].

Because TEM analyses [73, 79, 80] have revealed that extended defects (Type I see section 3.3) were formed around the projected range of the B profile, the researchers proposed that the anomalous diffusion was associated with the presence of those defects. In 1994, supported by TEM investigations, Eaglesham et al. [96] identified these defects as {113} defects, also known as “rod-like” defects. Their structure was determined by Takeda et al. [103] to be extrinsic defects consisting of periodical array of Si-interstitials atoms along the (110) directions. The authors also suggested that they are created by precipitation of a supersaturation of Si self-interstitials; {113} defects are almost one dimensional precipitates in which the host and the matrix atoms are the same and the driving force for such a precipitation is the reduction of the chemical potential for an Si interstitial atom (Si(I)) to be incorporated into the defect. Claverie et al. [101] suggested the possibility of several metastable configurations of the Si(I) atoms within the {113} defects, involving the clustering of an increasing number of Si atoms. The authors pointed out that these defects can be considered as sinks or as sources of Si atoms depending upon whether they are growing or dissolving (depending on their size and on the silicon supersaturation).

Several authors [96, 97, 78] studied quantitatively the evolution of the {113} defects during thermal annealing. Experimental results show that they are reduced in
density, while their mean size increases. This behaviour is typical of the phenomenon known as "Ostwald ripening" or coarsening [104, 105]. This is a competitive process where bigger defects grow in size at the expenses of smaller ones and it occurs through the exchange of atoms between all precipitates, and hence maintains a supersaturation of Si atoms in the region. Therefore, the number of Si atoms involved in the process remains constant during annealing [106]. Within the supersaturated region, a small precipitate acts as a source of Si atoms, while a large one acts as a sink, which is why larger precipitates grow in size, while the overall density of the defects decreases [95, 106]. Assuming that all the defects have the same width, Eaglesham [96] and Stolk [97], calculated the number of Si(I) atoms contained in those defects and studied their variation as a function of annealing time at different temperatures. They showed that the total number of the Si atoms bounded to the defects decreases with increasing temperature. Claverie et al. [101] described the whole process as being a non-conservative Ostwald ripening process which allows the defects to retain their Si interstitial atoms for a much longer period of time [107]. Moreover, the authors found that the energy dissolution of the defect was \(-3.5\, \text{eV}\), a value which is close to the formation energy of a free Si(I).

In 1991 Giles [108] proposed a model, called the "+1 model". From TEM observations the total number of Si(I) atoms contained in the \{113\} defects was estimated to be the same as the B dose (formation of B-Si(I) complexes), implanted at energy between 10 and 50 keV. The author suggested that all the vacancies recombined with the Si-interstitial atoms, until the material was left with an excess of displaced Si atoms numerically equal to the dose. During annealing, B enhanced diffusion occurred through the formation of B and Si-interstitials (B-Si(I)) pairs. However, a very recent review article from Cristiano et al. [109] reports that the "+1" model is valid only for implantations of light ions (such as B) and at low implantation energies, when the spatial separation between the vacancies and the recoiled atoms generated by implantation is small. In addition, experiments made by Zhang et al. in 1995 [110] showed that the +1 model did not adequately account for the TED phenomenon. In their experiments, they found that when implanting boron, at low doses (~ \(10^{13} \, \text{ions/cm}^2\)), \{113\} defects did not form, although SIMS analyses showed indeed strong B TED. The authors concluded that another source of Si interstitial atoms may exist. In this case the activation energy for the TED was found be around 1 eV, close to the energy of dissolution of small clusters of interstitials or
to the migration of Si(I) atoms. In 1996 the experiment conducted by Huizing et al. [111] showed that the maximum enhancement of B diffusivity occurred before the \{113\} defects started to dissolve. Also in this case the activation energy for TED was smaller for short annealing times compared to longer anneals. The authors concluded that in order for the TED phenomenon to occur, a fast injection of Si(I) must happen before Si(I) are released by the \{113\} defects. Finally, in 1998 Caturla et al. [112] used a Monte Carlo simulation to investigate the behaviour of interstitials and vacancies, created by B implantation, during annealing. They found that while vacancies disappeared after a few seconds of annealing, Si interstitial atoms clustered together and after about $10^2$ s they started to dissolve. The authors, also extracted from the simulation that TED of B occurred mostly during the Si(I) clusters formation, rather than their dissolution. They therefore concluded that no correlation exists between dissolution of \{113\} defects and boron TED.

### 3.4.2 Boron implanted into pre-amorphised silicon.

Many of the published results about boron TED in Si relates to B$^+$ implantation into Ge$^+$ or Si$^+$ preamorphised samples with an amorphous layer thickness between 150-200nm and annealed with rapid thermal annealing (typically at 1000°C) to activate the dopants and to achieved SPEG [78, 95, 106, 113]. Under those conditions, TEM analyses have shown the formation of EOR defects around the former c/a interface (see section 3.3.1) and it was proposed that B TED was linked to those defects [101]. Claverie et al. [101] suggested that EOR defects result from the precipitation of excess Si interstitials atoms stored in an energetically stable configuration and they are, as well as the \{113\} defects, as reservoir of Si atoms; they can also be either a source or a sink for Si(I) atoms. During the ramping up of the anneal, vacancies and interstitials left behind the c/a interface recombine until only the excess Si-interstitials remain in the region and start nucleating clusters and extrinsic defects [101]. In 1997, Claverie et al [114], using Monte Carlo simulation, calculated that the number of atoms contained within the EOR defects was of the same order of magnitude of the excess silicon interstitial atoms, after recombination with the vacancies generated by implantation in order to amorphise the silicon substrate. The authors, also pointed out that the model proposed is formally similar to the +1 model, except that in case of amorphisation, the net difference between vacancies and interstitials is relevant only in the crystalline region of the sample, as the amorphisation process causes an initial increase (in the range of $10^{14}$ Si/cm$^2$)
supersaturation of Si-interstitials compared to the case of boron implanted into crystalline silicon. Several authors studied [78, 98] the evolution of the EOR defects-dislocation loops, upon annealing. Claverie et al [78] presented a detailed analysis of the loop evolution under different annealing conditions. The authors showed that, as well as the \{113\} defects, the loops grow in size and reduce their density during annealing, but the total number of Si atoms stored in the loops remain constant (see Figure 18). Calverie et al. [78] showed the effect of the annealing time on the size-distribution of EOR defects on Ge preamorphised samples, uniformly doped with B \((2 \times 10^{18} \text{ ions/cm}^2)\) and annealed at 1000°C. Figure 17 and Figure 18, summarise their results.

![Figure 17 Variation of the loops density (at/cm²) and of the loops radius (nm) as a function of annealing time for (150 keV Ge⁺ 2e15 ions/cm²) preamorphised samples, uniformly doped with B \((2 \times 10^{18} \text{ ions/cm}^2)\) and annealed at 1000°C (from ref. [78]).](image)

The authors suggested that the B TED is the result of two competing phenomena: dopant trapping on the defects and enhanced diffusivity at the edges of the defect-rich region. In their experiment the authors found that in the early phase of the anneal, the EOR defects formed by agglomeration of excess self-interstitials,
provided a large number of boron trapping sites, leading to the observed boron segregation.

\[
\begin{array}{cccc}
\text{annealing time (s)} & 0 & 200 & 400 & 600 & 800 & 1000 & 1200 \\
\text{number of atoms stored in the loops (1000\circ C)} & \text{1.0x10^{14}} & \text{1.5x10^{14}} & \text{2.0x10^{14}} & \text{2.5x10^{14}} & \text{3.0x10^{14}} & \text{3.5x10^{14}} & \text{4.0x10^{14}} & \text{4.5x10^{14}} & \text{5.0x10^{14}} \\
\end{array}
\]

Figure 18 Variation of the number of atoms stored in the loops as a function of the annealing time for (150 keV Ge^+ 2e15 ions/cm^2) preamorphised samples, uniformly doped with B (2x10^{18} ions/cm^2) and annealed at 1000\circ C (from ref. [78]).

For longer annealing times, the loop density decreases by releasing self-interstitials which diffuse into the substrate or to the surface where they are annihilated. Therefore, the number of B trapping sites decreases, and a fraction of the B atoms trapped in the EOR is released, leading to the decrease of the observed B segregation peak. At the same time the EOR defects (which also release interstitials), supersaturate the region around them. Therefore boron diffusivity is increased in the whole of the defected region but is measurable only on the edge of the band of the defects where the trapping is reduced [78]. In 1998 Bonafos et al. [98] investigated the growth behaviour of the loops for annealing temperatures ranging from 900\circ C to 1100\circ C and times from 1 to 400 s. They concluded that the loop density varies with time as a function of 1/t and the mean radius increases with t^{1/2} independent of other processes such as diffusion or loop interactions. In addition, the authors reported that the activation energy for loop growth for long annealing times (> 30 s), had been
determined to be ~ 4.5 eV an energy close to the value for self-diffusion in Si. For shorter annealing times, the activation energy was found to be between 1 and 2 eV.

On the bases of these experiment, Claverie et al. in 1999 [101], proposed that: (i) for long annealing times, the faulted loops are very stable and the equilibrium between loops and the supersaturation of Si(I) around them has been reached, from which they concluded that the loops are the only source and sink for Si interstitials; (ii) for short annealing time and therefore at the beginning of the anneal, point defects and loops have not reached a dynamic equilibrium and that Si atoms trapped or captured by the loops are mostly provided by either free Si(I) atoms remaining from the initial supersaturation or from other less stable defects or clusters with a binding energy that decreases with reduced defect size. In addition Alquier et al. [115] showed that TED in the regrown layer decreases steadily from a high value close to the EOR, to a low value at the surface, and it was suggested that this effect arises from a balance between generation of interstitials at the EOR and their recombination at the surface. In 1999 Cowern et al. [113] proposed a model of boron TED in preamorphised Si, which takes into account the role played by the surface. The model was confirmed and supported by the process simulation program TSUPREM4. The experiment was conducted by varying the thickness of the amorphous layer (generated by Ge implantation), by etching away different thicknesses of silicon varying from 80 to 175 nm, prior to further processing in order to maintain constant the structure of the EOR defects. Boron was then implanted into the remaining amorphous layers within the amorphised region and annealed at 900°C for 1s. The B depth profiles were finally measured by SIMS in order to observe the dependence of TED on the thickness of the regrown layer. The results of their experiment showed: (i) clear evidence of TED, (ii) that the profiles diffuse more in the tail than at the peak and (iii) that the amount of diffusion increases with increasing proximity of the EOR with the surface. The profiles are shown in Figure 19.
Figure 19 Depth profiles of boron and interstitials during annealing of shallow boron implants in Ge-preamorphised layers. Three different amorphous layer thickness are obtained by etching off part of the Ge preamorphised layer, prior to B implantation. Thin solid curve: 3 keV B implanted profile. Symbols: SIMS profile after 1 s at 900°C anneal. Thick solid curve: simulated B profile at 1 s 900°C. Vertical dashed lines: simulated edges of EOR defect band. Dashed curve: simulated interstitial profile at 1 s 900°C (arbitrary units) (from ref. [H3]).

The authors argued that the TED observed arises from an interaction between the EOR defects as the source of interstitials, and the surface as sink. Under these conditions, the measured TED should decrease with distance from the EOR band and the supersaturation should decrease more steeply towards the surface in samples where the amorphous layer is thinner [113]. In order to obtain agreement with the
experimental profiles, the author adjusted only two parameters in their simulations: the supersaturation in the band of EOR defects ($s_{\text{EOR}}$) and the supersaturation at the surface ($s_0$). To determine whether $s_{\text{EOR}}$ and $s_0$ are influenced by the position of the EOR defects, they fitted the boron profiles for each different EOR depth, separately and the quality of the fit they reported was satisfactory.

3.5. **Si post amorphisation and solid phase epitaxial growth (SPEG)**

The realisation of ultra-shallow and abrupt junctions is one of the requirements to reduce device dimensions and to achieve better integration in CMOS technology. The introduction of a pre-amorphisation stage helps to produce such junctions; in this way, channelling of low energy dopants can be eliminated while good activation can be achieved during solid phase epitaxial regrowth (SPEG) of the amorphous layer [78]. However, after SPEG, extended defects (EOR, loops) are formed beneath the former c/a interface which are responsible for the leakage current when they are placed in a space charge region of the device [116, 117] and they strongly affect impurity diffusion [118, 119]. To reduce the EOR damage and to improve the quality of implanted layers, a post-amorphisation regrowth process was developed by Zhang and co-workers [4], called EPIFAB (epitaxial re-growth across phase boundaries) which combines ion beam synthesis, post-amorphisation and solid phase epitaxial regrowth. The role of this process is to drive the EOR defects deeper into the substrate and away from the active area of the device. Several authors adopted the EPIFAB step for the fabrication of defect free SiGe/Si heterojunctions especially in CMOS processes [120].

3.6. **Application to SiGe HBT and HMOS devices**

Ultra Large Scale Integration (ULSI) circuits require both lateral and vertical scaling of device dimensions to increase the packing density and operational speed, as well as to reduce power consumption. As the device channel and gate dimensions are reduced, also the gate oxide thickness and the dopant diffusion in the source and drain regions need to scale to reduce the gate capacitance and the short channel effect, respectively [121]. Under these considerations, future devices (0.1μm technology) will require ultra-low energy (ULE) implants and well controlled anneals and etching processes [121].
Kawaura et al. [122, 123], researched into 0.1μm metal-oxide-semiconductor field-effect transistors (MOSFET's) to investigate transistor characteristics of ultra fine-gate MOSFET's. It is expected that small feature size devices will facilitate manufacture of very high-density integrated circuits and also high switching speed with low power consumption [123]. When the gate length is decrease to less than 30-40nm, several physical phenomena become detrimental to transistor operation. Short-channel effects are a problem in ultra fine gate length MOSFET's, because they degrade the cut-off characteristics of the devices [122]. To suppress them the reduction of the junction depth is needed in accordance with the miniaturisation of the lateral device size [122]. However, Ochiai demonstrated [123] that to accelerate the investigation of these devices, it is also necessary to develop sub100nm direct lithography processes with good control.

Silicon-based heterostructure technology appears to have a very promising future with the advent of SiGe [3]. The SiGe material system potentially has great technological importance for high performance electronic and optoelectronic devices [4]. During recent years device grade structures, with low defect densities and abrupt Si/Si$_{1-x}$Ge$_x$ interfaces, have been grown on silicon substrates using molecular beam epitaxy (MBE) and chemical vapour deposition (CVD) [3, 4, 7]. However, control of these deposition techniques to realise SiGe layer is very expensive and difficult to integrate with the existing fabrication device lines [3].

The first SiGe-channel MOSFET transistors realised using high-dose germanium implantation shows that SiGe MOSFET's have significantly higher transconductance than Si-channel MOSFET [3]. Selvakumar and co-workers [3] and others [9, 11, 124] have reported that it is possible to synthesise pseudomorphic Si$_{1-x}$Ge$_x$ through the use of implantation of $^{74}$Ge followed by SPEG. Application of this technique has led to the fabrication of both NMOSFETs [3] and PMOSFETs [11], using a strained Si$_{1-x}$Ge$_x$ channel, showing higher transconductance in the Si$_{1-x}$Ge$_x$ transistors as compared to Si control devices [9]. In particular Jiang [11] reported that compared with Si control devices on the same chips, SiGe transistors exhibited improved performance: the channel hole mobility and linear transconductance was up to 18% higher for surface-channel SiGe transistors, and up to 12% higher for buried-channel SiGe p-MOSFET's than for equivalent Si devices. Moreover it has been shown by Nayak [7] that SiGe p-channel MOSFETs have higher channel mobility than bulk-Si p-channel MOSFETs by confining the holes in a buried channel, and therefore
reducing carrier scattering at the SiO$_2$/Si interface. In addition the effective channel mobility of a strained Si$_{1-x}$Ge$_x$ layer is found to be 90% higher than of an identically processed conventional SIMOX device [7]. However Verdockt [6], reported that the transconductance of the p-MOSFET remains inferior to that of the n-MOSFET, primarily because the field-effect hole mobility is over a factor of 3 lower than the field-effect electron mobility. In MOS structures with undoped SiGe channels the holes travelling in the channel are expected to have enhanced mobilities due to the presence of Ge [35].
Chapter 4

4. Experimental details

4.1. Sample Description

In this project, two different groups of samples were used: group (a) contained implanted boron, and group (b) contained implanted arsenic, as dopants:

(a) The first group of samples was prepared from (100) n-type Si wafers, with resistivity 6-12 $\Omega$ cm and diameter 4”, together with p-type Wafer Bonded Silicon-On-Insulator (SOI) wafers, with resistivity 26-30 $\Omega$ cm and diameter 5”. The SOI wafers consisted of 1 $\mu$m of crystalline Si on 1 $\mu$m of buried silicon oxide (BOX) layer. The samples were implanted at the University of Surrey using two different accelerator systems. The 200 keV double magnet Danfysik accelerator (further details are included in section 4.2.1) was used to implant $^{74}$Ge$^+$ and $^{11}$B$^+$. Germanium was implanted at energies and doses (implantations details are reported in section 4.2.1) in order to synthesise $\text{Si}_1-x\text{Ge}_x$ alloy layers of different thicknesses (between ~50 and ~200 nm) and composition ($0 \leq x \leq 0.15$). Boron was then implanted at energies in order to overlay the depth profile of germanium (see Figure 20), with doses designed to achieve a constant peak concentration of $1x10^{20}$ B$^+$/cm$^3$. Additional silicon implants were carried out on selected samples using the 2 MeV Van der Graaff accelerator (see section 4.2.1) at energy of 250 keV and dose of $5x10^{15}$ Si$^+$/cm$^2$ in order to post-amorphise the material.

(b) The second group of samples was prepared from (100) p-type Si wafers, resistivity 6-12 $\Omega$ cm and diameter 4”. Using the 200 keV double magnet Danfysik accelerator, these samples were implanted with $^{74}$Ge$^+$ ions at different energies and doses (see section 4.2.1) in order to synthesise
Si$_{1-x}$Ge$_x$ alloy layers of different thickness (between -25 and -200 nm) and composition (0 ≤ x ≤ 0.15). Arsenic was then implanted at energies to overlay the germanium depth profile (see Figure 20), with doses varying with the implantation energy so as to obtain a peak concentration of $1 \times 10^{20}$ As$^+$/cm$^3$. As in the previous group, additional silicon implants were carried out on selected samples using the 2 MeV Van der Graaff accelerator at an energy of 250 keV and dose of $5 \times 10^{15}$ Si$^+$/cm$^2$ in order to post-amorphise the material.

Figure 20 SUSPRE simulation of 30 keV Arsenic, 7 keV B and 30 keV Ge.

The germanium doses and energies where chosen in order to form strained layers, according to the empirical model presented by Cristiano and co-authors [61] described in section 3.2.

After implantation, the wafers were cleaved into small pieces (typically 1x1 cm) and cleaned using, in sequence, trichloroethylene (60°C), acetone, isopropyl alcohol and deionised water (DI). The samples were dipped for about two minutes in each solution and quickly transferred from one to the next in order to avoid the solvents drying on the surface. After rinsing with DI water the samples were dried with a flux of nitrogen gas. Subsequently, the samples were treated with thermal annealing (for further details see section 4.2.4). Table 2 and Table 3 describes group (a) and group (b) of samples, respectively.
### Table 2 Description of group (a) samples

<table>
<thead>
<tr>
<th>Sample (Ge %)</th>
<th>Ge$^+$ Energy (keV)</th>
<th>B$^+$ Energy (keV)</th>
<th>Nominal Dose (Ge$^+$/cm$^2$)</th>
<th>Nominal Dose (B$^+$/cm$^2$)</th>
<th>Post-amorphisation</th>
<th>Annealing conditions (N$_2$ ambient)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0%</td>
<td>100</td>
<td>20</td>
<td>-</td>
<td>9e14</td>
<td></td>
<td>T$_1$ = 700°C 20 min</td>
</tr>
<tr>
<td>1%</td>
<td>100</td>
<td>20</td>
<td>3.13e15</td>
<td>9e14</td>
<td></td>
<td>T$_2$ = 700°C 20 min + 250 keV Si$^+$ φ = 5e15 cm$^2$ at -150°C</td>
</tr>
<tr>
<td>4%</td>
<td>100</td>
<td>20</td>
<td>1.18e16</td>
<td>9e14</td>
<td></td>
<td>T$_3$ = 1050°C 10 sec</td>
</tr>
<tr>
<td>6%</td>
<td>100</td>
<td>20</td>
<td>1.87e16</td>
<td>9e14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9%</td>
<td>100</td>
<td>20</td>
<td>2.18e16</td>
<td>9e14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10%</td>
<td>30</td>
<td>7</td>
<td>1.15e16</td>
<td>3.48e14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13%</td>
<td>30</td>
<td>7</td>
<td>1.49e16</td>
<td>3.48e14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15%</td>
<td>30</td>
<td>7</td>
<td>1.72e16</td>
<td>3.48e14</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Table 3 Description of group (b) samples.

<table>
<thead>
<tr>
<th>Sample (Ge %)</th>
<th>Ge$^+$ Energy (keV)</th>
<th>As$^+$ Energy (keV)</th>
<th>Nominal Dose (Ge$^+$/cm$^2$)</th>
<th>Nominal Dose (As$^+$/cm$^2$)</th>
<th>Post-amorphisation</th>
<th>Annealing conditions (N$_2$ ambient)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0%</td>
<td>100</td>
<td>100</td>
<td>-</td>
<td>6.25e14</td>
<td></td>
<td>T$_1$ = 700°C 20 min</td>
</tr>
<tr>
<td>1%</td>
<td>100</td>
<td>100</td>
<td>3.13e15</td>
<td>6.25e14</td>
<td></td>
<td>T$_2$ = 700°C 20 min + 250 keV Si$^+$ φ = 5e15 cm$^2$ at -150°C</td>
</tr>
<tr>
<td>4%</td>
<td>100</td>
<td>100</td>
<td>1.18e16</td>
<td>6.25e14</td>
<td></td>
<td>T$_3$ = 1050°C 10 sec</td>
</tr>
<tr>
<td>6%</td>
<td>100</td>
<td>100</td>
<td>1.87e16</td>
<td>6.25e14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9%</td>
<td>100</td>
<td>100</td>
<td>2.18e16</td>
<td>6.25e14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10%</td>
<td>30</td>
<td>30</td>
<td>1.15e16</td>
<td>2.5e14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>13%</td>
<td>30</td>
<td>30</td>
<td>1.49e16</td>
<td>2.5e14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15%</td>
<td>30</td>
<td>30</td>
<td>1.72e16</td>
<td>2.5e14</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Room temperature sheet resistance and Hall mobility were measured in a HL5900 Hall Profiler, using the Van der Pauw method (VdP); further details are given in section 4.3.1. The free carrier concentration was determined using spreading resistance profiling (SRP), as described in section 4.3.2. SIMS was used to acquire
chemical depth profiles for as-implanted and annealed samples sequentially, under identical conditions of analysis (see section 4.3.3). Finally, XTEM analysis were carried out on selected samples (see section 4.3.4) in order to examine the effects of post-amorphisation and Solid Phase Epitaxial Growth (SPEG) on the number and location of extended defects (End of Range).

4.2. Processing

4.2.1 Ion Beam Processing

The samples were implanted with $^{74}\text{Ge}^+$, $^{11}\text{B}^+$ and $^{75}\text{As}^+$ using the 200 keV Danfysik accelerator, whereas the $^{28}\text{Si}^+$ was implanted using the 2 MeV Van der Graaff accelerator. A schematic diagram of the 2 MeV accelerator is shown in Figure 21.

![Figure 21 Schematic diagram of the 2 MeV accelerator at University of Surrey (from ref. [25])](Image)

The Danfysik is a twin beam line system, with one electrostatically scanned beam line—Line 1—for implantation into a single wafer (up to 200 mm) provided with a LN$_2$ cooling system, and one high current magnetically scanned line—Line 2—for general purpose implantation (up to 400 mm). The ion source is a vacuum chamber, with pressure typically of 1.5x10$^{-5}$ mbar, in which an electric discharge can be fully or partially sustained by the gas or vapour of the material to be ionised. Such a discharge is generated between two electrodes, an anode and a cathode, by the
application across the electrodes of a D.C. voltage, the optimum value depends upon the ion species. The source is equipped with a 1800°C oven, and metal ion beams used to bombard the target can therefore be produced from the pure material, rather than from volatile compounds. In particular, a solid germanium sulphide source material was used for the germanium implants, arsenic metal was used as the source material for arsenic and gaseous boron trifluoride for boron. The ions were extracted by an electric field created by applying a voltage typically between 10 and 40 kV, then separated for the desired ion mass by an analysing magnet, and post-accelerated to the desired energy. In order to achieve energies lower than 10 keV, the mass analysed beam was decelerated from 10 keV down to 0.2 keV, using a three electrode deceleration lens.

A second magnet, the switching magnet, is placed just after the acceleration lens in order to deflect the beam into the two separate lines of the accelerator. In addition to splitting the beam, the switching magnet provides a further filtration of the beam, which improves its isotopic purity. The beam spot size and shape is then defined using water-cooled silicon apertures together with a combination of magnetic and electrostatic quadrupole lenses. The ion beam is electrostatically deflected by raster scanning deflection plates, scanning in both horizontal and vertical directions, so that the target area is homogeneously illuminated. The dose is measured by integrating the charges collected on each of four Faraday Cups (FC) positioned at the corners of the area scanned by the beam, defining the aperture in front of the implanted wafer. Each FC, connected to a separate integrator, had a suppression electrode biased to -200 V, to suppress secondary electrons. To limit cross contamination by forward sputtering, silicon was used for the beam defining apertures during both synthesis and doping implants. The size of the silicon aperture was adjusted to define the implanted area (typically 5 x 5 cm²).

Line 1 was used for Ge⁺ and As⁺ implantations. Samples were mounted on support wafers which were in turn placed on a conducting elastomer in contact with a SiN coated aluminium chuck (see Figure 22), which was cooled with liquid nitrogen in the case of Ge⁺ implants. The temperature was monitored by a thermocouple positioned on the support plate of the wafer outside the view of the beam. The dopant implants were performed at low target current density (between 0.64 and 2.8 µA/cm²), to minimise beam-heating. Boron implantation was performed in Line 2, on the 8-wafer wheel, in a vacuum better than 10⁻⁶ mbar. The wafers were tilted by
7° and rotated by 22 degrees with respect to the incident ion beam, to reduce ion channelling.

The $^{28}\text{Si}^+$ implants were performed in the 2 MeV accelerator, using a Hot Penning source with either Si sputtered or gaseous SiH$_4$ as the charge material. The wafers were cooled by mounting on a nickel-plated copper block, which was in thermal contact with a LN$_2$ bath, and were tilted 7° off the incident beam direction. The temperature of the sample was monitored by a thermocouple, positioned on the wafer but not in sight of the beam. A thin film of vacuum grease was used to ensure good thermal contact between the wafer and the copper plate (see Figure 22).

Figure 22 Schematic of the sample holder in the 2 MeV accelerator at University of Surrey (from ref. [25])

4.2.2 Synthesis of SiGe alloy.

Germanium ions were implanted at three different energies, 10, 30 and 100 keV, with the wafers cooled to a temperature of less than −90°C. The average ion beam current density was of 2 µA/cm$^2$, which corresponds to a power loading of 0.8, 2.4 and 3.8 mW/cm$^2$ for 10, 30 and 100 keV, respectively.

In order to produce strained, defect-free SiGe layers, the Ge content in the alloy was restricted to peak values of 0 at % to 9 at % for $^{74}\text{Ge}^+$ implanted at 100 keV ($R_p = 71$ nm), and of 0 at % to 15 at % for $^{74}\text{Ge}^+$ implanted at 30 and 10 keV ($R_p = 25$ and 12.5 nm, respectively). The germanium doses used are listed in Table 2 and Table 3.
Selected samples were then post-amorphised with $5 \times 10^{16} \text{Si}^+/\text{cm}^2$ at 250 keV, in order to position the formation of the EOR defects far below the implanted SiGe layer at around 0.5 \( \mu \text{m} \) depth (see Figure 23).

### 4.2.3 Doping

Boron was implanted at room temperature at 20 keV (\( R_p = 69 \text{ nm} \)) and 7 keV (\( R_p = 27 \text{ nm} \)) with a peak concentration of $1 \times 10^{20} \text{ions/cm}^3$, corresponding to doses of $9 \times 10^{14} \text{B}^+/\text{cm}^2$ and $3.48 \times 10^{14} \text{B}^+/\text{cm}^2$, for 20 and 7 keV, respectively.

Arsenic was implanted at room temperature at 100 keV (\( R_p = 68 \text{ nm} \)), 30 keV (\( R_p = 26 \text{ nm} \)) and 10 keV (\( R_p = 13 \text{ nm} \)) with doses $\phi = 6.25 \times 10^{14} \text{As}^+/\text{cm}^2$, $\phi = 2.5 \times 10^{14} \text{As}^+/\text{cm}^2$ and $9.25 \times 10^{13} \text{As}^+/\text{cm}^2$, respectively, corresponding to a peak concentration of $1 \times 10^{20} \text{ions/cm}^3$.

### 4.2.4 Thermal anneals

All samples were annealed in a nitrogen gas ambient (\( \text{N}_2 : \text{H}_2 = 90 : 10 \)) at 1.5 l/min using a Process Products Corporation RTP halogen lamp system at the University of Surrey. The nitrogen process gas was purged for 3 minutes before each anneal, to
flush out water vapour and oxygen atmosphere. The samples were loaded horizontally, on a support silicon wafer supported by a 600 mm quartz rod, into a quartz sleeve furnace chamber. The annealing temperatures were monitored by a thermocouple cemented in the centre of the support wafer. The annealing conditions chosen in this work were: $T_1 = 700^\circ\text{C}$ for 20 minutes, $T_2 = 700^\circ\text{C}$ for 20 minutes plus RTA at 1050°C for 10 seconds and $T_3 = \text{RTA only}$. Furnace annealing conditions in $T_1$ and $T_2$ were selected on the basis of pilot work; elsewhere [25] this temperature has been shown to achieved good quality SPEG of IBS SiGe alloy layers. RTA conditions in $T_2$ and $T_3$ were selected to ensure comparability with research conducted elsewhere [120]. The ramp up temperature was of $\sim 5.8 \ ^\circ\text{C/s}$, whereas the ramp down was of $\sim 1 \ ^\circ\text{C/s}$.

4.2.5 Photolithography

Optical lithography was used to define the Van der Pauw (VdP) pattern on the samples prior to metallisation, using a chromium on quartz mask. The photoresist AZ4330a was used to cover the samples by spinning them at 40 RPM for 50 seconds to create a uniform film $\sim 3 \ \mu\text{m}$ thick. After a “soft” baking at $100^\circ\text{C}$ for 30 seconds on hot plate, each sample was exposed separately in a Karls Suss MJ 133 UV 300 Mask Aligner for 3.6 seconds under UV light generated by a mercury vapour arc lamp. The voltage applied to the electrodes in order to generate the arc ranged from 16 V to 70 V, when stabilised. A nitrogen flux was used to cool the lamp and to stop the contacts oxidising. After exposure, the photoresist was developed in AZ400K developer diluted with DI water in proportion 1 : 3. The defined VdP samples were 5 mm x 5 mm in size, as shown in Figure 24.

Figure 24 Van der Pauw pattern.
Chapter 4

4.2.6 Sample Etching

The samples were dipped for two minutes in an etchant solution composed of:
125 ml of nitric acid (HNO$_3$) 68%, 5 ml of hydro fluoride acid (HF) 48% and 25 ml of de-ionised water (DI), to etch ~ 1 μm of silicon.

The reactions oxidising the Si (HNO$_3$) and then removing the SiO$_2$ with HF followed the chemical equations:

\[ 4H^+ + Si + 4NO_3^- \Leftrightarrow SiO_2 + 4NO_2 + H_2O \]  
Eq. 4.1

\[ SiO_2 + 4HF \Leftrightarrow SiF_4（volatile）+ 2H_2O \]  
Eq. 4.2

4.2.7 Metallisation

Aluminium was evaporated on the patterned samples in a General Evaporator. The contact area was defined by painting the photoresist on the surface of the samples, taking care to cover all areas except those marked as “Al contact” in Figure 24. Before they were positioned in the evaporator, the samples were dipped in buffered HF to remove the native silicon dioxide. The base pressure inside the chamber prior to evaporation was between 1 and 2x10$^{-7}$ mbar, while the pressure during Al evaporation was between 2 and 4x10$^{-6}$ mbar. The Al metal was placed in a tungsten boat connected at both ends to resistors to which a potential of 23 Volts was applied, in order to evaporate the metal. The chamber was provided with a LN$_2$ trap to limit gas contamination. Once evaporated, the metal was sintered at 400°C for 2 minutes by furnace annealing in N$_2$ flow to ensure a good adhesion to the sample.

4.3. Analysis techniques

4.3.1 Hall Effect

Sheet resistance and in plane Hall mobility were measured at the University of Surrey, using an HL5900 Hall Profiler. The measurements were performed at room temperature using the Van der Pauw method (VdP) [125], applying a magnetic field of 0.328T for the Hall mobility measurements.
Figure 25 shows an example of cross section of a Van der Pauw clover leaf, when a current is injected through two of the Al contacts. The current will flow mainly through the implanted layer parallel to the surface of the sample, when a good p-n-p junction isolation and a "defect free" crystalline material are provided.

![Cross section of a Van der Pauw clover leaf when the current is injected through the Al contact.](image)

The case presented in Figure 25 represents an example of a SiGe implanted sample that, after SPEG, would show the presence of EOR defects (see Chapter 3). These defects, together with secondary defects which may form during annealing, can be one of the causes for leakage current flowing through the substrate. The quality of the active layer is therefore directly reflected in the electrical measurements.

Sheet resistance measurements were made by injecting a constant current of 4 µA (I) across two of the four aluminium contacts on the VdP patterned sample (see Figure 24), and measuring the potential difference (V) across the other two contacts. These measurements were repeated four times, so that all possible combinations were satisfied. Two values of resistance $R_1$ and $R_2$ were considered in order to estimate the value of sheet resistivity, according to the following equations:

$$R_1 = \frac{V_{3,4}}{I_{1,2}} \quad \text{Eq. 4.3}$$
$$R_2 = \frac{V_{4,1}}{I_{2,3}} \quad \text{Eq. 4.4}$$

where $I_{1,2}$ represents the current injected across contacts 1 and 2, and $V_{3,4}$ represents the potential difference between contacts 3 and 4, and likewise for $I_{2,3}$ and $V_{4,1}$. 57
These measurements were repeated by injecting a reverse current, in order to eliminate the effect of contact resistance. The sheet resistance was then extracted from the following relation:

\[ \rho_s = \frac{\pi}{\ln 2} \frac{(R_1 + R_2)}{2} \cdot F \]  
\[ \text{Eq. 4.5} \]

where \( F \) is a correction factor, which is a function of \( R_1 \) and \( R_2 \) and of the geometry of the sample; for a perfectly symmetrical sample \( F = 1 \).

When a magnetic field \( B \) is applied to the sample, together with the injected current \( I \), this induces an electric field perpendicular to both \( I \) and \( B \). This phenomenon is called the Hall Effect. The Hall effect was used to determine the type of majority free carriers (electrons or holes), their concentration, and the Hall mobility. The Hall mobility was extracted from values of the Hall coefficient, \( R_{Hs} \), estimated from measuring the Hall voltage \( V_H \) (when the magnetic field \( B \) was applied).

The Hall coefficient \( R_{Hs} \) is given by the following equation:

\[ R_{Hs} = \frac{(V_{HB} - V_{HO})}{B \cdot I} \]  
\[ \text{Eq. 4.6} \]

where \( V_{HB} \) is the Hall voltage, measured when the magnetic field is applied, and \( V_{HO} \) is the voltage with no magnetic field applied.

The Hall coefficient was then used to calculate the sheet carrier concentration \( N_s \) and the Hall mobility \( \mu_H \), as follows:

\[ N_s = \frac{r_H}{e \cdot R_{Hs}} \]  
\[ \text{Eq. 4.7} \]

\[ \mu_n = \frac{R_{Hs}}{\rho_s} \]  
\[ \text{Eq. 4.8} \]
where $e$ is the electronic charge, and $\tau_H$ is the ratio between the Hall mobility $\mu_H$ and the drift mobility $\mu_d$, also known as Hall scattering factor, which is assumed to be unity (but see section 7.3.4).

### 4.3.2 Spreading Resistance Profiling

Spreading resistance profiling (SRP) was conducted by Semiconductor Assessment Services Ltd., following the method outlined by Pawlik [126]. Samples were ground to a bevel of approximately 8', using high quality 0.1 µm polycrystalline diamond paste. Closely spaced (~ 20 µm) pre-conditioned tungsten-osmium alloy probes with contact radii ~ 1.8 µm and probe loading ~ 5 g were used to take repeated measures of spreading resistance with a step length of 1.0 µm, for a vertical resolution of ~ 2.5 nm. Probes had previously been calibrated using bulk calibration samples. A high quality optical microscope with dark field illumination and photographic camera was used to establish the starting point of profiles. Bevel angles were checked using a calibrated surface profilometer with accuracy of ± 1 %; hence, it is estimated that depths in the resulting profiles were accurate to the same percentage.

Smoothed spreading resistance profiles were estimated from the raw data by Semiconductor Assessment Services Ltd., using constrained cubic splines smoothing [127]. This uses conventional cubic splines to fit the data, but the algorithm is constrained on the basis of an initial visual examination to identify trends and concave or convex regions in the raw data, thus ensuring that the smoothing corrects for random noise, rather than amplifying it.

Resistivity profiles were derived from the smoothed profiles using the Berkowitz-Lux algorithm to calculate the sampling volume correction factor for non-bulk samples [128]. For input into this algorithm, the calibration curve was estimated using simple linear interpolation between data points [126]. Resistivity profiles were converted to carrier concentration profiles by Semiconductor Assessment Services Ltd., using ASTM Standard F723. In the course of extensive validation research comparing results from SRP with results from other electrical and non-electrical methods, such as secondary ion mass spectrometry (SIMS), Rutherford back scattering (RBS), neutron activation analysis (NAA), CV profiling, and electrochemical CV profiling (ECV) [129, 130], an accuracy value of ±2.5% in carrier concentration has been established in silicon [131].
Strictly, the extraction of carrier concentration from spreading resistance profiles assumes (i) that the material being profiled is uniformly doped bulk silicon, and (ii) that no changes are made in the carrier mobility during the layer creation process. Nevertheless extensive testing of samples in Si and Si_{1-x}Ge_{x} grown by MBE has shown no deviation from known concentration depth profiles in Si_{1-x}Ge_{x} samples with up to 20 at \% Ge. In samples with 20 to 50 at \% Ge, an increasing systematic deviation of up to 5\% from the known profile was observed. Above 50 at \% Ge, measurements were no longer possible as the softness of the material changed the nature of the point contacts [130, 131]. Since no mobility curves are available to date for bulk SiGe [131, 132, 133], the SRP measurement and the computations described above, which have been used elsewhere in SiGe research [134, 135, 136], were considered appropriate for the derivation of speculative values of carrier activation in Si_{1-x}Ge_{x} over the range of germanium peak concentrations used in this work (but see section 7.3.1).

4.3.3 Secondary Ion Mass Spectroscopy

The SIMS analyses were carried out by Dr. Claude Armand in the National Institute of Applied Science (INSA) in Toulouse, and by Dr. Hamid Kheyrandish in MATS, UK, using an Atomika quad 4500 instrument. For both analyses, the primary beam was 500 eV O^{2+} at near normal incidence conditions. The depths of the resulting SIMS craters were measured in two perpendicular directions using a Dektak surface profilometer. The boron and the arsenic concentrations were calibrated using SIMS reference materials which are traceable to NIST.

The uncertainty of the measurement depends on the background noise of the instrument. For example if boron is considered, the minimum measurable concentration was about 10^{15} at/cm^{2}. Depth resolution carried an uncertainty of ± 1 nm.

4.3.4 Transmission Electron Microscopy

The electron microscopy was carried out by Dr. Yun Wang using a JEOL 2000-FX TEM at the University of Surrey and by Dr. Fuccio Cristiano using a JEOL 2010-HC microscope at CEMES/CMRS in Toulouse.

Both microscopes operate at a voltage of 200 keV, with a nominal point-to-point resolution of ± 0.3 nm. The samples for cross sectional observations were cleaved into small pieces (typically 3 x 10 mm^{2}), cleaned in sequence with trichloroethylene,
acetone and isopropyl alcohol and glued together (top surfaces in contact), with an epoxy resin. The glued samples were then cut into 500 µm thin sections using a diamond saw. These sections were ground and polished down to a thickness of 30 µm, using silicon carbide and aluminium oxide grinding papers with grain sizes of 15 µm and 3 µm, respectively. The thin sections of the samples were then mounted into a 3 mm copper grid using silver dag, loaded into the beam miller (Model: Gatan 600) and bombarded using a dual Ar+ beam—accelerated to 5 keV with an incident angle of 15°—until electron transparency of the samples was obtained.

The areas analysed by cross section TEM were of the order of 10 µm² (typically 0.5 µm x 20 µm), so that the lower detection limit of the resolved defects was ~ 10⁷ cm⁻².
Chapter 5

5. Results from boron implanted samples

5.1. Introduction

This chapter reports sheet resistance ($R_s$) and Hall mobility ($\mu_H$) measured on Group (a) of samples, described in section 4.1. Atomic and electrical profiles are presented from which the activation of boron has been determined. Finally, selected samples were observed by transmission electron microscopy to investigate the formation and location of extended defects.

5.2. Activation and carrier transport of $Si_{1-x}Ge_x$ doped with boron at 20 keV and 7 keV.

This section is composed of two parts: section 5.2.1 presents the results for boron implanted at 20 keV into $Si_{1-x}Ge_x$ and section 5.2.2 presents the results for boron implanted at 7 keV. The data presented are from samples treated with three different annealing conditions: $T_1$ (furnace annealing at 700°C for 20 minutes), $T_2$ (furnace annealing plus RTA at 1050°C for 10 seconds) and $T_3$ (RTA only).

5.2.1 20 keV boron

5.2.1.1 $R_s$ and $\mu_H$ as a function of Ge content in bulk-Si and in SOI substrates

In all graphs in this chapter, lines joining data points are included only as a guide for the eye.

Figure 26 shows the variation of sheet resistance for samples prepared in bulk-Si substrates. For scaling purposes, the value of the sheet resistance for the sample annealed using schedule $T_1$ in bulk-Si substrate ($1700 \pm 17 \, \Omega/sq$) is omitted. In all $Si_{1-x}Ge_x$ samples, sheet resistance was higher than in bulk-Si annealed with $T_2$ or $T_3$, although substantially lower than in bulk-Si annealed with $T_1$. Samples annealed...
with T₁ showed consistently higher values of sheet resistance than those annealed with T₂ or T₃ with the same Ge content. For samples annealed with T₁ and T₂, sheet resistance in SiGe showed a similar trend as a function of Ge content, increasing up to 6 at % Ge, then decreasing at higher concentration. For samples annealed with T₃, sheet resistance increased up to 4 at % Ge, then levelled off at 142 ± 1 Ω/sq. The main point of divergence between the annealing conditions was at 6 at % germanium, where the sample annealed with T₂ showed a sheet resistance of 149 ± 1 Ω/sq and the sample annealed with T₁ showed a sheet resistance of 165 ± 2 Ω/sq.

Figure 26 Sheet resistance as a function of Ge content, for B implanted at 20 keV in bulk-Si substrate and annealing conditions of: T₁ = 700°C, 20 min, T₂ = 700°C, 20 min. + RTA and T₃ = RTA only.

Figure 27 shows sheet resistance for analogous samples using SOI as a substrate instead of bulk-Si. For scaling reasons, the sheet resistance for the sample annealed at T₁ in bulk-SOI (1110 ± 11 Ω/sq) is omitted.

Again, for all samples implanted in Si₁₋ₓGeₓ, sheet resistance was substantially lower than in bulk-Si annealed with T₁, but higher than in bulk-Si substrate annealed with T₂ or T₃. Both sets of samples where RTA was involved (T₂ and T₃) showed similar values of sheet resistance within the same Ge content, differing only within
Results from Boron Implanted Samples

Experimental error. Samples which received furnace annealing only showed significantly higher values of sheet resistance, although presenting a similar trend. For all annealing conditions, the data showed a broadly similar trend, with sheet resistance increasing up to 6 at %, then levelling off for samples annealed with T₂ or T₃, although continuing to rise in the samples annealed with T₁. The sheet resistance increased from a minimum value of 121 ± 1 Ω/sq for boron implanted in bulk-SOI substrate (0 at % Ge) and annealed with T₂ to a maximum value of 152 ± 1 Ω/sq, for the sample with 9 at % Ge peak concentration and annealed with the same annealing condition and up to 191 ± 2 Ω/sq for the sample with the same germanium content but annealed with T₁.

![Image of graph showing sheet resistance as a function of Ge content.](image)

Figure 27 Sheet resistance as a function of Ge content, for B implanted in SOI substrate at 20 keV and annealing conditions of T₁, T₂ and T₃.

Table 4 shows the values of sheet resistance in 20 keV B doped samples, for all the annealing conditions as a function of germanium content in the Si₁₋ₓGeₓ alloy layers, using bulk-Si and SOI material substrates, where the germanium peak concentration varies between 1 at % and 9 at %. The data are compared with those in bulk-Si or SOI substrates (0 at % Ge).

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Table 4. Values of $R_s$ in bulk-Si and in SOI for various Ge content and annealing temperature, where $T_1 = 700^\circ$C, 20 min, $T_2 = 700^\circ$C, 20 min + RTA at $1050^\circ$C, 10 sec and $T_3 =$ RTA only.

<table>
<thead>
<tr>
<th>Ge content (at % peak conc.)</th>
<th>Annealing Conditions</th>
<th>$R_s$ (\Omega/sq)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Bulk-Si substrate</td>
</tr>
<tr>
<td>0</td>
<td>$T_1$</td>
<td>1700 ± 17</td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>121 ± 1.2</td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>121 ± 1.2</td>
</tr>
<tr>
<td>1</td>
<td>$T_1$</td>
<td>140 ± 1.4</td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>136 ± 1.4</td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>137 ± 1.4</td>
</tr>
<tr>
<td>4</td>
<td>$T_1$</td>
<td>150 ± 1.5</td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>142 ± 1.4</td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>142 ± 1.4</td>
</tr>
<tr>
<td>6</td>
<td>$T_1$</td>
<td>165 ± 1.7</td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>149 ± 1.5</td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>142 ± 1.4</td>
</tr>
<tr>
<td>9</td>
<td>$T_1$</td>
<td>150 ± 1.5</td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>141 ± 1.4</td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>142 ± 1.4</td>
</tr>
</tbody>
</table>

Values of Hall mobility were highest for the samples with 0 at % Ge annealed at $T_1$ (86.5 ± 0.9 cm$^2$/V-s for bulk-Si, 93.3 ± 0.9 cm$^2$/V-s for SOI). Values for the remaining samples varied between 32.0 ± 0.3 cm$^2$/V-s and 45.4 ± 0.5 cm$^2$/V-s. Selected data are plotted in Figure 28 and Figure 29.

Figure 28 shows the variation of the Hall mobility for samples implanted in bulk-Si. For scaling purposes, also in this case the value of Hall mobility (86.5 ± 0.9 cm$^2$/V-s) for the sample with 0 at % germanium peak concentration (bulk-Si) and annealed with $T_1$ is not reported in this graph. As a general trend, for all three annealing procedures, the Hall mobility decreases with increasing germanium content up to 6 at %, although there was an especially pronounced drop in mobility between 4 at % and 6 at % within the samples annealed with RTA only. Between 6 at % and 9 at %, Hall mobility increases for samples annealed with $T_1$ and especially with $T_3$, but remains stable (within experimental error) for samples annealed with $T_2$. 65
Figure 28 Hall mobility as a function of Ge content, for B implanted at 20 keV in bulk-Si substrate and annealing conditions of: $T_1 = 700^\circ$C, 20 min, $T_2 = 700^\circ$C, 20 min. + RTA and $T_3 = $ RTA only.

Figure 29 shows the variation in Hall mobility for analogous samples implanted in SOI material. The value of mobility ($93.3 \pm 0.9 \text{ cm}^2/\text{V-s}$) for the sample in bulk-SOI substrate (0 at \% Ge) and annealed with $T_1$ is not reported in the graph for scaling purposes. For all annealing conditions, values for SiGe are lower than those for bulk-SOI substrate. All three conditions show a similar trend with mobility increasing from 1 at \% Ge to 4 at \% Ge, then decreasing from 4 at \% Ge to 9 at \% Ge. For 3 of the 4 Ge concentrations investigated here, samples annealed with $T_3$ showed higher mobilities compared to the other annealing conditions. However, this relative advantage was not present in samples with 6 at \% germanium peak concentration.

Table 5 shows values of Hall mobility in 20 keV B doped samples, for all the annealing conditions as a function of germanium content in the Si$_{1-x}$Ge$_x$ alloy layers, using bulk-Si and SOI material substrates, where the germanium peak concentration varies between 1 at \% and 9 at \%.
Chapter 5

Results from Boron Implanted Samples

Figure 29 Hall mobility as a function of Ge content, for B implanted at 20 keV in SOI substrate and annealing conditions of: $T_1 = 700^\circ C$, 20 min, $T_2 = 700^\circ C$, 20 min + RTA and $T_3 = $ RTA only.

Table 5 Values of $\mu_B$ in bulk-Si and in SOI for various Ge content and annealing temperature, where $T_1 = 700^\circ C$, 20 min, $T_2 = 700^\circ C$, 20 min + RTA at 1050°C, 10 sec and $T_3 = $ RTA only.

<table>
<thead>
<tr>
<th>Ge content (at % peak conc.)</th>
<th>Annealing Conditions</th>
<th>$\mu_B$ (cm²/V·s)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$T_1$</td>
<td>Bulk-Si substrate</td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
5.2.1.2  Effect of Si post-amorphisation on $R_s$ and $\mu_H$

Figure 30 shows variation in sheet resistance as a function of Ge content for samples implanted in bulk-Si and annealed with $T_3$, with and without post-amorphisation. The data show small but complex effects of post-amorphisation depending on the Ge concentration, with sheet resistance reduced marginally at 1 at % Ge, and to a greater extent at 4 at % Ge, but increased more substantially at 6 at % Ge and marginally at 9 at % Ge.

![Figure 30 Comparison of sheet resistance as a function of Ge content for samples implanted with 20 keV B in bulk-Si substrate and annealed with $T_3$, with and without post-amorphisation.](image)

Figure 30 Comparison of sheet resistance as a function of Ge content for samples implanted with 20 keV B in bulk-Si substrate and annealed with $T_3$, with and without post-amorphisation.

Figure 31 shows analogous data for samples implanted in SOI material. The data show a small crossover, such that sheet resistance is slightly reduced by post-amorphisation at 0 at % Ge, varies within experimental error 1 at % Ge and 4 at % Ge, but is increased by post-amorphisation at 6 at % Ge and especially at 9 at % Ge.
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Figure 31 Comparison of sheet resistance as a function of Ge content for samples implanted with 20 keV B in SOI substrate and annealed with T3, with and without post-amorphisation.

Figure 32 Comparison of Hall mobility as a function of Ge content for samples implanted with 20 keV B in bulk-Si substrate and annealed with T3, with and without post-amorphisation.
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Figure 32 shows values of Hall mobility for the samples reported in Figure 30. Again, the effect of post-amorphisation is complex, whereby mobility is reduced at 1 at % Ge but is increased at 6 at % Ge, and is unaffected at both 4 and 9 at % Ge. The data show a similar trend in both sets of samples, but relatively smaller variation with germanium content.

Figure 33 shows values of Hall mobility for the samples reported in Figure 31. Again there is a complex pattern of effects, whereby post-amorphisation slightly increases the Hall mobility at 1 at % Ge and 6 at % Ge, substantially reduces it at 4 at % Ge, and makes no difference to the mobility at either 0 at % Ge or 9 at % Ge. Thus, with post-amorphisation, the peak in Hall mobility at 4 at % Ge, previously observed in Figure 29 is no longer present, and mobility shows a gradual decline with increasing Ge content.

![Figure 33: Comparison of Hall mobility as a function of Ge content for samples implanted with 20 keV B in bulk-Si and in SiGe (from 1 at % to 9 at % Ge).](image)

Figure 33 Comparison of Hall mobility as a function of Ge content for samples implanted with 20 keV B in bulk-Si and in SiGe (from 1 at % to 9 at % Ge). Again, the trend is the same for both sets of samples, with mobility reducing as germanium content increases.

5.2.1.3  SR and SIMS profiles

Figure 34 shows spreading resistance profiles of free carrier concentration as a function of depth for 20 keV B implanted in bulk-Si and in SiGe (from 1 at % to 9 at % Ge).
% Ge peak concentration) and annealed with $T_3$. In particular, for a background doping of $1 \times 10^{15}$ at/cm$^3$, the junction depth of B in silicon is $\sim 310$ nm, and progressively reduces with increasing germanium content down to just under 200 nm for the samples which contains 4 at % Ge peak concentration. For the highest germanium content (9 at %) though, the depth of the profile is at $\sim 220$ nm, which is higher than any of the germanium samples, but still below the sample in bulk-Si.

![Figure 34 SRP profiles for 20 keV B implanted into Si substrate and SiGe (1 at % to 9 at % Ge) and annealed with $T_3$.](image)

Figure 34 SRP profiles for 20 keV B implanted into Si substrate and SiGe (1 at % to 9 at % Ge) and annealed with $T_3$.

To summarise the trend: no significant difference between the samples prepared in bulk-Si substrate or in SiGe in the free carrier profiles up to a depth of $\sim 50$ nm. Between $\sim 50$ nm and $\sim 140$ nm, the samples prepared in bulk- Si substrate presents higher concentration of activated carriers, compared with the samples in SiGe. The remaining part of the profiles show a dependence of the activated carriers with germanium content.

Selected samples were then chosen for SIMS analyses. Figure 35 shows as-implanted profiles of 20 keV B in bulk-Si substrate and in SiGe (9 at % Ge), together with profiles of boron for the same samples after annealing with $T_3$.

Looking at the as-implanted profiles, the boron concentration peaks at the same depth of $\sim 70$ nm for both bulk-Si substrate and SiGe, although in the latter the tail of the distribution is shallower at $10^{18}$ ions/cm$^3$ atomic concentration. Again the tail of the boron profile in SiGe after annealing is significantly shallower ($\sim 240$ nm) than
the tail for boron implanted in bulk-Si substrate (~ 325 nm). However, the profile in SiGe after annealing shows greater diffusion towards the surface.

![Figure 35 SIMS profiles of 20 keV B in bulk-Si substrate and SiGe as-implanted and after annealing with T3.](image)

5.2.2 7 keV boron

5.2.2.1 \( R_s \) and \( \mu_H \) as a function of Ge content in bulk-Si and in SOI substrates

For all cases where data are available, samples annealed with \( T_1 \) show substantially higher values of sheet resistance than those annealed with \( T_2 \) or \( T_3 \). Data for the latter two annealing conditions are plotted in Figure 36 and Figure 37.

Figure 36 shows values of sheet resistance for samples implanted in bulk-Si substrate and annealed with \( T_2 \) and \( T_3 \). For both annealing conditions, the data show a very similar trend, with sheet resistance increasing up to 13 at \% Ge, then levelling off from 13 at \% Ge to 15 at \% Ge. The two annealing conditions vary within experimental error up to 6 at \% Ge. However, with higher values of Ge content, sheet resistance is increasingly higher in samples annealed with \( T_2 \) compared to those annealed with \( T_3 \).
Figure 36 Sheet resistance of 7 keV B as a function of germanium content and annealing conditions ($T_2$ and $T_3$) in bulk-Si substrate.

Figure 37 Sheet resistance of 7 keV B as a function of germanium content and annealing conditions ($T_2$ and $T_3$) in SOI.

Figure 37 shows analogous data for samples implanted in SOI substrate. The data show a similar trend to the previous graph. Sheet resistance increases with increasing
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Ge content up to 13 at % Ge, then declines slightly to 15 at % Ge. As with the preceding samples, from 10 at % Ge upwards, sheet resistance is slightly higher in samples annealed with $T_2$ compared to those annealed with $T_3$. However, at 0 at % Ge, sheet resistance was slightly lower in this annealing condition.

Table 6 shows values of sheet resistance in 7 keV B doped samples, for all the annealing conditions as a function of germanium content in the $\text{Si}_{1-x}\text{Ge}_x$ alloy layers, using bulk-Si and SOI material substrates, where the germanium peak concentration varies between 6 at % and 15 at %. The data are compared with those in bulk-Si or SOI substrates (0 at % Ge).

<table>
<thead>
<tr>
<th>Ge content (at % peak conc.)</th>
<th>Annealing Conditions</th>
<th>$R_s$ (Ω/sq)</th>
<th>Bulk-Si substrate</th>
<th>SOI substrate</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$T_1$, $T_2$, $T_3$</td>
<td>2540 ± 25</td>
<td>2690 ± 27</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>$T_1$, $T_2$, $T_3$</td>
<td>± 459 ± 5</td>
<td>463 ± 5</td>
<td>489 ± 5</td>
</tr>
<tr>
<td>10</td>
<td>$T_1$, $T_2$, $T_3$</td>
<td>629 ± 6</td>
<td>614 ± 6</td>
<td>628 ± 6</td>
</tr>
<tr>
<td>13</td>
<td>$T_1$, $T_2$, $T_3$</td>
<td>± 835 ± 8</td>
<td>755 ± 8</td>
<td>712 ± 7</td>
</tr>
<tr>
<td>15</td>
<td>$T_1$, $T_2$, $T_3$</td>
<td>± 1000 ± 10</td>
<td>934 ± 9</td>
<td>891 ± 9</td>
</tr>
</tbody>
</table>

Values of Hall mobility were highest for the samples with 0 at % Ge annealed at $T_1$ (117 ± 1 cm$^2$/V-s for bulk-Si substrate, 120 ± 1 cm$^2$/V-s for SOI substrate). Values for the remaining samples varied between 21.6 ± 0.2 cm$^2$/V-s and 53.6 ± 0.5 cm$^2$/V-s. Selected data from Table 7 are plotted in Figure 38 and Figure 39.

Figure 38 shows Hall mobility as a function of Ge peak concentration in bulk-Si for the three annealing conditions. In SiGe samples, values for $T_1$ are consistently lower than those for $T_2$ or $T_3$, while values for $T_3$ are mostly slightly higher than those for $T_2$. Additionally there is a tendency for Hall mobility to decrease with increasing Ge content, although this decrease is not uniform in $T_2$ and $T_3$ samples.
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Figure 38 Hall mobility of 7 keV B as a function of germanium content and annealing conditions in bulk-Si.

Figure 39 Hall mobility of 7 keV B as a function of germanium content and annealing conditions in SOI material.
Figure 39 shows analogous measurements for samples implanted in SOI substrate. As in the preceding graph, values for $T_1$ in SiGe samples are consistently lower than those for $T_2$ or $T_3$. Values for $T_2$ and $T_3$ are very close to each other. As before, there is a tendency for Hall mobility to decrease with increasing Ge content, although this trend is more pronounced in $T_1$ than in $T_2$ and $T_3$ samples.

Table 7 shows values of Hall mobility in 7 keV B doped samples, for all the annealing conditions as a function of germanium content in the $Si_{1-x}Ge_x$ alloy layers, using bulk-Si and SOI material substrates, where the germanium peak concentration varies between 6 at % and 15 at %. The data are compared with those in bulk-Si or SOI (0 at % Ge).

Table 7 Values of $\mu_H$ in bulk-Si and in SOI for various Ge content (0 at % Ge to 15 at % Ge) and annealing temperature, where $T_1 = 700^\circ$C, 20 min, $T_2 = 700^\circ$C, 20 min + RTA at 1050°C, 10 sec and $T_3 = $ RTA only.

<table>
<thead>
<tr>
<th>Ge content (at % peak conc.)</th>
<th>Annealing Conditions</th>
<th>$\mu_H$ (cm$^2$/V-s)</th>
<th>Bulk-Si</th>
<th>SOI</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$T_1$</td>
<td>117 ± 1</td>
<td>120 ± 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>53 ± 0.5</td>
<td>53.6 ± 0.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>52.8 ± 0.5</td>
<td>52.3 ± 0.5</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>$T_1$</td>
<td>29.9 ± 0.3</td>
<td>28.6 ± 0.3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>42.9 ± 0.4</td>
<td>42.5 ± 0.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>44.4 ± 0.4</td>
<td>44.9 ± 0.4</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>$T_1$</td>
<td>25.7 ± 0.3</td>
<td>24.4 ± 0.2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>36.8 ± 0.4</td>
<td>40.4 ± 0.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>42.3 ± 0.4</td>
<td>41.2 ± 0.4</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>$T_1$</td>
<td>22.9 ± 0.2</td>
<td>21.6 ± 0.2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>38.6 ± 0.4</td>
<td>39.9 ± 0.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>37.8 ± 0.4</td>
<td>40.5 ± 0.4</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>$T_1$</td>
<td>22.2 ± 0.2</td>
<td>21.6 ± 0.2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>37.4 ± 0.4</td>
<td>39.6 ± 0.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>39.6 ± 0.4</td>
<td>37.8 ± 0.4</td>
<td></td>
</tr>
</tbody>
</table>

5.2.2.2 Effect of Si post-amorphisation on $R_s$ and $\mu_H$

Figure 40 shows variation in sheet resistance as a function of Ge content for samples implanted in bulk-Si and in SOI substrates and annealed with $T_3$, with and without post-amorphisation. Especially at higher Ge peak concentrations (13 at % Ge and 15 at % Ge), post-amorphisation led to an increase in sheet resistance.
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Figure 40  Sheet resistance of 7 keV B as a function of Ge peak concentration for samples annealed with $T_3$. Samples in bulk-Si are compared with samples in SOI substrate (solid lines) and both are compared with samples that were post-amorphised (PA) (dashed lines).

Figure 41  Hall mobility of 7 keV B as a function of Ge peak concentration for samples annealed with RTA. Samples in bulk-Si are compared with samples in SOI (solid lines) and both are compared with samples that were post-amorphised (PA) (dashed lines).
Figure 41 shows values of Hall mobility for the same samples. Here, post-amorphisation resulted in a reduction in Hall mobility for all values of Ge content and in both Si and SOI substrates, especially at lower concentrations of Ge (6 at % Ge and 10 at % Ge). A single exception was for 15 at % Ge in SOI substrate, where the effect of post-amorphisation was negligible (within experimental error).

5.2.2.3  **SR and SIMS profiles**

Spreading resistance profiles were acquired for boron implanted at 7 keV in bulk-Si substrate and in SiGe with germanium peak concentration varying from 6 at % to 15 at % and annealed with $T_3$. The data are reported in Figure 42. The figure shows a clear trend with less boron diffusion with increasing germanium peak concentration: all samples in SiGe show a lower junction depth (from ~ 90 nm for 6 at % Ge down to ~ 70 nm for 15 at % Ge) at $10^{15}$ atomic concentration, compared to the sample in bulk-Si substrate (~ 170 nm).

![SRP profile](image)

Figure 42 SRP profile for 7 keV B implanted into Si substrate and SiGe and annealed with $T_3 = 1050^\circ$C, 10".

As-implanted SIMS profiles of boron implanted in SiGe (6 at % Ge) and the germanium associated, are shown in Figure 43. The purpose of this graph is to show that, the boron profile was contained within the germanium profile and that both peak concentrations were positioned at the same depth of ~ 25 nm.
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Figure 43 SIMS profiles of 7 keV B as-implanted into SiGe (6 at% Ge) and 30 keV Ge as-implanted into bulk-Si substrate for synthesis purposes.

Figure 44 SIMS profiles for 7 keV B implanted in Si and SiGe and annealed with RTA only.
Figure 44 shows SIMS analysis of boron implanted in bulk-Si as-implanted and annealed with $T_3$ and in SiGe with germanium peak concentration of 13 at % and 15 at % annealed in the same condition. The peak of the boron distribution after annealing is closer to the surface in SiGe, than in bulk-Si as-implanted. Both samples in SiGe present a pile-up near the surface which is higher for the highest germanium content. The tails of the profiles show a reduction in boron diffusion in SiGe, compared to bulk-Si and a further reduction passing from SiGe with 13 at % Ge to 15 at % Ge. Both profile tails are within the boron profile as-implanted.

5.3. TEM characterisation of defects after SPEG

Figure 45 show XTEM micrographs on samples implanted with $3.48 \times 10^{14} \text{ cm}^{-2}$ $\text{B}^+$ at 7 keV and annealed with $T_3$, in bulk-Si (sample 12) (a) and in SiGe with 6 at % Ge peak concentration (sample 61) (b) The samples numbers are listed in Appendix A.

Figure 45 XTEM micrographs from samples implanted with $3.48 \times 10^{14} \text{ B}^+\text{cm}^{-2}$ at 7 keV and annealed with RTA at 1050°C for 10", in (a) bulk-Si (sample 12) and (b) in SiGe with 6 at % Ge peak concentration ($6.9 \times 10^{15} \text{ Ge}^+\text{cm}^{-2}$ at 30 keV) (sample 61).
The sample in bulk-Si, Figure 45 (a), shows no detectible presence of extended defects, whereas the sample in Si$_{0.94}$Ge$_{0.06}$ shows low density of End Of Range (EOR) defects at ~ 70 nm from the surface, below the former a/c interface.

Figure 46 shows bright field (a) and weak dark field (b) XTEM micrographs of the sample implanted with $3.48 \times 10^{14}$ cm$^{-2}$ B$^+$ at 7 keV and annealed with T$_{3}$, in SiGe with 15 at % Ge peak concentration (sample 64).

![Bright field (a) and weak dark field (b) XTEM micrographs of the sample 64](image)

The surface of the sample looks very damaged, with the presence of hairpin dislocations which extend along all the SiGe layer ($R_p \sim 26$ nm) up to the surface and not fully regrown; small regions of amorphous Ge are present near the surface (within ~ 25-28 nm).
Chapter 6

6. Results from arsenic implanted samples

6.1. Introduction

In this chapter are reported sheet resistance ($R_s$) and Hall mobility ($\mu_H$) measured on samples in Group (b), described in section 4.1. The atomic and electrical profiles are presented, from which the activation of arsenic has been determined. Finally, selected samples were observed by transmission electron microscopy to investigate the formation and location of extended defects.

6.2. Activation and carrier transport of $Si_{1-x}Ge_x$ doped with arsenic at 100, 30 and 10 keV.

This section is composed of three parts: section 6.2.1 reports the results for arsenic implanted at 100 keV into $Si_{1-x}Ge_x$, section 6.2.2 reports the results for arsenic implanted at 30 keV and section 6.2.3 reports the results for arsenic implanted at 10 keV. The data presented are from samples treated with three different annealing conditions: $T_1$ (furnace annealing at 700°C for 20 minutes), $T_2$ (furnace annealing plus RTA at 1050°C for 10 seconds) and $T_3$ (RTA only).

6.2.1 100 keV arsenic

6.2.1.1 $R_s$ and $\mu_H$ as a function of Ge content in bulk-Si substrate

In all graphs in this chapter, lines joining data points are included only as a guide for the eyes.

Figure 47 shows values of sheet resistance as a function of Ge content in the $Si_{1-x}Ge_x$ alloy samples for the three different annealing schedules. The solid line fits the samples which were annealed with $T_1$, the dashed line fits those samples which were annealed with $T_2$, and the dotted line fits the samples which were annealed with...
T₃. Values of sheet resistance in samples annealed with T₁ are consistently higher than the corresponding values for T₂ and T₃. In all three annealing conditions, the sheet resistance decreased with increasing Ge content up to a peak concentration of 4 at %, with a minimum value of 119 ± 1 Ω/sq after annealing at 700°C, 20min plus RTA. For higher Ge peak concentrations, sheet resistance increased with increasing Ge content with a maximum value of 144 ± 1 Ω/sq for Si₀·₉Ge₀·₉ annealed at 700°C, 20min.

![Sheet resistance as a function of Ge content](image)

**Figure 47** Sheet resistance as a function of Ge content, for As implanted at 100 keV and annealing conditions of: T₁ = 700°C, 20 min, T₂ = 700°C, 20 min. + RTA and T₃ = RTA only.

Figure 48 shows the variation in Hall mobility in the same samples. Hall mobilities in SiGe were consistently lower than that in bulk-Si substrate annealed with T₁. However, within the SiGe samples, Hall mobility was almost independent of Ge content, and varied only slightly with annealing condition, showing higher values for samples annealed with T₃.
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Figure 48 Hall mobility as a function of Ge content, for As implanted at 100 keV in Si and SiGe at 100 keV and annealing conditions of $T_1$, $T_2$, and $T_3$.

Table 8. Values of $R_s$ and $\mu_H$ for 100 keV As implanted in bulk-Si substrate and SiGe (0 at % Ge to 15 at % Ge) and annealed at $T_1 = 700^\circ$C, 20 min, $T_2 = 700^\circ$C, 20 min + RTA at 1050$^\circ$C, 10 sec and $T_3 = $ RTA only.

<table>
<thead>
<tr>
<th>Ge content (at % peak conc.)</th>
<th>Annealing Conditions</th>
<th>$R_s$ (\Omega/sq)</th>
<th>$\mu_H$ (cm$^2$/V-s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$T_1$</td>
<td>163 ± 2</td>
<td>137 ± 1</td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1</td>
<td>$T_1$</td>
<td>147 ± 1</td>
<td>67.3 ± 0.7</td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>134 ± 1</td>
<td>75.7 ± 0.8</td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>131 ± 1</td>
<td>87.8 ± 0.9</td>
</tr>
<tr>
<td>4</td>
<td>$T_1$</td>
<td>131 ± 1</td>
<td>64.7 ± 0.6</td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>119 ± 1</td>
<td>71.6 ± 0.7</td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>120 ± 1</td>
<td>74.1 ± 0.7</td>
</tr>
<tr>
<td>6</td>
<td>$T_1$</td>
<td>129 ± 1</td>
<td>64.6 ± 0.6</td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>121 ± 1</td>
<td>68.4 ± 0.7</td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>120 ± 1</td>
<td>70.7 ± 0.7</td>
</tr>
<tr>
<td>9</td>
<td>$T_1$</td>
<td>144 ± 1</td>
<td>68.6 ± 0.7</td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>138 ± 1</td>
<td>70.8 ± 0.7</td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>138 ± 1</td>
<td>73.1 ± 0.7</td>
</tr>
</tbody>
</table>
Table 8 shows values of sheet resistance and Hall mobility for all the annealing conditions as a function of germanium content in the Si_{1-x}Ge_x alloy layers, implanted with arsenic at 100 keV, using bulk-Si as substrate, where the germanium peak concentration varies between 1 at % and 9 at %. The data were compared to those in bulk-Si substrate (0 at % Ge).

6.2.1.2 Effect of Si post-amorphisation on $R_s$ and $\mu_H$

Figure 49 shows variation in sheet resistance as a function of Ge content for samples implanted in bulk-Si substrate and annealed with TRA, with and without post-amorphisation. With the exception of samples with 4 at % Ge, where there is no effect, post-amorphisation leads to an increase in sheet resistance.

![Graph showing variation in sheet resistance as a function of Ge content for samples implanted in bulk-Si substrate and annealed with TRA, with and without post-amorphisation.](image)

Figure 49 Comparison of sheet resistance as a function of Ge content for samples implanted with 100 keV As in bulk-Si substrate and annealed with RTA only, with and without post-amorphisation.

Figure 50 shows measurements of Hall mobility for the same samples. In this case, although there was no change in Hall mobility at 1 at % Ge, post-amorphisation substantially increased the Hall mobility for samples with 4 at % Ge to 9 at % Ge. For example, at 9 at % Ge, the mobility was increased by just over 20 %.
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6.2.1.3 SR profiles

Selected samples from this group were analysed by spreading resistance profiling. Figure 51 shows the free carrier concentration of arsenic implanted in SiGe, for values of germanium peak concentration varying from 1 at % to 9 at % after annealing with $T_3$. The peak position of the arsenic distribution for the sample with 9 at % germanium peak concentration, is closer to the surface than the samples with 4 at % and 1 at % Ge, with peak concentration depth at ~ 37 nm and between 40 and 50 nm, respectively.

The same set of samples were then analysed by spreading resistance profiling, with and without post-amorphisation, and the data are reported in Figure 52 in linear-linear plot. The data in SiGe with no PA are indicated with the square symbol, whereas the post-amorphised samples are indicated with the up-triangle symbol. The arsenic peak concentration of the free carrier distribution for the post-amorphised samples (dotted line) corresponds to the carrier peak concentration for arsenic as-implanted.
Results from Arsenic Implanted Samples

Figure 51: SRP profiles of 100 keV As in bulk-Si substrate for samples annealed with $T_3$.

Figure 52: SRP profiles of 100 keV As in SiGe, annealed with $T_3$, with and without Si post-amorphisation.
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The arsenic distribution of samples which were not amorphised showed a higher straggle distribution of 98.8 nm at FWHM compared to the straggle calculated for samples after post-amorphisation which was 93.4 nm for 9 at % Ge peak concentration after thermal treatment with $T_3$ samples.

6.2.2 30 keV arsenic

6.2.2.1 $R_s$ and $\mu_H$ as a function of Ge content in bulk-Si substrate

Figure 53 shows values of sheet resistance as a function of Ge content in the Si$_{1-x}$Ge$_x$ alloy samples for the three different annealing schedules. For all three annealing conditions, the sheet resistance decreased with increasing germanium content up to a peak concentration of 6 at %, with a minimum value of $203 \pm 2$ $\Omega$/sq after annealing with $T_1$. For higher germanium peak concentrations, sheet resistance increased with increasing germanium content with a maximum value of $492 \pm 5$ $\Omega$/sq for Si$_{1-0.15}$Ge$_{0.15}$ for the same annealing condition. Annealing condition made little difference to values of sheet resistance, except at higher concentrations of germanium (13 at % Ge and 15 at % Ge), where values for samples annealed with RTA only were significantly lower than for the other two annealing schedules.

![Figure 53 Sheet resistance of 30 keV As, as a function of germanium content and annealing temperature in bulk-Si substrate.](image)

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Figure 54 shows the variation of the Hall mobility for the same samples. In all three annealing conditions, the mobility increased with increasing germanium content up to 6 at %, then decreased, levelling off after 13 at % Ge. The highest value of Hall mobility was $116 \pm 1 \text{ cm}^2/\text{V-s}$ at 6 at % Ge annealed with $T_1$; the lowest value was $54.5 \pm 0.5 \text{ cm}^2/\text{V-s}$ at 15 at % Ge also annealed with $T_1$. Among the SiGe samples, Hall mobilities were higher under $T_1$ than under the other two annealing conditions for lower concentrations of germanium (6 at % to 10 at %), but were lower under $T_1$ for higher concentrations of germanium (13 at % to 15 at %).

![Graph showing Hall mobility as a function of germanium content and annealing temperature](image.png)

Figure 54 Hall mobility of 30 keV As as a function of germanium content and annealing temperature in bulk-Si substrate.

Table 9 shows values of sheet resistance and Hall mobility for all the annealing conditions as a function of germanium content in the $\text{Si}_{1-x}\text{Ge}_x$ alloy layers implanted with arsenic at 30 keV, where the germanium peak concentration varies between 1 at % and 15 at %. The data were compared to those in bulk-Si (0 at % Ge).
Table 9 Values of $R_s$ and $\mu_H$ in bulk-Si for various Ge content (0 at % Ge to 15 at % Ge) and annealing temperature, where $T_1 = 700^\circ C$, 20 min, $T_2 = 700^\circ C$, 20 min + RTA at 1050°C, 10 sec and $T_3 =$ RTA only.

<table>
<thead>
<tr>
<th>Ge content (at % peak conc.)</th>
<th>Annealing Conditions</th>
<th>$R_s$ (Ω/sq)</th>
<th>$\mu_H$ (cm²/V-s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$T_1$</td>
<td>384 ± 4</td>
<td>93 ± 0.9</td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>365 ± 4</td>
<td>64.6 ± 0.6</td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>364 ± 4</td>
<td>101 ± 1</td>
</tr>
<tr>
<td>6</td>
<td>$T_1$</td>
<td>203 ± 2</td>
<td>116 ± 1</td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>212 ± 2</td>
<td>104 ± 1</td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>207 ± 2</td>
<td>105 ± 1</td>
</tr>
<tr>
<td>10</td>
<td>$T_1$</td>
<td>208 ± 2</td>
<td>104 ± 1</td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>223 ± 2</td>
<td>89 ± 0.9</td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>233 ± 2</td>
<td>89.1 ±0.9</td>
</tr>
<tr>
<td>13</td>
<td>$T_1$</td>
<td>435 ± 4</td>
<td>56.7 ± 0.6</td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>430 ± 4</td>
<td>72.6 ± 0.7</td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>369 ± 4</td>
<td>70.8 ± 0.7</td>
</tr>
<tr>
<td>15</td>
<td>$T_1$</td>
<td>492 ± 5</td>
<td>54.5 ± 0.5</td>
</tr>
<tr>
<td></td>
<td>$T_2$</td>
<td>470 ± 5</td>
<td>71.6 ± 0.7</td>
</tr>
<tr>
<td></td>
<td>$T_3$</td>
<td>400 ± 4</td>
<td>75.7 ± 0.8</td>
</tr>
</tbody>
</table>

6.2.2.2 Effect of Si post-amorphisation on $R_s$ and $\mu_H$

Figure 55 shows variation in sheet resistance as a function of Ge content for samples implanted in bulk-Si substrate and annealed with $T_3$, with and without post-amorphisation. With the exception of samples with 0 at % Ge, post-amorphisation leads to a substantial increase in sheet resistance, eliminating the U-shaped trend observed earlier in Figure 53. In particular, at 10 at % Ge, post-amorphisation led to an increase in sheet resistance of just under 96%.
Chapter 6  
Results from Arsenic Implanted Samples

Figure 55 Sheet resistance of 30 keV As as a function of Ge peak concentration for samples annealed with $T_3$. Samples which did not receive post-amorphisation (solid lines) are compared with samples that were post-amorphised (PA) (dashed lines).

Figure 56 shows measurements of Hall mobility for the same samples. In this case, post-amorphisation led to a substantial increase in Hall mobility for all values of germanium peak concentration. In particular, at 13 at% Ge, post-amorphisation resulted in an increase in Hall mobility of just under 74%.

Overall, the samples which received post-amorphisation presented less sensitivity to the germanium content than those which were not post-amorphised.
Section 6

Results from Arsenic Implanted Samples

Figure 56 Hall mobility of 30 keV As as a function of Ge peak concentration for samples annealed with RTA. Samples which did not receive post-amorphisation (solid lines) are compared with samples that were post-amorphised (PA) (dashed lines).

6.2.2.3 SR and SIMS profiles

Samples implanted in bulk-Si and in SiGe with the whole range of germanium concentrations used in this work, were measured by spreading resistance profiling after annealing with $T_3$. Figure 57 shows the free carrier concentration profiles of these samples. All the samples in SiGe present a shallower junction depth, for a background doping of $10^{18}$ cm$^{-3}$, than the sample in bulk-Si substrate (~ 70 nm). However, the trend does not vary systematically with germanium content. The shallowest junction depth observed was for 13 at% germanium peak concentration at ~ 27 nm and increasing progressively for 6 at%, 15 at%, 10 at% and 0 at% Ge.

The same trend is followed by the percentage of dopant activation. The percentage of arsenic activation was calculated by comparing the integration of the SRP profiles with the retained dose of As determined from SIMS. Carrier activation ranged from 60% in bulk-Si, down to 21% in $\text{Si}_{1.015}\text{Ge}_{0.13}$, as listed in the insert to (Figure 56).
Figure 57 SRP profiles of 30 keV As implanted in bulk-Si substrate and SiGe (from 6 at % Ge to 15 at % Ge) and annealed with T3.

Figure 58 shows SIMS profiles for 30 keV As implanted into bulk-Si substrate and SiGe, as-implanted and after annealing with T3. The as-implanted arsenic peak distribution in bulk-Si and in SiGe (15 at % Ge) coincided at a depth of ~19 nm. The peak of the arsenic distribution after annealing is closer to the surface in SiGe, than in both the as-implanted samples. For all samples in SiGe, the profiles present a pile-up near the surface which is higher for the highest germanium content. After annealing the tails of the profiles show a reduction in arsenic diffusion in SiGe, compared to bulk-Si substrate. In particular, arsenic in bulk-Si diffused to a depth of ~85 nm at $10^{18}$ cm$^{-3}$ atomic concentration, whereas all samples in SiGe diffused to depths between 66 and 72 nm.
Figure 58 SIMS profiles of 30 keV As in bulk-Si substrate and SiGe (6 at % to 15 at % Ge) annealed with T₃.

6.2.3 10 keV As

6.2.3.1 $R_s$ and $\mu_H$ as a function of Ge content in bulk-Si substrate

Figure 59 shows values of sheet resistance as a function of Ge content in the Si₁₋ₓGeₓ alloy samples for the two different annealing schedules T₁ and T₃. For this energy, annealing condition T₂ was not used. In both annealing conditions, sheet resistance increases with increasing germanium content. However, this trend is considerably stronger in samples annealed with T₁ than with T₃. In bulk-Si substrate, values for both annealing conditions were similar, at $1388 \pm 14 \Omega$/sq for T₁, and $1325 \pm 13 \Omega$/sq for T₃. In Si₁₋₀.₁₅Ge₀.₁₅, corresponding values were, respectively, $3419 \pm 34 \Omega$/sq and $2181 \pm 22 \Omega$/sq.
Figure 59 Sheet resistance of 10 keV As implanted into bulk-Si substrate and SiGe (6 at % to 15 at % Ge) and annealed with $T_1$ and $T_3$.

Figure 60 Hall mobility of 10 keV As implanted into bulk-Si substrate and SiGe (6 at % to 15 at % Ge) and annealed with $T_1$ and $T_3$. 
Table 10 Values of $R_s$ and $\mu_H$ in bulk-Si for various Ge content (0 at % Ge to 15 at % Ge) and annealing temperature, where $T_1 = 700^\circ$C, 20 min and $T_3 = $ RTA at 1050°C, 10 sec only.

<table>
<thead>
<tr>
<th>Ge content (at % peak conc.)</th>
<th>Annealing Conditions</th>
<th>$R_s$ (\Omega/sq)</th>
<th>$\mu_H$ (cm$^2$/V-s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$T_1$, $T_2$, $T_3$</td>
<td>$1388 \pm 14$</td>
<td>$129 \pm 1$</td>
</tr>
<tr>
<td>6</td>
<td>$T_1$, $T_2$, $T_3$</td>
<td>$1451 \pm 14$</td>
<td>$88.2 \pm 0.9$</td>
</tr>
<tr>
<td>10</td>
<td>$T_1$, $T_2$, $T_3$</td>
<td>$1830 \pm 18$</td>
<td>$89.3 \pm 0.9$</td>
</tr>
<tr>
<td>13</td>
<td>$T_1$, $T_2$, $T_3$</td>
<td>$2521 \pm 25$</td>
<td>$91.9 \pm 0.9$</td>
</tr>
<tr>
<td>15</td>
<td>$T_1$, $T_2$, $T_3$</td>
<td>$3419 \pm 34$</td>
<td>$89.7 \pm 0.9$</td>
</tr>
</tbody>
</table>

Figure 60 shows Hall mobility measurements for the same samples. Values are consistently higher for samples annealed with $T_3$ than for furnace annealed samples. The former show a U-shaped trend, such that mobility decreases from $137 \pm 1$ cm$^2$/V-s in bulk-Si substrate to $115 \pm 1$ cm$^2$/V-s for 6 at % Ge, then increases to $138 \pm 1$ cm$^2$/V-s for 15 at % Ge. In furnace annealed samples, there is a simple disparity between silicon and SiGe samples: Hall mobility is $129 \pm 1$ cm$^2$/V-s in bulk-Si substrate and ranges from $88.2 \pm 0.9$ cm$^2$/V-s to $91.9 \pm 0.9$ cm$^2$/V-s in SiGe.

Table 10 shows values of sheet resistance and Hall mobility for all the annealing conditions as a function of germanium content in the Si$_{1-x}$Ge$_x$ alloy layers implanted with arsenic at 10 keV, where the germanium peak concentration varies between 1 at % and 15 at %. The data were compared to those in bulk-Si (0 at % Ge).
Chapter 7

7. Discussion

7.1. Introduction

In this chapter, possible explanations for the patterns of findings presented in Chapters 5 and 6 are discussed. Effects of the annealing conditions are considered briefly in section 7.2. Section 7.3 discusses effects of the germanium content on electrical properties (sheet resistance, mobility and carrier activation). Potential explanations of these findings in terms of (a) strain relaxation and (b) dopant diffusion and activation are outlined respectively in sections 7.4 and 7.5.

7.2. Influence of the annealing conditions

After implantation, some of the samples were annealed with furnace annealing only (T1), some of them with T1 plus RTA (T2) and some only with RTA (T3).

For all the samples listed in Chapter 5 and 6 (Tables 4, 5, 6, 7 and Tables 8, 9, 10, respectively), values of sheet resistance were consistently higher and values of Hall mobility consistently lower in samples which received furnace annealing only (T1), compared to those which received RTA (T2 and T3). The difference in these values between samples which received furnace annealing followed by RTA (T2) and those which received RTA only (T3) was within just 5%. This pattern of results is consistent with electrical results for heavily doped silicon and SiGe, where RTA is used to remove radiation damage and achieve dopant activation [137]. The furnace annealing condition chosen for this work at 700°C for 20 minutes, would have regrown the crystal structure (when amorphous) with partial electrical activation of the dopant, but temperatures of 900°C or above are necessary to fully activate the arsenic and boron [138, 139] and over ~1000°C to anneal residual defects, especially boron interstitial clusters or arsenic vacancy clusters [140].
Sheet resistance was especially high in B-doped samples in bulk-Si which did not receive RTA (e.g., 1700 $\Omega$/sq for 20 keV B in bulk-Si after $T_1$) and to a lesser extent in the alloy layers. In these cases, the implantation conditions would not have been sufficient to create an amorphous layer (see section 3.2); hence, damage is repaired by generation, annihilation and diffusion of point defects (see section 3.3 and [141]). This process of annihilation has a higher activation energy than the solid phase epitaxy process [141] and it requires temperatures of the order of 900 – 1000°C. In particular, Atzmon et al. [141] reported that for Sb$^+$ implanted in Si$_{0.90}$Ge$_{0.10}$ at a dose which was below the critical value for formation of a continuous amorphous layer ($\sim 10^{15}$ cm$^{-2}$), annihilation of the implantation damage was achieved only at temperatures between 800 and 900°C in N$_2$ atmosphere, when a maximum of carrier activation was recorded. An analogous experiment was carried out by the same authors, implanting Sb$^+$ to a dose which was above the amorphisation threshold; in this case, re-crystallisation by SPEG was achieved at temperatures between 500 and 600°C. Moreover, Zou et al. [142] reported that residual damage caused by high energy Ge$^+$ (400 keV) and BF$_2^+$ (300 keV) implantation was removed only at temperatures of 950°C (in N$_2$ and Ar$_2$ atmosphere) and above. In addition, Downey et al. [143] reported a systematic study on the annealing parameters to produce ultra-shallow, highly activated B$^+$, BF$_2^+$ and As$^+$ implanted junctions. In particular, they observed a reduction in junction depth at $1 \times 10^{17}$/cm$^3$ of 320 Å and reproducible data, for 1 keV and 2 keV implanted B$^+$ in silicon, using a "standard" annealing condition of 1050°C, 10" (40°C/s ramp-rate, 750°C 10" stabilisation step and 27°C/s cool), when the level of background O$_2$ (which was causing oxidation enhanced diffusion, OED, by injecting Si-interstitials) was monitored and reduced to a minimum level of 33 ppm. The ramp-rate alone (compared to spike ramp-rate of 240°C/s) did have negligible effects on boron activation and diffusion. However, a significant reduction in junction depth was found for those samples which received a fast cool down rate (from standard at 27°C/s to fast 86°C/s).

In this work, a N$_2$ atmosphere was used to perform all the annealing (see section 4.2.4). Moreover, TEM analyses (see section 5.3) on samples annealed with $T_3$, show that the residual implantation damage was fully removed even in samples where an amorphous layer was not formed after implantation (B in bulk-Si). Hence the discussion which follows focuses especially on those samples annealed with RTA.
7.3. Influence of germanium content on electrical properties

7.3.1 Credibility and reproducibility of measured values

Values of sheet resistance of B-doped layers in bulk Si and SOI wafers differed mostly within experimental error of ±1%. Since the current flow into the substrate in the SOI wafers is blocked by the buried oxide layer, the close correspondence in sheet resistance indicates that low-leakage p-n junctions were generated also in the samples implanted in bulk-Si wafers. It is also assumed that no significant leakage occurred in the As-doped samples, since n-p junctions were formed by the same process (see section 4.2).

The reproducibility of the measurements was tested through repeated measurements of the same samples made at various time intervals (30 seconds up to 6 months). The scatter in these measurements was within ±1%.

As discussed in section 4.3.2, values of carrier concentration derived from the SRP measurements had a notional accuracy of ±2.5%. However, since the bulk Si mobility was used to extract carrier concentrations in SiGe, and given uncertainty about the crystal quality of the material and actual carrier mobility in IBS SiGe, there remains the possibility of significant systematic errors. Since these errors remain unknown at present (see section 4.3.2), it is impossible to establish a reliable confidence limit in determining carrier concentration profiles from SRP measurements in IBS SiGe. Hence the carrier concentration profiles reported here, and all proposed values of \( N_s, \mu_B, \tau_H \) and \( X_{si} \) which were calculated using them, must necessarily be treated as speculative. These values should be taken to indicate possible trends and not absolute measurements.

Assuming an uncertainty of ±3% in atomic concentration and ±1% in profile depth in the SIMS measurements, the sheet atomic concentration is estimated to have an uncertainty of ±3.2% \(^1\) [144].

7.3.2 Trends in sheet resistance

Values of sheet resistance in the silicon control samples (0% Ge) for both dopants at all implantation energies are within the range of values published elsewhere in the

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\(^1\) For calculations with \( n \) independent sources of error, \( e_1, e_2 \ldots e_n \), combined error was calculated according to the formula \( \sqrt{\sum_{i=1}^{n} (e_i)^2} \) [144].
literature \([82, 145, 146]\) for annealing temperatures ranging from 750°C up to 1100°C and boron or arsenic peak concentration between \( \sim 10^{18} \) and \( \sim 10^{21} \) (400 to 525 \( \Omega \)/sq for 7 keV B; 120 to 125 \( \Omega \)/sq for 20 keV B; 170 \( \Omega \)/sq to 200 \( \Omega \)/sq for 100 keV As; 350 \( \Omega \)/sq to 550 \( \Omega \)/sq for 30 keV As; and 1000 \( \Omega \)/sq to 2010 \( \Omega \)/sq for 10 keV As).

A summary of values of sheet resistance as a function of the germanium peak concentration (\(0 \leq x \leq 0.09\) for 100 keV Ge and \(0 \leq x \leq 0.15\) for 30 keV Ge) for boron implanted at 7 and 20 keV, respectively in silicon and SOI and annealed with RTA, is shown in Figure 61. As reported in chapter 5, the overall trend shows an increase in sheet resistance as a function of germanium content up to the maximum value investigated at 15 at% for all the annealing conditions used here.

Figure 62 shows a comparison of sheet resistance measurements as a function of germanium content for the three arsenic implantation energies, again for samples annealed with RTA only, which exhibited the lowest values of sheet resistance. The two deeper implants (100 keV and 30 keV) show similar U-shaped trends as a function of germanium content, whereas the shallower implant (10 keV) shows a slight increase in sheet resistance with increasing germanium content.

![Figure 61 Sheet resistance as a function of Ge peak concentration for both 7 keV and 20 keV B implanted into bulk-Si and SOI and annealed with RTA at 1050°C for 10" (T3)](image)

100
Figure 62 Comparison of sheet resistance of As implanted at 100, 30, and 10 keV in Si and SiGe (1 at % to 10 at % Ge) and annealed at 1050°C for 10 seconds.

These results contrast with published results for SiGe layers grown by MBE/CVD [147, 148, 149], which have generally shown a reduction in sheet resistance with increasing germanium content up to 30%, in both n-type and p-type layers.

Considering that the sheet resistance is $R_s \propto 1/\mu N_s$, the trends in sheet resistance observed here must be related to corresponding trends in $\mu$ and/or $N_s$. For example, the increase in sheet resistance with increasing germanium content, observed in the B-doped samples, is attributable to a corresponding decrease in either the drift mobility or the number of activated carriers, or both. It should be noted also that the carrier activation and mobility are normally expected to have an inverse relationship at room temperature owing to the predominant effect of the impurity scattering over the lattice scattering [150]. In the next two sections, respectively, the dopant activation and the mobility are discussed.

7.3.3 Carrier activation

For all samples where both SIMS and SRP data were available, speculative values of the percentage of activated carriers were derived for each sample by integration under the two corresponding curves. Given uncertainty about the accuracy of the
SRP carrier concentration profiles (see sections 4.3.2 and 7.3.1), the values proposed should not be taken as absolute values, but as an indication of possible trends in carrier activation with varying Ge content. Figure 63 compares the dopant atomic profiles from SIMS with the derived free carrier distribution from SRP for 30 keV arsenic in bulk-Si and in SiGe (10 at % Ge), after annealing with RTA only. In both cases the SRP profile shows a box shape, with lower activation in both the peak and the tail, compared to the SIMS profiles. Integration under these curves was used to calculate the percentage of activated carriers. The activation of arsenic in bulk-Si was almost 60%, where the main concentration of activated carriers was within the first 70 nm. In SiGe the proposed percentage of carriers activated was 55% of the actual dose extracted from the SIMS profile with the main concentration of the activated carriers within the first 50 nm (considering the electrical junction depth at $10^{18}$ ions/cm$^3$). For the samples implanted with arsenic at 100 keV, where SIMS data were not available, the nominal dose was used as an estimate of the actual dose.

![Figure 63 Comparison between SIMS atomic profiles and proposed free carrier concentration profiles from SRP for 30 keV As in Si and SiGe (10 at% Ge) and annealed with RTA.](image)

Proposed values of percentage carrier activation for B-doped and As-doped samples are described in Figure 64 and Figure 65, respectively. For both dopants, the
shallower implants show lower values of carrier activation than the deeper implants. This is consistent with published results for boron implanted into silicon: from Hall-van der Pauw measurements, Collart et al. [151] found that, with decreasing implantation energy of boron into bulk-Si from 10 keV to 100 eV, carrier activation became increasingly difficult. After considering an explanation in terms of boron clustering, they argued that this trend was attributable to boron trapping and deactivation at the surface; a similar explanation of the current results is developed in section 7.5.2.

For each implantation energy, Figure 64 clearly shows an inverse pattern to that of the sheet resistance values reported in Figure 61: for 7 keV boron, the steady increase in sheet resistance with increasing germanium content is matched by a corresponding decrease in carrier activation; for the 20 keV boron, the sharp increase in sheet resistance from 0 to 1 at % Ge in particular is matched by a sharp decrease in carrier activation. This indicates that the disparity between the trends reported here of sheet resistance for B-doped SiGe samples and those reported elsewhere for epitaxy material [147, 148, 149], must be at least partly attributable to a failure to activate the dopant.

![Figure 64 Proposed percentage of free carrier activation for boron implanted at 20 and 7 keV in bulk-Si and SiGe after RTA at 1050°C for 10" (T3).](image)

Figure 64 Proposed percentage of free carrier activation for boron implanted at 20 and 7 keV in bulk-Si and SiGe after RTA at 1050°C for 10" (T3).
Proposed values of carrier activation for As-doped samples shown in Figure 65 are less clearly related to values of sheet resistance for these samples shown in Figure 62, although there is some correlation. For samples implanted with 100 keV As, an inverted U-trend is apparent, corresponding with the U-trend observed in sheet resistance. For samples implanted with 30 keV As, the sharp increase in sheet resistance observed between 10 and 13 at % Ge is matched by a sharp decrease in carrier activation; on the other hand, the reduction in sheet resistance from 0 to 6 at % Ge is accompanied by a decrease in carrier activation, from which it can be concluded that the sheet resistance trend here must be explained in terms of changes in the mobility.

7.3.4 Hall and Drift mobility

Measurements of channel, Hall and drift mobility in SiGe layers grown by MBE/CVD have typically shown rising values with increasing germanium content [147, 148, 149]. In the work presented here, measures of Hall mobility typically decreased with increasing germanium content (see sections 5.2.1.1, 5.2.2.1, 6.2.1.1, 6.2.2.1 and 6.2.3.1). However, several authors [13, 152, 153, 154, 155] have argued...
that Hall mobility measurements are not the most appropriate measure of carrier 
transport properties at room temperature. The main reason for this is intrinsic to the 
Hall method (see section 4.3.1). The carriers which move perpendicular to the 
magnetic field applied $B_z$, will be deflected from their direction of motion by the 
Lorenz force. This deflection will cause a Hall voltage across the sample, which is 
given by [155]:

$$V_H = R_H I_x B_z / d,$$  \hspace{1cm} Eq. 7.1

where $d$ is the sample thickness in the direction of the magnetic field, $I_x$ is the current 
through the sample and $R_H$ is the Hall coefficient. The Hall coefficient can also be 
expressed as [155]:

$$R_H = r_H / (Ne),$$  \hspace{1cm} Eq. 7.2

where $N$ is the carrier concentration, $e$ is the electric charge and $r_H$ is the Hall 
scattering factor. The Hall mobility is then defined as the product of the conductivity, 
$\sigma$, and the Hall coefficient and is related to the drift mobility, $\mu_D$, as follows [155]:

$$\mu_H = \sigma R_H = eN\mu_D / Ne = r_H \mu_D$$ \hspace{1cm} Eq. 7.3

Thus the Hall scattering factor, $r_H$, is the conversion factor needed to determine 
both the actual carrier concentration and the drift mobility from Hall measurements. 
However, a problem in determining $r_H$ is that it is not possible to measure 
independently the drift and Hall mobilities nor the absolute carrier concentration and 
the Hall carrier concentration.

By convention, the Hall carrier concentration ($N_H$) and the Hall mobility ($\mu_H$) are 
calculated from $R_H$, using the approximation $r_H = 1$ (see section 4.3.1), which leads 
to $\mu_H = \mu_D$. However, a theoretical analysis shows that the approximation $r_H = 1$ is 
not always adequate. A method to estimate the Hall scattering factor was presented 
by Joelsson et al [155], using the relationship: $r_H = N / N_H = (N / N_b)(N_b / N_H)$, 
with $(N/N_b)$ being the degree of ionisation, obtained from a theoretical calculation 
[156], and $(N_b/N_H)$ being the ratio between the concentration of boron atoms 
estimated from the conductivity of a Si reference sample and the experimentally
measured Hall carrier concentration. In SiGe, the degree of ionisation is expected to increase with increasing germanium content, owing to a reduction in the ionisation energy due to bandgap narrowing. Therefore, in order not to underestimate \( \frac{N}{N_B} \), the bandgap narrowing as a function of germanium content, has to be taken into account in calculating \( r_H \). According to the work of Mamontov et al. [156], for doping concentrations up to \( \sim 3 \times 10^{18} \text{ cm}^{-3} \), calculations of \( r_H \) are insensitive to the choice of method or model, and one can assume that the carrier concentration depends mainly on the ionisation energy. However, for higher concentrations (up to \( \sim 2 \times 10^{20} \text{ cm}^{-3} \)) a substantial proportion of the dopants may not be ionised and further complications, such as carrier-carrier scattering and temperature dependent bandgap narrowing, must also be considered.

Figure 66 Hall scattering factor \( r_H \) in B-doped SiGe layers grown by MBE as a function of germanium content (at %), from data obtained by Lu et al [154] and by Joelsson et al [155].

Figure 66 shows values of \( r_H \) as a function of germanium concentration, from data collected by Lu et al [154] and by Joelsson et al [155] for strained B-doped Si\(_{1-x}\)Ge\(_x\) grown by MBE where \( 0 \leq x \leq 0.24 \) with a B concentration between \( 2 \times 10^{18} \) and \( 7.5 \times 10^{18} \text{ cm}^{-3} \) at room temperature. These data show the deviation from a value of unity for the Hall scattering factor in alloy layers: here, values of the Hall
scattering factor are consistently below unity, decreasing from ~0.7 in bulk-Si to ~0.4 in SiGe with ≥ 15 at % Ge.

The availability of values of Hall scattering factor for B-doped samples in the literature [154, 155] provides a means of estimating the drift mobility (μD) from direct measurements of Hall mobility, according the relation $\mu_D = \mu_H / r_H$, for those samples doped with boron [13]. However, a complication arises in ion beam synthesised SiGe due to the depth dependence of the layer composition, which gives graded SiGe interfaces rather than layers of homogeneous composition. Hence, in ion beam synthesised SiGe, it is not clear whether the effects of germanium content on the bandgap, which influence $r_H$, will be the same as in SiGe layers grown by MBE/CVD. Furthermore, the dopant concentrations used in this work were more than one order of magnitude greater than those used by the authors referenced above (~$1 \times 10^{20}$ cm$^{-3}$), and the shallower implants formed considerably thinner layers (~70 nm) than those referred to in Figure 66 (typically ~150 to ~220 nm, similar to the deeper implants performed here).

An alternative route to estimating the drift mobility is through the relation, $R_s = 1/\mu eN_s$, discussed earlier (section 7.3.2): according to this relation, it is possible to estimate the drift mobility independently of Hall mobility measurements, as a function of the sheet resistance ($R_s$) and free sheet carrier concentration ($N_s$): $\mu = 1/R_s eN_s$. In the early 1990's, McGregor and colleagues [157] used this relation to estimate the drift mobility of boron (1.5-2.1 $\times 10^{19}$ cm$^{-3}$) in SiGe grown by MBE with germanium concentration up to 20%, approximating the sheet carrier concentration from SIMS analysis assuming 100% boron activation.

However, the availability of speculative values of carrier concentration from SRP measurements reported in this thesis, makes it possible to propose corresponding values of drift mobility without assuming 100% dopant activation. For those samples measured by SRP in this work, speculative values of drift mobility were calculated using the formula, $\mu = 1/R_s eN_s$. Additionally, speculative values of the Hall scattering factor were derived by comparing the calculated values of drift mobility with the measured values of Hall mobility for each sample.

It is important to reiterate that the values of carrier concentration used in these calculations were derived assuming a value of bulk Si mobility in the absence of experimental values for IBS SiGe. Hence, the values of $\mu_D$ and $r_H$ proposed here should not be taken as absolute values, but may indicate possible trends in these
parameters (see section 7.3.1). Nevertheless, the use of bulk Si mobility is currently accepted for general use in SRP analyses [131, 132, 134, 135, 136], and is also used in modelling software such as SILVACO ATLAS [133] to estimate electrical characteristics of SiGe material for device purposes. In addition, in the work presented here, the germanium peak concentrations used were relatively low (up to 15 at % Ge) and the dopant concentration was relatively high \( (10^{20} \text{ cm}^{-3}) \); under these conditions the SiGe alloy scattering is considered negligible, as the main scattering effect is assumed to be due to impurity scattering [152].

In order to test the sensitivity of the obtained values of carrier concentration to the value of bulk mobility used, additional calculations were made by Semiconductor Assessment Services Ltd., varying the bulk mobility over a range of 50\% (± 25\%). Resulting estimates varied over a range of ± 10\%. This suggests that the values of carrier concentration reported here may be comparatively reliable.

Some further confidence in the results presented here is given by the close agreement of values of \( n_h \) proposed here for the higher energy boron implants (100 keV) with the values reported in the literature for MBE/CVD strained SiGe layers, obtained using different estimation methods [154, 155]. Figure 67 compares the calculated values of \( n_h \) for both B- and As-doped samples in this work, with the published values for B-doped MBE/CVD SiGe layers previously reported in Figure 66. They show a very good agreement for the higher energy implants.

However, contrary to the general trend of a reduction in the Hall scattering factor with increasing germanium content, the trends for all four sets of samples show a noticeable increase in proposed values of \( n_H \) for the higher values of germanium content investigated. A possible explanation is that the SiGe layer had relaxed in these samples (this suggestion is developed in section 7.4 below), in which case a different set of factors should have been involved in determining the Hall scattering factor. Values for the 20 keV B implants were close to the published data over the middle range of germanium concentrations (from 1 to 6 at % Ge), but values for the 7 keV B implants were considerably lower. It is worth noting that the thickness of the SiGe layer for the higher energy implants was similar to those in the literature (≈200 nm) whereas the layer created by the lower energy implants was much thinner (≈70 nm). We can speculate that the lower values of \( n_H \) in the thinner layers can be attributed to a stronger trapping-effect of the surface in these samples, and therefore a lower carrier activation [151].
Figure 67 Speculative values of Hall scattering factor \( r_H \) as a function of germanium content (at \%), in B-doped SiGe, compared with data obtained by Lu et al [154] and by Joelsson et al [155].

Figure 68 Speculative values of drift mobility as a function of Ge peak concentration for samples implanted with 20 keV B or with 7 keV B after RTA.
Speculative values of drift mobility as a function of Ge peak concentration for samples implanted with 100 keV As or with 30 keV As after RTA except for the sample with 100 keV As in bulk-Si, which was annealed with T1.

Speculative values of drift mobility for both B- and As-doped samples are summarised in Figure 68 and Figure 69, respectively. Comparing these values with the measurements of Hall mobility reported in chapters 5 and 6, it is apparent that they are larger, in some cases by as much as 200-300% (e.g. for Si0.9Ge0.1 with 7 keV B, the proposed drift mobility is 179 cm²/V-s whereas the Hall mobility is just 42 cm²/V-s). This is consistent with values of $r_H$ being less than unity. Furthermore, in many cases the Hall and proposed drift mobilities show opposite trends with increasing germanium content, as found elsewhere for epitaxially grown material [157]: while values of Hall mobility generally show a downward trend with increasing germanium content, the trends in proposed drift mobility are more complex, with only the values for 100 keV As showing a comparable downward trend. On the other hand, proposed values of drift mobility for 30 keV As and for the B-doped samples show forms of inverted U-trend, increasing up to intermediate values of germanium content, then declining.

Comparing these trends with the corresponding results for sheet resistance and carrier activation, it can be seen that the trends observed in sheet resistance are in general more closely related to the proposed values of carrier activation than to those of drift mobility. In samples implanted with 7 keV B, a steady rise in sheet resistance
with increasing germanium is accompanied by an inverse trend in carrier concentration. However the sharp peak in mobility at 10 at % Ge is not reflected in either of these trends. In samples implanted with 20 keV B, the increase in sheet resistance from 0 to 1 at % Ge occurs despite a rise in mobility, but is related to a reduction in carrier activation over the same range of germanium content. In samples implanted with 100 keV As, mobility falls slightly over the range of germanium content, whereas the U-trend in sheet resistance is clearly reflected in an inverted U-trend in carrier activation.

In samples implanted with 30 keV As, it is necessary to consider the mobility in order to account for the trend in sheet resistance. As noted above (see section 7.3.3), the sharp decrease in sheet resistance from 0 to 6 at % Ge in these samples cannot be explained in terms of an increase in carrier activation because carrier activation also falls over this range of germanium content. On the other hand, the proposed values of drift mobility rise by over 100% over the same range. Also the Hall mobility rises over this range, from 101 cm$^2$/V·s in bulk-Si to 125 cm$^2$/V·s in 6 at % Ge—despite the opposing influence of the Hall scattering factor, from which is predicted a greater underestimation of drift mobility with increasing germanium content—showing the reliability of this increase in mobility using two completely independent measurement techniques. Thus in these samples it is an increase in mobility which accounts for the reduction in sheet resistance.

7.4. Strain relaxation

Both TEM analyses and electrical results provide evidence that alloy layers with the highest values of germanium content (13 and 15 at % Ge in the shallower implants, and 9 at % Ge in the deeper implants) had relaxed during annealing ($T_3$).

7.4.1 Evidence from TEM analysis

In TEM analyses on selected samples (see section 5.3), the sample implanted with 7 keV boron in silicon shows no detectable presence of extended defects and a good crystalline quality of the regrown layer. However, the sample which contains 6 at % germanium shows the presence of EOR defects at a depth just below the amorphous/crystalline interface (~ 50 nm) prior to SPEG. The density of these defects was at the limit of the TEM detection and thus the areal density was estimated to be between $\sim 10^5$ and $\sim 10^6$ cm$^{-2}$. Overall this sample also presented a good crystalline quality (see Figure 45).
In contrast, in both bright and weak beam dark field TEM micrographs (see Figure 46), the sample with 15 at % Ge peak concentration shows a very highly damaged surface with the presence of hairpin dislocations, which extend up to the surface from a depth of ~100 nm, just below where the former a/c interface was located before SPEG, together with pockets of amorphous Ge within the same region. These features provide clear evidence that the critical Ge peak concentration was exceeded in this sample and that the layer had relaxed during annealing (see section 2.4).

![Figure 70](image)

Figure 70. Combined figure of a TEM micrograph and SIMS profile on sample 64 (7 keV B in SiGe with 15 at % Ge peak concentration and annealed with RTA at 1050°C for 10 sec).

Figure 70 shows a TEM micrograph with a superimposed SIMS profile from the sample described above. As shown in the figure, the entire boron distribution (~70 nm at $10^{18}$ cm$^{-3}$) lies well inside the damaged layer (~100 nm). This helps to explain why the electrical properties degrade especially in samples with high germanium content. Moreover, as discussed subsequently (see section 7.5.1) the presence of EOR defects even in samples with lower germanium content, compared to the absence of detectable defects in bulk-Si, may also contribute to the increase in sheet resistance over the range of the germanium content studied here.
7.4.2 Evidence from electrical measurements

The TEM observation of strain relaxation in the sample illustrated in Figure 70 is consistent with the comparatively high value of sheet resistance (897 Ω/sq) and comparatively low proposed values of carrier activation (22%) and drift mobility (133 cm²/V-s) in this sample (see Figure 36, Figure 64 and Figure 68). However, inspection of the trends in these properties with germanium peak concentration over the range from 0 at % to 15 at % suggests further that relaxation in the 7 keV B samples may have happened also with 13 at % Ge. In particular, the sheet resistance rises steadily up to (904 Ω/sq) at this germanium concentration and then levels off (see Figure 61), while the proposed drift mobility rises up to 10 at % Ge and then falls through 13 to 15 at % Ge (see Figure 64). Both of these trends show turning points in the region between 10 and 13 at % Ge.

![Figure 71](image)

**Figure 71** The effective density of states for strained and unstrained SiGe as a function of Ge fraction. The values have been normalised to the value obtained at 0 % Ge (3.1×10¹⁹ cm⁻³), which correspond to value for Si (from ref. [149]).

Further evidence for the occurrence of strain relaxation at 13 at % Ge comes from speculated values of the Hall scattering factor for samples implanted with 7 keV B reported in Figure 67. For germanium concentrations up to 10 at % Ge, the
calculated Hall scattering factor decreases from 0.58 to 0.24, consistent with the expected trend in strained SiGe. However this trend is then interrupted as the values increase to 0.25 at 13 at % Ge and 0.30 at 15 at % Ge. As discussed by Manku et al [149], with increasing germanium content in strained SiGe alloy, the effective density of states in the valence band decreases (a theoretical explanation is given in ref. 149), resulting in a corresponding decrease in the Hall scattering factor and an increase in drift mobility; however, the effective density of states is higher in unstrained compared to strained SiGe (see Figure 71), resulting in higher values of the Hall scattering factor and lowered values of drift mobility [149]. Assuming that strain relaxation had occurred in the Si$_{0.87}$Ge$_{0.13}$ and Si$_{0.85}$Ge$_{0.15}$ layers, these considerations would predict exactly the pattern of results observed here.

Results from samples implanted with 30 keV arsenic, show similar trends, but with some variations. As with the B-doped samples, there is a sharp decrease in mobility and a sharp increase in the calculated Hall scattering factor with high germanium content, but this is restricted to the samples with 15 at % Ge. Nevertheless, from 10 to 13 at % Ge, there is a drop in the proposed value of carrier activation from 52% down to 20% of the implanted dose. This would account for the apparent increase in drift mobility over the same range, since the reduced number of carriers will lead to a corresponding reduction in carrier-carrier scattering, a key factor in determining both the Hall scattering factor and the drift mobility for higher dopant concentration [134, 149].

Furthermore, it is suggested that also in samples with 9 at % Ge in the deepest implants strain-relaxation of the alloy may have occurred. Although values of sheet resistance, carrier activation and drift mobility do not show a clear turning point, there is a clear upturn in the calculated Hall scattering factor at this germanium content for B-doped samples: at lower germanium peak concentrations, values of $r_{HH}$ closely follow the available published values for layers of a similar thickness, decreasing from 0.70 in Si$_{0.99}$Ge$_{0.01}$ to 0.60 in Si$_{0.94}$Ge$_{0.06}$, but the value of 0.67 in Si$_{0.91}$Ge$_{0.09}$ shows a marked departure from this downward trend (see Figure 67). Although values of $r_{HH}$ are not available for all of the samples doped with 100 keV As, the available values are also consistent with this trend: in particular, the proposed value of the Hall scattering factor in Si$_{0.91}$Ge$_{0.09}$ (0.51) is higher than that in Si$_{0.96}$Ge$_{0.04}$ (0.49), although a value for Si$_{0.96}$Ge$_{0.06}$, the expected minimum according to the trend for 20 keV B, has not been obtained.
7.4.3 **Comparison with available models of strain relaxation**

Although the range of germanium doses used here was intended to generate strained SiGe layers for all implantation energies using the model of Cristiano et al [139], 15 at % Ge peak concentration is very close to the critical value for 30 keV Ge. This implantation already exceeds the critical concentration according to both theoretical prediction and experimental results of Paine’s work (see section 3.2). In relation to the latter model, even 13 at % Ge peak concentration is borderline and already relaxed in term of Paine’s experimental work (see Figure 15). Similarly for the deeper implants, it should be noted that 9 at % Ge peak concentration is above the critical value for 100 keV Ge from Paine’s experimental results, even if both Cristiano et al and Paine’s theoretical model suggest a critical concentration closer to 10 at % Ge for this implantation energy. This suggests that strain relaxation has occurred in the deeper implants with 9 at % Ge peak concentration. The discussion which follows in section 7.5 will therefore focus mainly on the electrical properties of those samples which we can be confident have a strained SiGe layer (0 to 10 at % Ge for the shallower implants, 0 to 6 at % Ge for the deeper implants).

7.5. **Dopant diffusion and carrier activation**

While strain relaxation can explain the degradation in electrical properties observed for the highest germanium concentrations in each set of samples, it cannot be used to explain the electrical characteristics over the whole range of germanium content investigated. In order to explain these characteristics it is important to consider also the patterns of dopant diffusion and carrier activation in these samples. Characteristics of the dopant profiles from SIMS are summarised in section 7.5.1, focusing especially on the extent of diffusion and dopant pile-up at the surface during the annealing. Possible mechanisms of diffusion and deactivation for boron and arsenic are considered in sections 7.5.2 to 7.5.3. Finally the electrical junction depths achieved are considered in section 7.5.4.

7.5.1 **Characteristics of dopant profiles**

SIMS profiles from selected samples were shown in sections 5.2.2.3 and 6.2.2.3. The boron peak concentration is \( \sim 1 \times 10^{20} \text{B}^+/\text{cm}^3 \) for both the chosen energies. The integral under the SIMS curves confirms that the target doses of \( 1 \times 10^{15} \) and \( 3.48 \times 10^{15} \text{cm}^{-2} \) for boron implanted at 20 and 7 keV, respectively have been achieved,
within experimental uncertainty of ± 5%. Also in the case of arsenic implanted at 30 keV, the dose measured by SIMS coincided, within experimental error of ± 1%, with the nominal dose of 2.5x10^{14} \text{ cm}^{-2}. In addition, comparing the integrations from as-implanted and annealed samples, no appreciable dose loss was found after annealing.

The as-implanted profiles for both deep and shallow implants with both boron and arsenic as dopant show less ion channelling in SiGe alloy, compared to bulk-Si. This is illustrated in Figure 72, which shows SIMS profiles of 20 keV B in bulk-Si substrate and in Si_{0.91}Ge_{0.09} as-implanted. The profiles have a similar peak value, but the silicon sample has a tail to the distribution. This is to be expected as the germanium dose needed for synthesis purposes (>3x10^{15} \text{ Ge}^+/\text{cm}^2, see section 4.1) was at least one order of magnitude larger than the critical dose for the formation of a continuous surface amorphous layer (typically > 5 \times 10^{14} \text{ Ge}^+/\text{cm}^2 [158]); thus all the SiGe layers would have been amorphous at the time of dopant implantation to a depth of ~200nm, and so ion channelling would not have occurred.

![Figure 72 SIMS profiles of 20 keV B in bulk-Si substrate and Si_{0.91}Ge_{0.09} as-implanted.](image)

After RTA, the dopant distributions in bulk-Si show evidence of diffusional broadening consistent with transient enhanced diffusion [159, 160, 161, 162]. However, comparison of the SIMS profiles for samples as-implanted and after
annealing shows that dopant diffusion is retarded in SiGe compared to bulk-Si for both dopants. For example, Figure 73 compares SIMS profiles for 30 keV arsenic implanted in bulk-Si and in Si\(_{0.85}\)Ge\(_{0.15}\), as-implanted and after RTA. While the sample in bulk-Si shows diffusional broadening, with reduction of the peak and extension of the tail of the arsenic distribution, these characteristics are reduced considerably in SiGe.

Several authors have reported that boron diffusivity decreases with increasing germanium content in strained Si\(_{1-x}\)Ge\(_{x}\) (x ≤ 0.50) [163, 164, 165], which is consistent with the results presented here. However, it has been reported elsewhere that, in epitaxial grown SiGe both strained and relaxed [162, 166, 167], arsenic diffuses more with increasing Ge content in the alloy layer. Possible mechanisms explaining this discrepancy between current and published results are discussed below.

![Figure 73 SIMS profiles for 30 keV As implanted in bulk-Si and in Si\(_{0.85}\)Ge\(_{0.15}\), as-implanted and after RTA.](image)

Figure 73 also shows a "pile-up" of arsenic towards the surface in the annealed samples. Figure 74 includes the full set of SIMS profiles of 30 keV As in Si\(_{1-x}\)Ge\(_{x}\) (0 ≤ x ≤ 0.15) as-implanted and after RTA. To better observe the profile peaks, Figure 74 show the linear-linear plot of the data. There is a clear presence of arsenic...
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Discussion

Piled up within the first 15 nm of the surface, which increases with germanium content, except for the case of alloy composition with 6 at % Ge where there was no presence of pile-up at the surface. This sample also showed the lowest value of sheet resistance, suggesting that the pile-up may be due to As clustered or trapped near the surface which would lead to a degradation in electrical properties.

Alternatively, these double peaks (some of which are indicated by an arrow in Figure 73) may be due to arsenic precipitates if the arsenic solid solubility was exceeded in Si as well as in SiGe. However, since arsenic solid solubility in silicon (~ $3 \times 10^{21}$ cm$^{-3}$ [162]) is more than one order of magnitude higher than the arsenic concentration in this work, this seems unlikely.

![Figure 74 Linear-linear SIMS profiles for 30 keV As implanted in bulk-Si and SiGe.](image)

However, High Resolution TEM studies carried out by Gaiduk et al in 1998 [168] reported the presence of small (0.55 nm) monoclinic GeAs precipitates in samples implanted with high dose arsenic ($\geq 10^{20}$ cm$^{-3}$) in relaxed Si$_{1-x}$Ge$_x$ alloy of composition varying within 0.15 $\leq x \leq$ 0.50, followed by RTA up to 900°C and 1100°C. The authors observed that these precipitates formed at an arsenic peak concentration about an order of magnitude lower than that observed in Si (AsSi) and that there was a clear dependence of the critical arsenic concentration on the
germanium concentration. Furthermore, Tishkov et al. [138] studied the evolution of defects in heavily doped arsenic-implanted $\text{Si}_{0.60}\text{Ge}_{0.40}$ alloy samples; they observed that the dislocations loops disappeared during annealing with the formation of $\text{AsGe}$ precipitates. This behaviour is different from that observed in $\text{Si}$, where the precipitates coexist with dislocations [169].

Another source of arsenic electrical deactivation which has been identified by several authors [170, 171, 172], is the formation of clusters of arsenic with vacancies ($\text{As}_4\text{V}$). The formation of these clusters was calculated by Pandey et al. [173] to be energetically favoured over both substitutional isolated $\text{As}$ and $\text{As}_4\text{I}$ configurations. Furthermore, Parisini et al [174] proposed a model for the arsenic deactivation process tested on samples thermally annealed in a low temperature range (350-550°C). The authors argued that the first step of the arsenic deactivation phenomenon is governed by the capture of two electrons by an initial cluster formed by the pairing of two $\text{As}$ atoms in second neighbour position in the $\text{Si}$ lattice. Experimental evidence for $\text{As-As}$ pairs were reported by Angelucci and co-authors [175]. Parisini’s model can be summarised as follows:

$$\text{(As}_2\text{)}^{2+} + 2e^- \rightarrow \text{(As}_2\text{V)}^+ + \text{I}^- $$

Eq. 7.4

The first step of deactivation consists in the formation of an ($\text{As}_2\text{V}$)$^+$ cluster and the ejection of a $\text{Si}$ self-interstitial, $\text{I}^-$, starting from the capture of two electrons from ($\text{As}_2\text{)}^{2+}$ pair. It was also proposed that this reaction starts in the region of the electric junction, where a charge separation phenomenon can favour the formation of the negatively charged $\text{Si}$ self-interstitial and of the positively charged As-vacancy cluster. However, at higher annealing temperatures and after achieving thermal equilibrium it was not clear whether precipitation or clustering was the dominant phenomenon.

Because clustering and precipitation are the main phenomena proposed by several authors [174, 175, 176] to explain the arsenic deactivation process, the following discussion focuses especially on these phenomena to address arsenic deactivation and diffusion in this work.

Figure 75 shows a combined plot of both atomic and free carrier profiles from selected samples implanted with 30 keV $\text{As}$ in bulk-$\text{Si}$ and $\text{Si}_{1-x}\text{Ge}_x$ ($0 \leq x \leq 0.15$) after annealing with RTA only. The SRP profiles show an overall similar box shape
where the tail of the arsenic distribution is inactive. The percentage of the activated dopant which in this case was calculated using SIMS profiles as reference, decreases with increasing germanium content from a proposed value of 60% in bulk-Si down to only 21% in the alloy composition with 13 at % Ge, consistent with the pattern of results reported by Tishkov [138].

![Figure 75](image_url)

Figure 75 Comparison between SIMS profiles and proposed free carrier concentration profiles from SRP for 30 keV As in Si and SiGe and annealed with RTA.

Figure 75 clearly shows that arsenic diffusion is less in SiGe than in bulk-Si; the annealed arsenic profile in SiGe remains close to the as-implanted arsenic profile in silicon.

In IBS SiGe, EOR defects (which are known to inject interstitials during annealing [159]) will be present after epitaxial re-growth. It has also been demonstrated by Cristiano et al. [109] that the total number of interstitials bound to the loops increases, at a given implantation energy, with increasing Ge content after RTA annealing at 1000°C for 100 sec. It has also been demonstrated [170, 171] that arsenic diffuses mainly via vacancies and tends to move away from interstitials; therefore EOR defects could act as a barrier for the arsenic diffusion [14]. In addition Uematsu [177] notes that the coarsening process of point defects, reduces arsenic diffusion for annealing times longer than about 1s, 10 s, 5 min, and 1 h at 1050,
1000, 900 and 850°C, respectively. Recently, Eguchi and colleagues [178] have proposed that the retarded diffusion of As in SiGe may be due to excess Si interstitials injected by the As ion implantation suppressing the vacancy concentration in SiGe.

Consistent with these findings are the results presented here from samples which have been post-amorphised (the EOR defects are located much deeper than the alloy layer at ~0.5 μm) where arsenic diffusion towards the surface was reduced.

![Figure 76 Proposed free carrier concentration as a function of Ge content for 100 keV As in SiGe with and without post-amorphisation (PA) after RTA at 1050°C for 10" (T3).](image)

Figure 76 shows a comparison of proposed free carrier concentration profiles in As implanted Si₁₋ₓGeₓ (0.1≤x≤0.9) after annealing with RTA only and the same samples after Si⁺ post-amorphisation and RTA. The arsenic distribution in samples which were not amorphised shows a broader distribution (calculated measuring the FWHM of the distribution, 98.8 nm), compared to the distribution for samples after PA which was 93.4 nm for Si₁₀.₀₉Ge₀.₀₉ sample. This shows that arsenic diffuses more towards the surface in samples without post-amorphisation, confirming that the EOR defects did act as a barrier for arsenic diffusion into the substrate. In addition, calculations of the total free carrier concentration, obtained by integration of the distribution curves, show a slight improvement in dopant activation after post-
amorphisation (e.g. 2.8% with 1 at % Ge). Again, PA, having located the EOR defects deeper into the substrate (~ 500 nm) and away from the implanted layer (~ 70 nm), would have reduced the density of the Si self-interstitials in the active region and therefore reduced the formation of electrically inactive \((\text{As}_2\text{V})^+\) clusters (as reported above in p 115 in region of the electric junction charged SiI can form more easily and therefore they can favour the formation of these clusters). In particular, the calculated value of total carrier concentration for arsenic in Si\(_{1-0.04}\text{Ge}_{0.04}\) was ~10% higher after post-amorphisation. To summarise, Si\(^+\) post-amorphisation did reduce arsenic diffusion, and appeared to give higher carrier activation.

Similar to the arsenic, also the boron distribution shows “pile-up” at the surface in samples with the higher germanium content for both energies (13 and 15 at % Ge at 7 keV and 9 at % Ge at 20 keV). Figure 77 shows a linear-linear plot of the SIMS data for the sample implanted with 7 keV boron in Si\(_{0.87}\text{Ge}_{0.13}\).

**Figure 77** Linear-linear SIMS profiles for 7 keV B implanted in Si and SiGe after RTA (T\(_3\) = 1050°, 10\(^\circ\)).

After RTA the boron profiles present a double peak (indicated by an arrow), close to the surface (~ 15 nm), which increases with germanium peak concentration for the samples investigated. In this case, the double peak of the boron distribution in SiGe
can be attributable to boron trapped and therefore deactivated at the surface in the relaxed and highly damaged $\text{Si}_{0.85}\text{Ge}_{0.15}$ and $\text{Si}_{0.85}\text{Ge}_{0.15}$ layers (see section 7.4). In addition, because TEM investigations on the samples containing 0 at % and 6 at % Ge peak concentration (see section 5.3) did not show a detectable presence of boron precipitates or clusters, we can also conclude that the boron solid solubility in those samples was not exceeded (solid solubility of boron in silicon being $6 \times 10^{19} \text{ cm}^{-3}$ at 900°C and $1.2 \times 10^{20}$ at 1000°C [151]). However, the formation of boron-interstitial clusters (BICs) can occur below the boron solid solubility deactivating the boron, but because of their very small dimension (several Å) they are not readily detected by TEM.

On the other hand, supporting the hypothesis of formation of electrical inactive BGe pairs discussed by Kuo et al. [163], are the SRP analyses, which show an apparent reduction in the activated carriers, proportional to the germanium content, which could explain the trend of the electrical results of sheet resistance increasing with increasing germanium peak concentration.

Figure 78 Comparison between SIMS profiles and proposed free carrier concentration profiles from SRP for 7 keV B in Si and SiGe and annealed with RTA.
Figure 7.8 shows a combined plot of both atomic and proposed free carrier profiles from samples implanted with 7 keV B in bulk Si and SiGe with 13 at % Ge and 15 at % Ge, after RTA. Profiles from the alloy layers show similar shape as the sample in silicon, with the dopant activation being independent of depth. However, only 61% of the boron appeared to be activated in bulk Si. On the other hand, in SiGe the dopant activation is significantly lower (23% and 22% for 13 at % Ge and 15 at % Ge, respectively). One can also observe that all of the boron in the tail is not active, with conduction mainly confined to the first 30 nm of the alloy layers.

To help to understand the phenomena involved in B diffusion in SiGe, some simulations of boron profiles in bulk-Si and in SiGe (6 at % Ge) are presented taking into account the kick-out mechanism, discussed by Cowern et al [179, 180, 181].

7.5.2 Kick-out mechanism

Supported by quantum-mechanical calculation of diffusion, in particular of B, P, As and Sb in silicon made by Nichols et al. [182], in 1990 Cowern et al [183, 184, 185] presented a theoretical model applicable to impurities in silicon that diffuse via "fast-diffusing intermediate species", either an impurity-interstitial (Xs-I) or an impurity-vacancy (Xs-V) pair. In both cases (Xs-I or Xs-V) diffusion is supposed to proceed by a series of migration events (of frequency "g") as the impurity randomly jumps between substitutional sites (immobile) and its less probable "fast-diffusing" state. During each migration event, the impurity travels randomly and terminates at some distance from the starting point, reverting to a substitutional site position [184]. In particular, for the interstitial-mediated component of diffusion, the energetically favoured route found by the authors was the kick-out reaction. In this process, a self-interstitial (I) reacts with a substitutional dopant atom (Xs), for example boron (Bs), which has been demonstrated by the same authors to diffuse via an interstitial mechanism [183] also see section 3.4), to form an interstitial impurity complex that migrates for some distance (λ) before recombining. The following equation shows the described mechanism:

\[ B_s + I \leftrightarrow B_I \text{ (kick-out reaction)} \]

When a proportion of boron atoms are displaced into a mobile state and therefore allowed to diffuse, the resulting boron profile would show an exponential-like tail.
[186]. The shape and the width of the profile provide information about both the kick-out rate \((g)\) and the migration distance \((\lambda)\) of the displaced atoms. The authors studied the temperature dependence of \(g\) and \(\lambda\) upon various levels of interstitial supersaturation \((S_I)\) during inert-ambient diffusion, oxidising-ambient diffusion and transient-enhanced diffusion. In all cases, \(g\) is proportional to \(S_I\), but the inverse reaction is independent of \(S_I\). At lower temperatures \(g\) decreases, being dependent on the formation and the migration energies of the self-interstitials. This energy depends upon the diffusion process involved. In particular, during TED, when interstitials “evaporate” from the implant damage, the energy required for the formation and migration of \(S_I\) is lower. In contrast, \(\lambda\) is characteristic of a thermal process and does not depend on a reaction with a point defect, and therefore is the same for all diffusion processes. In addition, Cowern et al. [186] found that \(\lambda\) becomes larger with decreasing temperature and therefore boron atoms migrate further at low temperatures, before returning into substitutional sites [186]. The basic mechanism can be summarised therefore as follows:

(a) dopant impurities in silicon diffuse by an intermittent process where they sit most of the time in an immobile substitutional site, but they can be converted into “fast-moving” species when interacting with a point defect.

(b) At high annealing temperatures, these interactions are more frequent and the diffusion appears to be a continuous process.

(c) At low annealing temperatures the individual migration events are rare (in time) and the diffusion distance is comparable with the device dimension in scale (nm)

(d) In all cases, the diffusion coefficient is given by \(D = \lambda^2 g\).

Figure 79 shows SIMS profiles from 7 keV B-doped bulk-Si, as-implanted and annealed (with \(T_3\)). The annealed profile was modelled using the kick-out model. The diffusivity of boron \((D_B)\) extracted from the fit of 7 keV boron was \(5.1 \times 10^{13} \text{ cm}^2/\text{s}\), which compared to the equilibrium diffusion \((D_B^* = 5.1 \times 10^{14} \text{ cm}^2/\text{s}\) from ref. [187]) was ~ 10% higher due to boron enhanced diffusion which occurs at the beginning of the annealing (see section 3.4). Similarly, when boron was implanted at 20 keV \(D_B\) was found to be \(8.3 \times 10^{13} \text{ cm}^2/\text{s}\), which is ~ 16% higher than the equilibrium value.
Section 3.3), followed by a "plateau" associated with the Ostwald ripening process of \{113\} defects (see section 3.3), whose lifetime increases with increasing implantation energy. The authors also suggested that this phenomenon demonstrates the crucial role of the vicinity of the boron profile to the surface to determine the TED decay time, especially for shallow implants (≤ 100nm). This can be explained by the change in dissolution rate of the implantation defects in
the presence of a trap for interstitials, such as the wafer surface, during annealing in an inert atmosphere (see section 3.3).

Figure 80 Simulation of the $S_n$ supersaturation evolution for $1\times10^{14}$ cm$^{-2}$ boron implants in the 1-25 keV range at an annealing temperature of 950°C [from ref. 189].

Figure 81 Scheme illustrating the model proposed by Cowern [191].

The kick-out modelling does not take into account that after Ge implantation followed by SPEG, EOR defects are localised below the depth of the original a/c interface and their density increases with germanium content (see section 3.2). Thus, in order to model boron diffusion in IBS SiGe is necessary to take into account the...
evolution of EOR defects during an anneal and how they affect the boron enhanced diffusion (see section 2.4 and [190]). Figure 81 summarises the model developed by Cowern et al [191] in order to explain the effect of EOR on boron TED.

Cowern et al. considered a damage band containing $10^{15}$ interstitials/cm$^2$, located at the position of the EOR defect band. The rate of emission of interstitials from this region into the wafer was set as a parameter to be adjusted to fit the amount of boron diffusion. This parameter only depends upon two conditions: (a) the Si-interstitial supersaturation at the depth of the EOR defects, $S_{\text{EOR}} = C_i/C_i^*$ and (b) the Si-interstitial supersaturation at the surface, $S_0 = C_i/C_i^*$, where $C_i^*$ is the concentration of Si-interstitials in the equilibrium conditions and $S_0$ a constant. According to this model, $S_{\text{EOR}}$ decreases from typically 1000 to 2 to 3 according to the Ostwald ripening theory (see section 3.4).

![Figure 82 Simulation of 20 keV B in SiGe (6 at % Ge peak concentration) and annealed with RTA at 1050°C for 10 seconds (T3) using the model presented by Cowern et al. [191]](image-url)
The SIMS boron profile in SiGe from this work was then simulated using MatLab according to Cowern's model\(^2\). The EOR box was positioned within 150 and 200 nm, where the location of the EOR defects had been detected with TEM observation (see section 5.3). The results are shown in Figure 82.

Also, in this case, a value of \(D_B = 9.36 \times 10^{-13} \text{ cm}^2/\text{s}\) in SiGe was calculated. From this model it is possible to link boron diffusion with germanium concentration as follows. In particular, the density of EOR defects would increase with germanium dose which mainly results in increasing the supersaturation of Si-interstitials below the a/c interface [192]. Because it has been demonstrated (see section 3.4.2) that the EOR defect region provides a time-decay source of Si-interstitials and that it is the coupling between this source and the boron atoms which is responsible for TED [183], one can postulate that with increasing germanium content, the amount of boron TED will increase.

However, this model does not account for either the kick-out mechanism or the formation of GeB complex which was suggested by Kuo et al [163] as the main constraint for boron diffusion. Kuo's model is briefly described in the following section.

### 7.5.3 Pairing (Kuo model)

Kuo et al. [163] have proposed a model to describe boron diffusivity in SiGe, which fitted with their experimental results. The model is based on the assumption that boron diffusivity in silicon is proportional to the concentration of mobile boron atoms, \(B_m\) (\(D_B \propto [B_m]\)), which diffuse via interstitial sites; the authors proposed that in SiGe B atoms can became immobile \(B_S\) through a pairing interaction with the germanium atoms (BGe):

\[
B_S + I \rightleftharpoons B_m
\]

Eq. 7.6

where \(B_S\) is a substitutional boron atom, \(I\) a silicon self-interstitial, and \(k_1\) is the reaction coefficient and

\(^2\) I am very grateful to Dr. Benjamin Colombeau for running the diffusion simulations presented in this chapter.
where $k_2$ is the reaction coefficient of Eq. 7.7.

The authors suggested that a possible driving force for this interaction is the local strain compensation between the larger germanium atoms and the smaller boron atoms. If one assumes that the interstitial interaction (Eq. 7.6) is independent of the pairing reaction (Eq. 7.7), Kuo et al. proposed that the net concentration of the $B_m$ in $Si_{1-x}Ge_x$ is reduced compared to that in silicon, as shown below:

$$[BGe] = \frac{[BSi]}{1 + K_2x} \quad \text{Eq. 7.8}$$

Since they assumed the diffusivity to be directly proportional to the concentration of the mobile boron atoms in silicon, as a result of the pairing interaction, then:

$$D^{SiGe}_B = \frac{D^{Si}_B}{1 + K_2x} \quad \text{Eq. 7.9}$$

and therefore the diffusion of boron in SiGe will be inversely proportional to the germanium content. To summarise, Kuo’s mechanism which describes the formation of immobile and electrically inactive BGe pairs, can be used to explain the reduced diffusion and the reduced activation of boron with increasing germanium content in this work.

### 7.5.4 Arsenic and Boron electrical junction depths achieved

The electrical junction depths of arsenic and boron were calculated using the spreading resistance data, assuming implanted material with a background doping of $1 \times 10^{17}$ cm$^{-3}$. As with all parameters derived from the SRP carrier concentration profiles (see section 7.3.1), these values are speculative and may not accurately reflect absolute values. Figure 83 shows the calculated electrical junction depths for samples implanted with 100 keV arsenic annealed at $T_1$ (open symbols) and $T_3$ (solid symbols), and 30 keV arsenic annealed at $T_3$. As a result of the reduced arsenic diffusion in SiGe, the electrical junction depths are reduced.
Figure 83 Speculative electrical junction depths at $1 \times 10^{17}$ cm$^{-3}$ for arsenic implanted in bulk-Si and SiGe after furnace annealing at 700°C for 20 min ($T_1$) and RTA at 1050°C for 10" ($T_3$).

Figure 84 Speculative electrical junction depths at $1 \times 10^{17}$ cm$^{-3}$ for boron implanted in bulk-Si and SiGe after RTA at 1050°C for 10" ($T_3$).
In the B-doped samples, the electrical junction depths are also reduced in SiGe. In particular, assuming the same background doping level, calculated junction depths for 20 keV boron vary from 280 nm in bulk-Si, to 180 nm in SiGe (4 at % Ge) and junction depths for 7 keV boron vary from 140 nm in bulk-Si, to 62 nm in SiGe (10 at % Ge). Figure 84 shows these results.

For the shallower As⁺ and B⁺ implants, the electrical junction depth was reduced by more than 50% in samples with $x > 10$ at%, compared to the values in bulk-Si. If reliable, the results for 30 keV As in particular show promise for PMOS device application, as the International Technology Roadmap for Semiconductors (ITRS 2001) proposes at the 60 nm node, contact junctions ($X_{jn}$) between 30 and 50 nm and contact extension between 16 and 20 nm.

### 7.6. Summary of the electrical characteristics achieved

Some noteworthy improvements in electrical characteristics were achieved in IBS SiGe compared to Si. Table 11 shows electrical properties of selected strained SiGe layers within each group of samples investigated here, compared to bulk-Si control samples. Samples with 4 at % Ge among the deeper implants, and samples with 6 to 10 at % Ge among the shallower implants, showed the best overall characteristics.

**Table 11** Electrical characteristics of strained SiGe layers after annealing with RTA ($T_3$), compared with data for bulk-Si control samples.

<table>
<thead>
<tr>
<th>Ge conc (%)</th>
<th>$X_d$ (nm)$^{ab}$</th>
<th>$R_x$ (Ω/sq)</th>
<th>$\mu_{Hall}$ (cm²/V-s)</th>
<th>$\mu_{Drift}$ (cm²/V-s)$^b$</th>
<th>$N_{Activated}$ (%)$^b$</th>
</tr>
</thead>
<tbody>
<tr>
<td>20 keV B</td>
<td>~ 280</td>
<td>121 ± 1</td>
<td>44.3 ± 0.4</td>
<td>51.7</td>
<td>99</td>
</tr>
<tr>
<td>4</td>
<td>~ 180</td>
<td>142 ± 1</td>
<td>39.4 ± 0.4</td>
<td>60.3</td>
<td>73</td>
</tr>
<tr>
<td>7 keV B</td>
<td>~ 140</td>
<td>459 ± 5</td>
<td>52.8 ± 0.5</td>
<td>91.3</td>
<td>67</td>
</tr>
<tr>
<td>10</td>
<td>~ 62</td>
<td>766 ± 8</td>
<td>42.3 ± 4</td>
<td>179.1</td>
<td>27</td>
</tr>
<tr>
<td>100 keV As</td>
<td>(~ 132)</td>
<td>(163 ± 2)</td>
<td>(137 ± 1)</td>
<td>(127.8)</td>
<td>(75)</td>
</tr>
<tr>
<td>4</td>
<td>~ 129</td>
<td>120 ± 1</td>
<td>74.1 ± 0.7</td>
<td>150.1</td>
<td>88</td>
</tr>
<tr>
<td>30 keV As</td>
<td>~ 69</td>
<td>364 ± 4</td>
<td>101 ± 1</td>
<td>211.3</td>
<td>58</td>
</tr>
<tr>
<td>6</td>
<td>~ 34</td>
<td>207 ± 2</td>
<td>105 ± 1</td>
<td>488</td>
<td>41</td>
</tr>
</tbody>
</table>

$^a$ Values of $X_d$ assuming an effective background doping level of $1 \times 10^{17}$ cm⁻³.

$^b$ Values of $X_d$, $R_x$ and $N_{Activated}$ are speculative, and hence confidence intervals are unknown (see section 7.3.1).

$^c$ Values for 100 keV As in bulk-Si are after furnace annealing only ($T_1$).
These are the first available data for an all-implanted route to the synthesis and doping of strained Si$_{1-x}$Ge$_x$ layers [13, 14]. Trends in drift mobility of B in bulk-Si and in SiGe were consistent with results reported elsewhere for comparable epitaxially grown material with B concentration up to $3 \times 10^{20}$ ions/cm$^3$ [157, 193]. In all cases, a reduction in proposed electrical junction depth and an increase in speculated values of drift mobility were achieved in SiGe, compared to Si.
Chapter 8

8. Conclusions and future work

In this project, ion implantation followed by thermal treatments was used as an alternative to epitaxial deposition for the synthesis and doping of Si$_{1-x}$Ge$_x$ alloy layers. The influence of germanium peak concentration ($0 \leq x \leq 0.15$) upon sheet resistance and Hall mobility was investigated for high doping concentrations of boron and arsenic ($1 \times 10^{20}$ ions/cm$^3$), using the van der Pauw method. The experiments were conducted using bulk-Si and SOI substrates. Selected material was also post-amorphised using silicon ions. SIMS and SRP were employed to determine the dopant distribution and to propose values of carrier activation, respectively. Finally, the crystalline quality of the material after annealing, as well as the location of extended defects, was investigated using XTEM analysis of selected samples. The main conclusions are summarised below.

8.1. Electrical characteristics achieved

Some noteworthy improvements in electrical characteristics were achieved in IBS SiGe, compared to Si. Electrical properties of those SiGe samples which showed the best overall characteristics (samples with 4 at% Ge among the deeper layers, synthesised by implantation of 100 keV Ge, and samples with 6 to 10 at% Ge among the shallower layers, synthesised by implantation of 30 keV Ge) were compared with the properties of Si control samples in Table 11 (section 7.6). These results are the first from strained SiGe layers, synthesised and doped by an all-implanted process, and show comparable electrical characteristics to epitaxially grown material [35, 149, 153, 154, 155].

In all cases, a reduction in electrical junction depth ($X_{el}$) was achieved in the IBS SiGe layers, compared to bulk-Si control samples. For the shallowest B$^+$ (7keV) and As$^+$ (30keV) implant layers, the $X_{el}$ is less than 50 % of the values in bulk-Si. The
proposed value of ~34 nm obtained for 30 keV As in SiGe (6 at% Ge) is particularly promising for application in PMOS devices as the International Technology Roadmap for Semiconductors (ITRS 2001) proposes contact junctions depths $X_{jn}$ between 30 and 50 nm and contact extensions between 16 and 20 nm for 60 nm devices. Also the $R_s$ of this sample, ~207 $\Omega$/sq, is within the ITRS target range of 150-535 $\Omega$/sq.

The availability of independent values of proposed free carrier density from the SRP and sheet resistance from the Hall measurements made it possible to speculate values of drift mobility, and hence to discuss the variation in the Hall scattering factor, $r_H$, as a function of germanium content in IBS SiGe. Estimates of $r_H$ for 20 keV B-doped samples were consistent with the values reported in the literature for MBE grown SiGe layers of similar thickness (see section 7.3.4).

With just one exception (see Table 11), the estimated percentage of activated carriers was reduced in SiGe. Nevertheless, proposed values of drift mobility were higher than the values in bulk silicon. Moreover, it should be noted that a high doping concentration was used in this work ($\sim 1 \times 10^{20}$ ions/cm$^3$); lower doping levels (less than $10^{18}$ ions/cm$^3$) may lead to better activation than was found here.

It is acknowledged that the values of carrier activation, junction depth and drift mobility reported here are all dependent upon the use of bulk Si mobility for extracting free carrier density from SRP measurements in SiGe. Hence, all of these values must be taken to indicate possible trends rather than to determine absolute values. In the absence of standard mobility curves for strained and unstrained SiGe or for ion implanted material, the extraction of free carrier density was consistent with current best practice (see section 4.3.2). However, the establishment of standard mobility curves for strained IBS SiGe alloys will be required to confirm the results presented here (see also section 8.4).

### 8.2. Strain relaxation

Evidence from both XTEM analysis and electrical measurements suggests that the highest germanium peak concentrations used here (13 and 15 at% Ge in the shallower layers, synthesised by Ge implantation at 30 keV; 9 at% Ge in the deeper layers, synthesised by Ge implantation at 100 keV) had exceeded the critical threshold for the production of strained SiGe layers after SPEG (see section 7.4).
This suggests that applications of IBS SiGe should be limited to lower germanium peak concentrations and/or shallower layers than those reported in this work. Based on the current results, Paine’s experimental model of strain relaxation (see sections 2.4.3 and 3.2) appears to provide the best prediction of the critical germanium content for lower implantation energies in IBS SiGe alloy layers.

It is also proposed that speculated values of $r_H$ at higher germanium concentrations, which departed from the general downward trend with increasing germanium, may provide a useful source of evidence for strain-relaxation (see section 7.4.2).

### 8.3. Dopant diffusion and activation

The presence of implanted germanium led to a reduction in the tail of both boron and arsenic distributions compared to bulk-Si, with proposed electrical junction depths reduced in some cases by over 50%. As discussed in section 7.5 and references within, it is hypothesised that this reduction in diffusion is mainly due to the formation of electrically inactive BGe pairs and/or BI clusters in the case of boron and the formation of GeAs precipitates and/or As$_4$V' clusters in the case of arsenic. The presence of these complexes could also be responsible for the reduction in estimated carrier activation with increasing germanium content. Silicon post-amorphisation improved the carrier activation in the case of As-doped samples. It is proposed that the presence of EOR defects acts as a barrier to arsenic enhanced diffusion, thus promoting a shift of the arsenic distribution towards the surface. In particular, it is noted that the trend for As-doped samples differs from previous findings using deposited strained SiGe layers, where greater diffusion of arsenic has been observed with increasing germanium content (see section 7.5.1).

Mechanisms of diffusion of both dopants, but especially arsenic, are still poorly understood and much further research is needed to clarify how diffusion occurs in both deposited and IBS substrates.

### 8.4. Discussion of future work

One of the main issues for CMOS device fabrication is to constrain the dopants within the source and drain regions, during thermal treatments, in order to avoid short-channel effects. Although boron diffusion behaviour in Si and in SiGe is better understood, a lot more research is needed in order to understand the diffusion of arsenic, in both Si and SiGe. In particular, the opposite behaviour of arsenic diffusion...
in IBS SiGe compared to deposited alloy material needs attention. Especially useful would be a closer comparison of IBS SiGe with epitaxy SiGe material of similar thickness and similar germanium content, doped with the same implanted dose of arsenic and regrown under the same annealing conditions. This would help to address questions about diffusion mechanisms, dopant clustering and activation and the exact role of the germanium\(^3\). Furthermore, to comprehensively investigate diffusion, it will be necessary to consider a wider range of annealing schedules, especially longer times and lower temperatures, to ensure a defect-free regrowth of the material together with equilibrium diffusion. SRP, CV and SIMS measurements will give information on carrier activation and diffusion. Ideally, the data should be compared with simulated profiles (although no software is currently available which can reliably predict diffusion coefficients in SiGe alloys). Furthermore, XTEM studies should be carried out in order to establish how the a/c interface regrowth velocity varies through the SiGe layers during SPEG. Also, the formation and dissolution of extended defects (in particular EOR) and their role in limiting the dopant diffusion in ion beam synthesised SiGe warrants investigation.

Alternative techniques to TEM, such as Deep Level Transient Spectroscopy (DLTS), can be used to study the crystalline quality of SiGe material and in particular the presence of point defects, coupling and clustering. X-ray diffraction (XRD) can be used to investigate SiGe strain-relaxation [61], and in particular Double-crystal x-ray diffraction (DCD) can be used to measure the lattice mismatch, both parallel and perpendicular to the SiGe/Si interface [194].

Electrical profiles can be achieved, especially for layers thicker than ~ 50 nm, with Hall stripping measurements that, together with temperature dependent measurement, can provide a better picture of carrier activation, scattering mechanisms and mobility. Furthermore CV profiling should be used to determine

\(^3\) Very recently, Mitchell and colleagues [M.J. Mitchell, P. Ashburn, J. M. Bonar, P.L.F. Hemment, in press] have reported a comparison of arsenic diffusion in SiGe formed by epitaxy and IBS. Their study uses a different sample structure to that used here, with the arsenic distribution fully contained within the germanium distribution after annealing, rather than matching the depth of Ge and As peak concentrations. Furthermore the As peak concentration was more than one order of magnitude higher than in this work. Unlike the results presented here, arsenic diffusion was greater in IBS SiGe than in epitaxy SiGe or bulk-Si.
carrier profiles independently of drift mobilities, which will be crucial to test the accuracy of deriving carrier density from SRP measurements in IBS SiGe.

It is now accepted that SiGe has found a place in silicon-based technology, and more than 30 companies, including IBM, Philips and Hitachi, are now developing SiGe Integrated Circuits using chemical vapour deposition [5]. The present work suggests that an all-implanted route to the production of strained SiGe layers is worth considering. In particular, the use of IBS SiGe substrates in place of bulk-Si has been shown to result in improvements in the control of dopant diffusion and the value of carrier drift mobility. Nevertheless there remains the need to improve the crystalline quality of thin layers after the impact of high dose implantation in order to improve on the levels of dopant activation observed here.
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