Design, Development and Fabrication of a New Generation Semiconductor X-ray Detector

Shada Kazemi

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Ion Beam Centre, School of Electronics and Physical Sciences,
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I want to thank all my colleagues from both the academic and the industrial milieu for the scientific and interesting discussions we have had.

Finally, I would like to thank my family for their patience and support.
Abstract

X-ray detectors are used in a number of areas, namely in astronomy, microscopy, medical imaging diagnostic, biological science and material analysis [1-10].

Demand is rising significantly within the industry for X-ray detectors that do not require a cooling system, e.g. pin-diode detectors.

The elimination of the cooling system will facilitate the design of portable detectors. Development of this technology opens opportunities for the design of new instruments and the manufacture of more specialist detectors for customised applications.

The rapid progress of the semiconductor industry has enabled the construction of more sophisticated electronic devices. This progress has also resulted in the creation of simulation tools, which enable researchers to simulate the processing of their devices. This method is more time and cost efficient as different models can be tested before actually investing in device processing in a laboratory.

For this project we have used Silvaco simulation tools and packages to design nine different pin-diode X-ray detectors and evaluated their electrical performance before manufacturing them.

Microfabrication technology has also been employed to make the pin-diode X-ray detectors that are capable of simultaneously detecting low X-ray energies (<10 keV) and measure the radiation energies with high sensitivity, speed and resolution. The X-ray detectors have been manufactured using the University of Surrey’s cleanroom and laboratories.

This project is run as a Knowledge Transfer Partnership scheme in partnership with e2V Scientific Instruments (e2Vsi).

To improve efficiency and productivity in industry, recent years have seen increased collaboration between industry and academia. New technologies have been commercialised with varying degrees of success and new applications have emerged, also benefiting academic research.
e2Vsi is a manufacturing company specialising in the design, development and production of high resolution semiconductor X-ray detectors and the project objectives are therefore closely aligned with industry's needs.
## Abbreviations

<table>
<thead>
<tr>
<th>Short form</th>
<th>Full description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AlSi1%</td>
<td>1% of aluminium in silicon</td>
</tr>
<tr>
<td>B⁺</td>
<td>Boron</td>
</tr>
<tr>
<td>CBKR</td>
<td>Cross-Bridge Kelvin Resistor</td>
</tr>
<tr>
<td>CCD</td>
<td>Charge Coupled Device</td>
</tr>
<tr>
<td>CVD</td>
<td>Chemical Vapor Deposition</td>
</tr>
<tr>
<td>DI</td>
<td>Deionised water</td>
</tr>
<tr>
<td>E2Vsi</td>
<td>E2V Scientific Instruments</td>
</tr>
<tr>
<td>EDX</td>
<td>Energy Dispersive X-ray Spectroscopy</td>
</tr>
<tr>
<td>FET</td>
<td>Field Effect Transistor</td>
</tr>
<tr>
<td>Ge(Li)</td>
<td>Lithium Drifted Germanium</td>
</tr>
<tr>
<td>HF</td>
<td>Hydrofluoric acid</td>
</tr>
<tr>
<td>KTP</td>
<td>Knowledge Transfer Partnership</td>
</tr>
<tr>
<td>LN</td>
<td>Liquid Nitrogen</td>
</tr>
<tr>
<td>PC</td>
<td>Photoconductance</td>
</tr>
<tr>
<td>pin-diode</td>
<td>p-type, intrinsic, n-type diode</td>
</tr>
<tr>
<td>P⁺</td>
<td>Phosphorous</td>
</tr>
<tr>
<td>QSS</td>
<td>Quasi-steady-state</td>
</tr>
<tr>
<td>RCA</td>
<td>Radio Corporation of America</td>
</tr>
<tr>
<td>RTA</td>
<td>Rapid Thermal Annealing</td>
</tr>
<tr>
<td>SC</td>
<td>Standard Clean</td>
</tr>
<tr>
<td>SDD</td>
<td>Silicon Drift Detector</td>
</tr>
<tr>
<td>SEM</td>
<td>Scanning Electron Microscope</td>
</tr>
<tr>
<td>Si</td>
<td>Silicon</td>
</tr>
<tr>
<td>Si(Li)</td>
<td>Lithium Drifted Silicon</td>
</tr>
<tr>
<td>SIMS</td>
<td>Secondary-Ion Mass Spectrometry</td>
</tr>
<tr>
<td>STJ</td>
<td>Superconducting Tunnel Junction</td>
</tr>
<tr>
<td>TED</td>
<td>Transient Enhanced Diffusion</td>
</tr>
<tr>
<td>UV</td>
<td>Ultra Violet</td>
</tr>
<tr>
<td>VWF</td>
<td>Virtual Wafer Fabrication</td>
</tr>
<tr>
<td>W</td>
<td>Tungsten</td>
</tr>
<tr>
<td>XRF</td>
<td>X-ray Fluorescence</td>
</tr>
<tr>
<td>Z</td>
<td>Atomic Number</td>
</tr>
</tbody>
</table>
# Table of Contents

ACKNOWLEDGMENTS ................................................................................................................. 1  
ABSTRACT ..................................................................................................................................................... 2  
1 INTRODUCTION ........................................................................................................................................ 8  
2 X-RAY DETECTOR TECHNOLOGY ........................................................................................................... 14  
  2.1 DETECTOR MATERIALS ......................................................................................................................... 14  
  2.2 DIFFERENT RADIATION DETECTORS .............................................................................................. 19  
    2.2.1 Gas-filled Detectors ................................................................................................................... 19  
    2.2.2 Superconducting Tunnel Junction Detectors ........................................................................... 20  
    2.2.3 Semiconductor Detectors ......................................................................................................... 21  
      2.2.3.1 Si(Li) Detectors .................................................................................................................... 21  
      2.2.3.2 Silicon Drift Detector .......................................................................................................... 23  
      2.2.3.3 Charge Coupled Devices ........................................................................................................ 25  
      2.2.3.4 Pin-diode Detectors ........................................................................................................... 27  
3 REVIEW OF SILVACO SOFTWARE SUITE ........................................................................................... 30  
  3.1 VIRTUAL WAFER FABRICATION TOOLS ......................................................................................... 31  
    3.1.1 DeckBuild Run-time Environment .......................................................................................... 32  
    3.1.2 DevEdit Structure and Mesh Editor ....................................................................................... 32  
    3.1.3 MaskView Layout Editor .......................................................................................................... 32  
    3.1.4 Optimizer .................................................................................................................................... 33  
  3.2 ATHENA PROCESS SIMULATION FRAMEWORK ......................................................................... 34  
  3.3 ATLAS DEVICE SIMULATION FRAMEWORK ................................................................................ 35  
  3.4 EXPERT LAYOUT EDITOR FRAMEWORK ..................................................................................... 36  
  3.5 SETTING UP THE SIMULATOR ....................................................................................................... 37  
4 X-RAY DETECTOR DESIGN .................................................................................................................. 39  
  4.1 DEVICE SIZE ..................................................................................................................................... 39  
  4.2 CHOICE OF MATERIAL ....................................................................................................................... 40  
  4.3 CHOICE OF PARAMETERS .................................................................................................................. 40  
    4.3.1 Ion Implantation in Athena ......................................................................................................... 41  
      4.3.1.1 Gaussian Implant Model ....................................................................................................... 42  
      4.3.1.2 Pearson Implant Model ......................................................................................................... 43  
      4.3.1.3 Dual Pearson Model ............................................................................................................. 43  
      4.3.1.4 Monte Carlo Model ............................................................................................................. 44  
    4.3.2 Choice of Ion Dose and Energy ................................................................................................. 46
6.2.3 Wafer 3 – B⁺ Used for Implantation ................................................................. 110
6.2.4 Wafer 4 – B⁺ Used for Implantation through a 10nm Oxide .............................. 111
6.2.5 Analysis of the Results .................................................................................... 113

6.3 SECOND PROCESSING RUN ANALYSIS ...................................................................... 115

   6.3.1 Batch 1 – Section of Wafer 1 Implanted with 2 keV B⁺ 3x10¹³ cm⁻² Annealed for 5s at 950 °C ................................................................. 116
   6.3.2 Batch 2 - Section of Wafer 1 Implanted with an Additional 10 keV B⁺ 2x10¹⁴ cm⁻² Annealed for 5s at 950 °C .................................................. 117
   6.3.3 Batch 3 – Section of Wafer 2 Implanted with 2 keV B⁺ 3x10¹³ cm⁻² Annealed for 10s at 850 °C ................................................................. 118
   6.3.4 Batch 4 – Section of Wafer 2 Implanted with an Additional 10 keV B⁺ 2x10¹⁴ cm⁻² Annealed for 10s at 850 °C ........................................ 119

6.3.5 Batches 1-4 - 1mm² Pin-diode Detectors with 2 Guard-rings ......................... 121
6.3.6 Batches 1-4 - 1mm² Pin-diode Detectors with 3 Guard-rings .......................... 123

6.4 DEVICE COMPARISON .......................................................................................... 127

   6.4.1 Devices with a Different Number of Guard-rings ........................................ 128
   6.4.2 Devices with a Different Number of Floating Guard-rings .......................... 131
   6.4.3 Comparing Devices with Floating Guard-rings and Devices with Metal Contacts on the Guard-rings ............................................................ 132
   6.4.4 Comparing Devices with an Oxide Layer or Metal Contact on the Active-area ... 135
   6.4.5 Analysing the Effect of Deep and Shallow Implantation under the Active-area’s Contact ................................................................. 138
   6.4.6 Analysing the Effect of the n⁺ Layer .............................................................. 140
   6.4.7 Analysing the Area’s Impact on the Leakage Current .................................. 142

6.5 ANALYSIS OF THE RESULTS ................................................................................. 143

7 CONCLUSION ........................................................................................................... 156

8 FUTURE WORK ......................................................................................................... 163

REFERENCES ............................................................................................................. 165
1 Introduction

In 1895 German physics professor Wilhelm Conrad Röntgen, while experimenting with a cathode-ray tube, noticed a green light against a bench one meter away from the tube. Surprisingly, the light was travelling through some materials (paper, wood, and books) in its way. He called this X-rays because of the algebraic symbol of the unknown variable in order to indicate that it was an unknown type of radiation.

Since then scientists have become interested in measuring the energy of X-rays and also identifying the direction of the radiation by manufacturing various types of X-ray detectors.

To understand radiation detection we need to investigate and determine the radiation’s properties and characteristics.

An X-ray is an electromagnetic radiation with a wavelength between 10nm and 100pm, corresponding to frequencies in the range $3 \times 10^4$ THz - $3 \times 10^6$ THz. In the electromagnetic spectrum, X-rays are located before the Ultra Violet (UV) in wavelength and have higher energies than UV. See Figure 1.

![Figure 1: The electromagnetic spectrum [11].](image)

The basic production of X-rays is by accelerating electrons in order to collide with a metal target. The electrons must have enough energy to be able to knock out an electron from the inner shell (K-shell). The incoming X-ray ejects an electron from the inner shell (K-shell) and creates a vacancy. For the atom to go back to the stable
condition, an electron from the L, M, or N-shell jumps in, to fill the vacancy. If the electron jumps from the L-shell to the K-shell, the emitted X-ray is called Ka, if it is from the M-shell, it is called Kβ and if it is from N-shell it is called Ky. The X-ray’s energy emitted from the atom is the energy difference between the corresponding shells. That is why the emitted X-ray has different levels of energy.

When a vacancy is created in the L-shell by either the primary excitation X-ray or by the previous event (an electron jumping from the L- to the K-shell), an electron from the higher shells (M or N) jumps in to occupy the vacancy in the L-shell. If an electron from the M shell jumps, the X-ray that is emitted from the atom is called Lα and if it is from N shell is called Lβ.

Figure 2 shows a simplified diagram of this phenomenon. The K series are rays, which are emitted by electrons from the upper shells jumping to the K shell and the same for the L and M series.

![Figure 2: Atomic level diagram [12].](image)

Figure 3 shows K, L and M shell’s X-ray energies as a function of atomic number Z. Elements with atomic number up to 10 generate only K series energies. Elements from Z=10 up to Z=47 generate both K and L series energies. Elements with atomic numbers 48 and above generate also M series energies.
Table 1 shows X-ray K-series spectral-line wavelengths for some common target materials [14].

<table>
<thead>
<tr>
<th>Target</th>
<th>$\lambda_{K\alpha_1}$ (nm)</th>
<th>$\lambda_{K\alpha_2}$ (nm)</th>
<th>$\lambda_{K\beta_1}$ (nm)</th>
<th>$\lambda_{K\beta_2}$ (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$^{26}$Fe</td>
<td>0.193604</td>
<td>0.193998</td>
<td>0.17566</td>
<td>0.17442</td>
</tr>
<tr>
<td>$^{28}$Ni</td>
<td>0.165791</td>
<td>0.166175</td>
<td>0.15001</td>
<td>0.14886</td>
</tr>
<tr>
<td>$^{29}$Cu</td>
<td>0.154056</td>
<td>0.154439</td>
<td>0.139222</td>
<td>0.138109</td>
</tr>
<tr>
<td>$^{40}$Zr</td>
<td>0.078593</td>
<td>0.079015</td>
<td>0.070173</td>
<td>0.068993</td>
</tr>
<tr>
<td>$^{42}$Mo</td>
<td>0.070930</td>
<td>0.071359</td>
<td>0.063229</td>
<td>0.062099</td>
</tr>
</tbody>
</table>

Table 1: X-ray K-series spectral-line wavelengths for some common target materials.

Table 2 shows the K series energies for some common target materials [15].

<table>
<thead>
<tr>
<th>Target</th>
<th>$\lambda_{K\alpha_1}$ (keV)</th>
<th>$\lambda_{K\alpha_2}$ (keV)</th>
<th>$\lambda_{K\beta_1}$ (keV)</th>
<th>$\lambda_{K\beta_2}$ (keV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$^{26}$Fe</td>
<td>6.403</td>
<td>6.390</td>
<td>7.057</td>
<td>-</td>
</tr>
<tr>
<td>$^{28}$Ni</td>
<td>7.477</td>
<td>7.460</td>
<td>8.264</td>
<td>8.328</td>
</tr>
<tr>
<td>$^{29}$Cu</td>
<td>8.047</td>
<td>8.027</td>
<td>8.904</td>
<td>8.976</td>
</tr>
<tr>
<td>$^{40}$Zr</td>
<td>15.774</td>
<td>15.690</td>
<td>17.666</td>
<td>17.969</td>
</tr>
<tr>
<td>$^{42}$Mo</td>
<td>17.478</td>
<td>17.373</td>
<td>19.607</td>
<td>19.964</td>
</tr>
</tbody>
</table>

Table 2: X-ray K-series energies for some common target materials.
Radioactive sources also emit X-rays. Sources which emit only X-rays are very rare. Usually they also emit γ-rays.

The most widespread X-ray sources are Fe-55, Co-57, Cd-109, Am-241 and I-129. These sources emit X-rays of definite energy and are therefore capable of exciting a specific number of atoms.

Table 3 shows a list of X-ray sources with corresponding radiation type and energies. Also their half-life time and the nuclides resulting from the radioactive decay of the parent isotope (daughter products) are noted.

<table>
<thead>
<tr>
<th>Isotope</th>
<th>Atomic Number</th>
<th>Half-life (years)</th>
<th>Radiation</th>
<th>Energy (keV)</th>
<th>Intensity (%)</th>
<th>Progeny</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fe-55</td>
<td>26</td>
<td>2.7</td>
<td>X-ray</td>
<td>5.9 (27.8%)</td>
<td>4.95 (60.7%)</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Auger electron</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Co-57</td>
<td>27</td>
<td>0.7</td>
<td>X-ray</td>
<td>6.48 (57.9)</td>
<td>14.4 (9.54%)</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>γ</td>
<td>122 (85.6%)</td>
<td>136 (10.6%)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>692 (0.02%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cd-109</td>
<td>48</td>
<td>1.3</td>
<td>X-rays</td>
<td>22.1 (83.6%)</td>
<td>25.0 (17.7%)</td>
<td>Ag 109</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>γ</td>
<td>88.0 (3.6%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Am-241</td>
<td>95</td>
<td>432.2</td>
<td>X-ray</td>
<td>16.6 (37.7%)</td>
<td>59.5 (35.9%)</td>
<td>Np-237</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>γ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>α</td>
<td>5.44 (12.8%)</td>
<td>5.48 (85.2%)</td>
<td></td>
</tr>
<tr>
<td>I-129</td>
<td>53</td>
<td>15.7X10⁶</td>
<td>X-ray</td>
<td>4.3 (7%)</td>
<td>29.67 (58.2%)</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>γ</td>
<td>33.7 (12.6%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>β</td>
<td>39.58 (7.51%)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>41.2 (100%)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 3: The most common X-ray sources [16].
In 1908 Hans Geiger developed a device which later was named after him (Geiger counter) and could detect alpha particles. Later, in 1928, he improved the device with his PhD student Walter Müller so that it would be capable of detecting X-rays by indicating the presence of the radiation with a needle or lamp and/or audible clicks while being capable of measuring high X-ray energies. This was the beginning of a new era which led to the invention of gas, semiconductors and superconducting detectors. These different detectors resulted from the needs of different applications and also the level of the X-ray energies to be measured. Numerous types of materials have also been investigated for the manufacture of X-ray detectors and the research is still ongoing. This will be described in detail later in this thesis.

This project addresses a multitude of topics ranging from the investigation of current theory to device design and fabrication. Our approach has combined modern techniques for analysis, such as modelling the X-ray detectors using the Silvaco TCAD software to predict the optimal pin-diode detector’s configuration and practical device processing to produce the X-ray detectors.

Silvaco TCAD software has enabled us to determine the optimal device configuration in terms of choice of material, device dimensions, number of guard-rings, the distance between the guard-rings and their widths, parameters for processing methods such as implantation energy and dose, annealing time and temperature. The electrical performance of the pin-diode detector has also been determined from these simulations.

This thesis describes the design, development and manufacture of a new-generation semiconductor X-ray detector that combines the latest advances in detector theory.

The objective is to design and manufacture a 5×5 mm² X-ray detector capable of measuring low X-ray energies (<10 keV). There is also a requirement to reduce the leakage current to about 0.5 nA/cm² and obtain an efficiency of up to 100% without using a liquid nitrogen dewar to cool down the system. The elimination of the dewar will facilitate the manufacture of portable detectors.

The theory behind the device configurations and reasons behind the choice of material (Silicon) and the detector type (pin-diode) to meet the requirements are discussed in this thesis.
The thesis has the following structure:

Chapter 1 introduces the thesis.

Chapter 2 introduces the reader to different X-ray detectors, the latest detector technology and also describes the reason behind our choice of the material and the type of the X-ray detector.

Chapter 3 provides an overview of the capabilities of the Silvaco software package, which has been used to design the X-ray detectors.

Chapter 4 describes the X-ray detector’s design and includes all the simulation results. It also describes how the pin-diode’s configuration changes when placing guard-rings in the device.

Chapter 5 describes the processing technology applied to the wafers in order to manufacture the pin-diode X-ray detectors. This includes quality control and performance evaluation.

Chapter 6 presents all the electrical measurements and analysis of the manufactured pin-diode X-ray detectors.

Chapter 7 provides the project conclusions, derived by analysing the detectors’ design and actual electrical characteristics.

Chapter 8 suggests future work for this project.

References provide a list of scientific papers, books, etc. utilised and evaluated as part of this project.
2 X-Ray Detector Technology

X-ray detectors are used to measure the energy and sometimes also the direction of an emitted X-ray depending on the measurements method of the signal which is generated from the detector. Since this project is to produce an X-ray detector for the purpose of energy measurement, the thesis focuses on these types of detectors.

There are three types of X-ray detectors: gas-filled, superconducting tunnel junction and semiconductor detectors. The last two types utilise modern detector concepts while gas-filled detectors are based on relatively old technology. The advantages and disadvantages of using each type of X-ray detector are described in this chapter. X-ray detectors are described in greater detail in [17-19].

This chapter begins with description of different materials used in detector technology and also shows the reason of our choice of silicon (Si).

2.1 Detector Materials

Depending on the different requirements from the industry, different materials have been used in producing detectors.

Si is the most used material for this technique. It has a high charge carrier mobility for both, holes and electrons, leading to an excellent charge collection efficiency. silicon’s large band gap (1.12 eV) assures that the thermally generated leakage current at any given temperature will be small. Si can be produced with very low impurity concentration. It is also cheaply available in large quantities and its processing is well developed in the electronic industry.

Ge is another semiconductor material for this purpose. Since Ge can have a thickness of a few centimetres is the most suitable material for γ-ray detectors. Ge detectors have a higher energy resolution compared to Si detectors due to germanium’s narrow energy band gap (0.66 eV). However Ge detectors need to be cooled to reduce their thermally generated leakage current.
GaAs has been used to detect high X-ray energies due to its large energy band gap (1.42 eV). Since GaAs has a large atomic number, it provides a good absorption efficiency. However the effective absorption thickness of the detector is reduced due to the dead layer which is built on the surface (see chapter 2.2.3.1) for the explanation of the dead layer). The charge carriers generated in the dead layer zone are not collected by the electrodes and are lost for signal detection. In addition, these detectors require a cooling system.

Other materials with a high atomic number which are used for detectors are CdTe, CdZnTe, HgI₂ and PbI₂. Because of their high atomic number these materials have a large photon absorption and a good energy resolution. However the low hole mobility in these materials and the tendency to hole trapping causes insufficient charge collection. Moreover it is still difficult to produce these materials in large area monocrystals. These materials are mainly used to detect γ-rays [20-23].

Diamond, which has a low atomic number (Z= 6) and is classified as an insulator, is also used as a detector material. At present they are much more expensive and more difficult to manufacture.

To choose the detector material, not only the radiation absorption is important but also factors such as the electron-hole generation, technology feasibility, economy, material availability and the effect of the radiation on the detector should be considered.

Very important aspects of the detector material are the penetration depth of charged particles and the absorption length of the photons. A very small absorption length will result in a high probability of generating the signal close to the surface. In this area the signal charge may be partially collected because of surface damage due to ion implantation. A very large absorption coefficient leads to inefficiencies as radiation may traverse the detector without interaction [17].

Figure 4 shows the absorption length of different high Z-materials in comparison to Si. Si has higher absorption length than the other materials. The high absorption length results in most of the X-ray energy being absorbed.
Figure 4: Absorption lengths for various high Z materials in comparison to Si [24].

Since Si has higher absorption length and is also suitable for detecting low energy X-rays (as shown in Figure 4), this material has been chosen for this project. Further investigation is needed, however to confirm whether the manufacture of portable detectors is feasible using Si. This leads to an investigation of the material's properties.

Material with low carrier density is needed to minimise the current noise in the X-ray detector. Materials with this quality have a high resistivity and a long carrier life-time.

The long carrier life-time makes the device able to collect the charges efficiently. This implies also material where the lattice defects and impurity concentrations have been reduced to a very low level. This is obtained to a certain level by processing the X-ray detectors in a very clean environment.

Figure 5 shows the minority carrier life-time (hole) in n-type Si. Experimental data follows the predicted life-time, although there is some scatter in the experimental data. The life-time depends very much on the device’s cleanliness during the
processing. The scatter in the data is a reflection of this dependence [25].

Figure 5: Experimental and theoretical hole life-time values in n-type Si as a function of electron concentration [25].

Material with higher carrier density has low carrier mobility due to the collection among the carriers. See Figure 6.

Figure 6: Electron mobility in n-type Si at 300 K as a function of total donor density. Curve 1-4 are based on theoretical calculation [25].
The carrier mobility is temperature dependent. Factors such as increased thermal agitation of the Si atoms, replacement of Si atoms in the lattice by impurities and the existence of crystal defects all cause disturbances that can scatter the carriers in the lattice. This reduces the mobility.

Figure 7 shows the electron mobility in n-type Si as function of temperature for various dopant densities [25].

![Figure 7: Electron mobility in n-type Si as function of temperature for various dopant densities](image)

The higher the carrier life-time, the lower the leakage current and the more efficient the detector becomes. To ensure that Si is not full of defects and impurities, and also to obtain a lower leakage current, Si with high carrier life-time about 1 ms and a resistivity of 5 kΩ-cm has been chosen for this project. See also the simulation carried out in Silvaco in chapter 4, which shows that the X-ray detector manufactured with this material yields lower leakage current than the X-ray detectors manufactured with lower carrier life-time material.

Also silicon’s properties such as high absorption coefficient and high carrier mobility make it suitable for this project. The high absorption length results in most of the X-
ray energy being absorbed. The high charge carrier mobility for both holes and electrons in Si leads to sufficient charge collection efficiency in the X-ray detector. silicon's large band gap (1.12 eV) insures that the thermally generated leakage current at any given temperature will be smaller than the other semiconductor materials. This also makes Si suitable for X-ray detector production without using a cooling system.

2.2 Different Radiation Detectors

In this chapter different radiation detectors are described. This thesis puts greater emphasis on semiconductor detectors' functionality since this project is to manufacture a semiconductor detector (pin-diode).

2.2.1 Gas-filled Detectors

Helium, Neon and Argon are the most common gases used in gas-filled detectors. Figure 8 shows an illustration of a gas filled detector. When a particle or photon hits the gas-filled tube, ions are created in the tube. The gas ions move to the electrodes of the opposite polarity, thus creating a current pulse.

The resulting current is proportional to the amount of charge, which is in turn proportional to the amount of charge generated by the initial photon interaction.

![Figure 8: A simplified circuit of a gas-filled detector [26].](image)
In gases, a large amount of energy is required for the ionisation. This means that gas-filled detectors are best used to detect only higher X-ray energies and γ-rays.

Gas-filled detectors can only detect the presence and the intensity of the radiation. They are used in nuclear physics, geophysics (mining), medicine and in industry.

### 2.2.2 Superconducting Tunnel Junction Detectors

A superconducting tunnel junction (STJ) detector consists of two superconducting regions separated by a thin insulating barrier. When a particle or photon hits one of the superconducting electrodes, the energy will break the superconducting Cooper pairs (a pair of electrons with a small attraction between them) into quasi-particles.

When a bias voltage is applied to the barrier these quasi-particles will tunnel through the barrier and create a measurable current, which is proportional to the absorbed particle or photon energy. See Figure 9.

![Figure 9: X-ray detection mechanism in an STJ crystal](image)

Since the number of created quasi-particles in a superconductor is much larger than the respective number of electron-hole pairs excited in a semiconductor by the same photon, the energy resolution is correspondingly much higher in STJ detectors [28, 29].
STJ systems are used as detectors for optical, ultraviolet, X-ray, γ-ray photons and massive particles.

STJ systems operate at a temperature of 0.1 K and for this reason they are connected to a cooling system with liquid He. This means that they are not portable [30]. They are relatively expensive and are usually only used by research institutions.

2.2.3 Semiconductor Detectors

Semiconductor detectors have been developed since the 1970s, initially using Si doped with Lithium Si(Li) or Germanium doped with Lithium Ge(Li).

In recent years, progress in semiconductors technology has resulted in a number of new types of detectors. The most used semiconductor detectors are Si(Li)-based, Si drift detectors (SDD), charge coupled devices (CCD) and pin-diode detectors.

2.2.3.1 Si(Li) Detectors

To produce the Si(Li) crystal the method is to diffuse Li into a p-type Si substrate. Since the n-type surface layer is heavily doped compared to the p-type original crystal, the depletion region extends primarily into the p-side of the junction. Therefore much of the surface layer remains outside of the depletion region and represents a dead layer or window [31]. This dead layer can be a real disadvantage because the incident radiation loses a portion of its energy through this layer before it reaches the depleted region, see Figure 10.

When the X-ray photon hits the detector it may escape or be absorbed within the crystal. The absorbed X-ray ejects electron-hole pairs, X-rays or Auger electrons depending on in which shell the X-ray energy is absorbed.

To ensure complete collection of the charge carriers (created by the X-ray) in the depleted region, a reverse bias voltage about -500V must be applied to the crystal. The electrons within the depletion region will transfer to the positive charged
electrode (anode) and the holes will transfer towards the negative charged electrode (cathode).

Figure 10 a) shows the charge transfer towards the electrodes and b) shows the dead layer and the process in the Si atom when it is hit by an X-ray photon.

![Figure 10 a) Cross-section of a Si(Li) crystal and b) Detection mechanism in a Si atom](image)

The electric charges created in the crystal will be amplified by a field effect transistor (FET), which is located within the detector, behind the crystal. The FET also converts the electric charges to a voltage step. This signal is too small to be measured and processed. Therefore another FET preamplifier has to be used to amplify the signal before it goes through an analogue or a digital signal processor for further analysis.

In order to reduce the leakage current and get a low noise level compared to the signal, the crystal has to be cooled down to a temperature close to liquid nitrogen (LN) at 77K or -196 °C. This is obtained by putting the crystal and the FET in a cryostat and keeping them cold via a copper rod (cold finger) connected to a dewar containing LN. Hence detectors based on Ge(Li) and Si(Li) are not portable.

Figure 11 a) shows the LN dewar on a SEM detector and b) shows the crystal, FET and the cold finger within the cryostat.
Figure 11 a) A schematic of a SEM detector with a LN dewar and cryostat. b) Schematic of a cold finger, FET and crystal [15].

Figure 12 shows a typical spectrum of a FE-55 X-ray source detected by a 10 mm$^2$ Si(Li) detector manufactured by e2Vsi. The resolution is 128eV and the peak to background ratio is 22000:1.

Figure 12: A typical spectrum of a FE-55 X-ray source detected by a 10 mm$^2$ Si(Li) detector [15].

2.2.3.2 Silicon Drift Detector

The first working silicon Drift Detector (SDD) was built at the Max Planck Institute in Munich in 1985. The idea was to shorten and move the n+ region in a diode to the opposite side and place diodes on both sides. See Figure 13 a).
SDDs are used in applications like electron microscopy (SEM-EDX) and X-ray fluorescence analysis (XRF) [33].

Figure 13a) shows the schematic and functionality of a linear SDD with strips on both front and the back sides. In the linear SDD each electrode on the front and the back is reverse biased until the detector gets fully depleted. The anode is segmented.

When a particle or photon hits the surface of the SDD it creates an electron-hole pair. The p-type strips on the front are used to shape the electrical field and create the potential gradient needed to drive the electron cloud generated by the photon to the collecting anode. The resulting current is proportional to the absorbed particle or photon energy. The signal will be amplified and analysed later by the read-out electronics.

Figure 13b) shows a schematic of a cylindrical SDD. In the cylindrical design the FET is integrated in the anode, which in this case minimises the detector’s capacitance and reduces the generated noise. The back of the SDD is a planar surface without structures and is the entrance window for the incident radiation. The n-type substrate is fully depleted by applying a negative voltage to the back contact and the drift-rings with respect to the anode in the centre of the SDD. The generated electrons by the incident radiation are then guided towards the anode by the drift-rings. This signal is proportional to the energy of the incident radiation.

Figure 13: a) A cross-section of a linear SDD [34]. b) A schematic of a cylindrical SDD with an integrated central FET readout [35].
SDDs are used for detecting low energy X-rays without using any cooling systems, providing a better resolution than the Si(Li), Ge(Li) and pin-diode detectors but they are relatively more expensive.

2.2.3.3 Charge Coupled Devices

Charge Coupled Devices (CCD) were first invented at Bell Laboratories in the late 1960s. They have been used for storing and transferring charges (most commonly in digital video cameras, astronomical telescopes, scanners, bar-code readers and robots), in the processing of satellite photographs and in the enhancement of radar images.

More importantly, they have revolutionised digital radiography, medical and dentistry equipment by requiring fewer X-rays than conventional radiography and by providing an image within seconds. Due to these larger sensitivity detectors, they can provide an equivalent clinical image with about 70% less exposure to radiation than by using conventional film. With less radiation exposure, the dose absorbed by the patient is significantly lower [36].

The semiconductor substrate of a CCD may be n or p-type. Figure 14 illustrates the working function of an n-type CCD. The p⁺ back contact acts as an entrance window for the radiation. By grounding the substrate and applying negative voltages to all the electrodes on the surface, the device gets depleted and sensitive to the ionisation radiation. Applying a significantly more negative voltage to one of the electrodes on the surface will cause the depletion region beneath this electrode to extend more deeply. This deeper depletion region is called a “potential well”. The electrons generated by the radiation trap in this potential well. These packets of electrons can be transferred to the next electrode by putting more negative potential to that electrode and allowing the potential on the previous electrode to go back. By repeating this process along the electrodes, eventually the charge packets shift to the readout electrode (anode) [37].
Figure 14: A cross-section of an n-type CCD [38].

Figure 15 illustrates the structure of a p-type CCD. The principle for the p-type CCD is the same as the n-type CCD and here also the electrons are collected (minority carriers) to be analysed later.

CCDs, similarly to SDDs, are portable detectors and are relatively expensive compared to Si(Li), Ge(Li) and pin-diode detectors.
2.2.3.4 Pin-diode Detectors

Pin-diode detectors are the cheapest detectors capable of measuring low energy X-rays without the need for a cooling system.

There are four different methods to produce these detectors:

- Implantation of $p^+$ ions in an n-type substrate
- Implantation of $p^+$ ions in a p-type substrate
- Implantation of $n^+$ ions in an n-type substrate
- Implantation of $n^+$ ions in a p-type substrate

To produce a detector with $p^+$ in p and $n^+$ in n junctions, both the front and the back side of the device need to be processed. Processing one side of the wafer is more favourable due to the simplicity and consequently the low cost of the processing. Only one side of $p^+$ in n and $n^+$ in p detectors need to be processed. For this reason we should focus on these types of detectors.

$n^+$ in p junctions usually have lower breakdown voltage compared to $p^+$ in n. Also these diodes exhibit higher leakage current usually two orders of magnitude higher than detectors fabricated with n-type substrate [40-42].

In contrary, $p^+$ in n junctions exhibit high breakdown voltage. Values exceeding 1000V have been reached by using guard-rings in the device (see chapter 4.8). $p^+$ in n detector can operate partially depleted. Sometimes when the back of the detector is damaged it is better to prevent the device from full depletion. As the depletion region reaches the damaged area the leakage current increases. No other detector type has this quality to function without being fully-depleted.

For the reasons mentioned above $p^+$ in n detectors have been chosen to be designed and manufactured for this project.

Table 4 shows the four combinations of detector types with their advantages and disadvantages [24].
Table 4: Possible combinations of substrate and electrodes type.

<table>
<thead>
<tr>
<th>Readout electrode</th>
<th>p-type substrate</th>
<th>n-type substrate</th>
</tr>
</thead>
<tbody>
<tr>
<td>$n^+$</td>
<td>Single sided process, lower breakdown voltage, Not yet seriously developed. May be relatively cheaper.</td>
<td>Double sided process, Relatively expensive, Can’t operate partially depleted.</td>
</tr>
</tbody>
</table>

In a pin-diode the intrinsic region covers a large region in the device. This increases the photo sensitive region and consequently enhances the conversion efficiency. This quality also makes the pin-diode detector suitable to be used as radiation detectors. The large intrinsic region forms a low capacitance in the device, which contributes to a high resolution in the pin-diode detector.

Pin-diode detectors were originally developed for use in satellite instrumentations. They were commercialised 1993 and today they are used for bench top and handheld systems, also for micro X-ray fluorescence and coating thickness measurements because they don’t need to have a cooling system with dewars. Pin-diode detectors are used for medical purposes, especially in radiology. They are also used in digital signal processing and as data storage devices.

The majority of pin-diode detectors are used in the areas of X-ray fluorescence (XRF) and Energy Dispersive X-ray (EDX) spectroscopy [43, 44].

Figure 16 illustrates the pin-diode detector’s functionality.

When a reverse bias voltage is applied to the pin-diode, the depletion region expands from the $p^+$ anode towards the $n^+$ cathode. The device can be fully-depleted by increasing the bias voltage.
When a particle or photon hits the entrance window (anode) and penetrate through to the depletion region, it generates electron-hole pairs. The holes travel towards the opposite polarity electrode (anode) and the electrons move towards the cathode. The signal generated from the electrons will be amplified and analysed later by the read-out electronics. This signal is proportional to the energy of the incident radiation.

Figure 16: pin-diode detector's functionality.
3 Review of Silvaco Software Suite

Simulation tools can be utilised to design devices with optimal electrical configuration potentially avoiding several iterations of expensive and time-consuming device manufacture to attain the desired configuration. The perfect simulation tool would be a package that provides ready-made detectors where the user could change certain parameters to achieve the desirable electrical performance. Unfortunately such a simulation package does not currently exist. However, the Silvaco package provides tools to design semiconductor devices. It is also capable to optimise all device parameters in order to achieve the optimal electrical configuration. It simulates the electrical characteristic of the X-ray detector and can be used to design the layouts for the masks, which are used for the processing of the X-ray detectors. For these reason, the Silvaco software was used to design the X-ray detector required for this project.

As with any other simulation package the Silvaco software has disadvantages which were discovered while designing the detectors. The first disadvantage is that the package does not take into account changes in the carrier life-time of the device throughout the processing. This is the consequence of the factors which affect the carrier life-time such as the contamination level in the laboratory, variety of equipment used, that are unique to each laboratory. Also the package is not able to show any difference between the electrical performance of the pin-diode detectors with or without floating guard-rings (unless the guard-rings were biased), which led us to manufacture a variety of pin-diode detectors to determine the real performance. The other disadvantage is that the simulation is mesh based. If the mesh is not well constructed the simulation runs incorrectly or exhibits convergence issues.

The Silvaco package, in common with other simulation programs does not show the X-ray response of the X-ray detectors. This is a complex behaviour to exhibit. It does, however, show the I-V characteristic of the X-ray detector and if we aim for the lowest leakage current this means that the detector has also the highest X-ray resolution.
The use of the simulation package replaces costly wafer experiments to deliver shorter development cycles and higher yields. The packages and the tools, which have been used for this project (Virtual Wafer Fab, Athena, Atlas and Expert), are described below [45-48].

3.1 Virtual Wafer Fabrication tools

The Virtual Wafer Fabrication (VWF) package provides an integrated software environment to automate and emulate physical wafer manufacturing. The tool facilitates the input, execution, run-time optimisation, and results processing of simulations in a single flow managed through a common database. For device processing, it enabled us to specify and achieve optimal process recipes.

Figure 17 shows the modules and architecture of VWF, including the interfaces between the tools in terms of inputs and outputs. VWF tools, Athena and Atlas were used for this project as shown in the figure. Each tool is described in this chapter.
3.1.1 DeckBuild Run-time Environment

Deckbuild is an interactive graphical environment that allowed us to progress from process to device simulation by transferring output from Athena into Atlas. Deckbuild was also used for invoking and connecting other VWF tools as shown in Figure 17.

Deckbuild provides a graphical interface for programmers to write simulation code and invoke the other Silvaco tools to process the code. Moreover Deckbuild offers multiple windows to show the run-time of the simulation, errors in the program and simulation results in text format.

3.1.2 DevEdit Structure and Mesh Editor

We have used DevEdit to edit, convert, merge, optimise, and save structures and meshes between the process and device simulation stages. The mesh, geometry, electrode positions and the doping of the structure were also specified in DevEdit.

A feature of DevEdit, DevEdit3D, was used for converting structures from 2D to 3D by extending region and the mesh into the third plane.

3.1.3 MaskView Layout Editor

MaskView is an editor for device layouts that can eventually be passed to Athena for process simulation. MaskView provides functionality for drawing and editing the layout, storing and loading complete layouts, and importing/exporting layout information using the industry-standard GDS2 and CIF layout formats.

GDS2 files were used for this project. Note that MaskView does not currently provide a function to create new GDS2 files, so the Silvaco component Expert (see chapter 3.4) was used to create the initial GDS2-format layout files that were subsequently edited via MaskView.
MaskView is also used to provide information, via GDS2 files, on how Athena should construct its grid, specifies region and electrodes names for use with Deckbuild when passing the simulated region on for device simulation.

Layout experimentation such as misalignment, polygon oversizing/undersizing, and global rescaling are functions available in MaskView that we used on this project.

### 3.1.4 Optimizer

The Optimizer is used to tune the parameters in Deckbuild to allow the achievement of user defined targets. Targets were specified as measured parameters, such as extracted thin junction depth, the lowest leakage current and the highest breakdown voltage. The parameters in the X-ray detectors that required optimisation included process variables (implantation dose and energy, etc.) and device structure attributes such as the number of guard-rings, their widths and the distance between them.

The optimizer calculates response values versus a set of input parameters in order to determine which input parameter results in a response value closest to a user-defined target. The optimizer works iteratively through a sequence of input parameters defined in terms of numerical start and last values, and the increment size between iterations. When all iterations are complete, the optimal input value and calculated response value are returned by the optimizer.

### 3.1.5 TonyPlot 1D/2D/3D Interactive Visualization Utility

Tonyplot is a graphical analysis tool used to display the output of Silvaco simulations. This facilitated the analysis of process and device design. Tonyplot is a key tool in the Silvaco suite and was used frequently to verify the relative merits of design decisions. TonyPlot supports 1D x-y data, 2D plotting of contour data and import of measured data. There is also 3D TonyPlot, which produces 3D plots for Atlas and DevEdit3D. We have used 1D, 2D and 3D TonyPlot for this project. It also enabled us to carry out graphical rotation around any axis (x, y, z), immediately repositioning the device.
structure. The Cut-plane feature allowed us to create 2D cuts to be defined around any axis within the structure and exported to a file to be analysed later in Atlas.

3.2 Athena Process Simulation Framework

Athena enables development and optimisation of the X-ray detector manufacturing process by providing simulation of the ion implantation, ion diffusion during the annealing, photolithography, oxidation, deposition of the Al contacts and etching of the oxide and the Al contacts.

Athena also provides the simulation of all critical fabrication steps used in CMOS, bipolar, SiGe/SiGeC, SiC, SOI, III-V, optoelectronic, and power device technologies.

Athena processing determined the physical structures of the devices. These structures were used as input into Atlas, which then calculated the electrical characteristics associated with pre-defined bias conditions. The combination of Athena and Atlas made it possible to determine the impact of process parameters on device characteristics.

Figure 18 shows Athena’s inputs and outputs, within the context of this project.
3.3 Atlas Device Simulation Framework

Atlas is the main device simulation tool used in this project and is responsible for calculating the electrical characteristics and the thermal behaviour of the X-ray detectors.

Atlas is a physical properties-based device simulator and has been used in conjunction with Athena and the VWF tools Deckbuild, TonyPlot, DevEdit, MaskViews, and Optimizer.

Atlas produces three types of output.

1) Run-time output – displays the progress of running simulations, including error and warning messages.

2) Log files - stored all terminal voltages and currents resulting from device analysis.
3) Solution files - stored data relating to the values of solution variables within the device for a single bias point.

The output from Athena was used as input into Atlas so as to be able to simulate the electrical characteristics of the device.

Figure 19 shows the input and outputs for Atlas, within the context of this project.

![Atlas inputs and outputs diagram]

**3.4 Expert Layout Editor Framework**

Expert is a high performance hierarchical layout editor with editing features and layout viewing. This Silvaco tool was used for the creation of the layouts for the masks required for this project. The layouts for different X-ray detectors were created on 8 different masks. The masks were then used in the photolithography step of the wafer processing (see chapter 4.9).

The output files were saved as GDSII files, which is an industrial standard format.
3.5 Setting up the Simulator

To design a device via the Atlas or Athena command language, first the mesh has to be defined. The mesh or grid covers the physical simulation domain.

It is defined by a series of horizontal and vertical lines and the spacing between them. Regions within this mesh are allocated to different materials as required to construct the device. For example, the specification of the X-ray detector requires the specification of Si and SiO$_2$ regions. After the regions are defined, the locations of the electrodes are specified. The final step is to specify the doping in each region. The mesh grids have to be tighter in the regions with higher rate of changing in carrier density. Figure 20 shows the mesh structure for the X-ray detector. The mesh is tighter for the high doping concentration on the surface and the back of the device, also for the guard-rings around the anode. Guard-rings are needed to reduce the leakage current and increase the breakdown voltage in the device. This will be described later in chapter 4.

When a reverse bias is applied to the pin-diode, the depletion region not only extends into the diode but also on to the surface. Since the density of the crystal defects and the impurities are larger at the edge of the device, the leakage current increases suddenly when the depletion approaches this region. For this reason, phosphorous (P$^+$) is implanted at the edge of the device to prevent the depletion region from developing further. This region has been named the n$^+$ layer. See Figure 20.
Figure 20: The mesh structure for the device.
4 X-ray Detector Design

This chapter describes the design of an X-ray detector that meets the following specification:

- Size of the device must satisfy commercial requirements
- Device must be capable of measuring low X-ray energies (<10 keV)
- Leakage current must be as low as 0.5 nA/cm²
- The breakdown voltage must be as high as possible
- There must be no need for a liquid nitrogen dewar to cool down the system.

To design the X-ray detectors, the Silvaco package and tools described in chapter 3 above have been used. All the graphs and figures shown in chapter 4 were generated using TonyPlot (see chapter 3.1.5).

In this chapter all the parameters that control the leakage current, the breakdown voltage and consequently the effect on X-ray performance, have been investigated. The choice of the material has also been investigated using the Silvaco suite.

4.1 Device Size

The market-established active-area size for pin-diode X-ray detectors is 10mm². Therefore, in order to compete in the market, the device to be modelled should also have a 10mm² active-area. Also, a very large active-area would give too much capacitance in the measurement circuit as well as the potential for more leakage current, so small areas are preferred and a 10mm² device is a good compromise. As for the overall size of the device, 5x5mm² is sufficient to accommodate the structures.
4.2 Choice of Material

In chapter 2.1 the reasons behind the choice of Si for this project were given. Si with high carrier life-time of about 1 ms and a resistivity of 5 $\text{k}\Omega$-cm has been chosen for this project. Figure 21 shows the Atlas simulation result for the I-V characteristic for various carrier life-times. The higher the carrier life-time, the lower the leakage current becomes.

![ATLAS I-V characteristic for different carrier lifetime](image)

Figure 21: The I-V characteristic for various carrier life-time.

4.3 Choice of Parameters

During ion implantation, a beam of ions enter crystalline or amorphous material. The dopant atoms slow down and scatter due to nuclear collisions and electronic interaction. Along the path, an individual ion may create fast recoil atoms that can initiate collision cascades of moving target atoms. The ion implantation results in local compositional changes, damage creation and finally amorphization of the target.
Depending on the crystal orientation, the direction of the beam, the ions energy and dose, the implanted ions have a different distribution.

There are several programs which are used to characterise the implantation profile. The Stopping and Range of Ions in Matter (SRIM) is a program which calculates the stopping and range of ions into matter using a quantum mechanical treatment of ion-atom collisions. The calculation is made very efficient by the use of statistical algorithms. A full description of the calculation is found in [49].

Srim does not support two-dimensional profiles or implantation through more than one layer. Athena, on the other hand, has the advantage of providing two-dimensional ion implantation profiles and implantation through multiple layers.

SUSPRE is another program based on energy deposition in the surface and is written and developed by Prof. Roger Webb at University of Surrey. At the time of the ion implantation stage of this project, SUSPRE did not support implantation through multiple layers; for this reason, Athena was used to design and model the detectors for this project.

### 4.3.1 Ion Implantation in Athena

Figure 22 shows the implantation geometry used in Athena in order to simulate the implantation profile. It shows the orientation of the ion beam, relative to the crystallographic orientation of the substrate. There are three major planes regarding ion implantation in materials, mainly:

- the implantation plane $\alpha$
- the surface plane $\Sigma$
- and the simulation plane $\beta$

The implantation plane is where the initial beam of incoming ions hits. It equivocally defines the direction of the incoming beam, tilt and rotation. If the orientation of the surface plane is $<100>$, the offset of the rotation angle is the direction $<101>$ on this
plane. This means that the tilt angle $\theta$ will be the polar angle in laying this plane, while the rotation angle $\phi$, is the azimuth of the line where the implantation plane crosses the surface plane and the direction $<101>$. The simulation (projection) plane is where all data regarding the simulation is projected on, which is what finally goes into Athena’s structure. See Figure 22.

![Diagram of implantation geometry](image)

Figure 22: The implantation geometry in Athena [46].

### 4.3.1.1 Gaussian Implant Model

There are several ways to construct 1D ion implantation profiles. The simplest way is to use the Gaussian distribution, which is specified by Athena as following:

$$C(x) = \frac{\phi}{\sqrt{2\pi\Delta R_\rho}} \exp\left(-\frac{(x-R_\rho)^2}{2\Delta R_\rho^2}\right)$$

where $\phi$ is the ion dose/cm$^2$ and $R_\rho$ is the projected range [46].
4.3.1.2 Pearson Implant Model

Generally, the Gaussian distribution is inadequate because real ion implantation profiles are asymmetrical in most cases. The simplest and most widely approved method for calculation of asymmetrical ion implantation profiles is the Pearson distribution, particularly the Pearson IV function [46]. Athena uses this function to obtain longitudinal implantation profiles. To find out about the differential equation and the resulting distribution curves, refer to [46]. The complete classification of various Pearson curves is found in [50].

In the standard Pearson model, the longitudinal dopant concentration is proportional to the ion dose [46]:

\[ C(x) = \phi f(x) \]

where \( \phi \) is the ion dose/cm\(^2\), \( f(x) \) is the function for Pearson IV distribution [46]. This single Pearson approach (method) has been proved to give an adequate solution for many ion, substrate, energy, dose combinations but there are many cases when the channeling effects make the single Pearson method inadequate. The dual Pearson model, described below, solves this problem.

4.3.1.3 Dual Pearson Model

To extend applicability of the analytical approach toward profiles heavily affected by channeling, [51] suggests the dual (or double) Pearson Method. An improved modeling approach is described for simulating as-implanted boron impurity profiles for B\(^+\) and BF\(_2^+\) implants into single-crystal silicon. This method uses the sum of two Pearson distribution functions to account for the non-channeling and channeling components of the implant distribution. The ratio of the two Pearson functions varies with dose, which accounts for the change in the degree of channeling with dose. This modeling approach has been compared with experimentally measured SIMS profiles for a wide range of energies and doses for shallow B\(^+\) and BF\(_2^+\) implants. The excellent agreement indicates that this method offers a large improvement in
simulation capability for $B^+$ and $BF_2^+$ implants. In addition, this method is applicable to accurately model other impurities which have channel intendancies. With this method, the implant concentration is calculated as a linear combination of two Pearson functions [46]:

$$C(x) = \phi_1 f_1(x) + \phi_2 f_2(x)$$

The first Pearson function represents the random scattering part (around the peak of the profile) and the second function represents the channeling tail region.

### 4.3.1.4 Monte Carlo Model

The analytical models described in the previous section give very good results when applied to ion implantation into simple planar structures (bare silicon or silicon covered with thin layer of other materials). But for structures containing many layers (material regions) and for the cases which have not been studied yet experimentally, more sophisticated simulation models are required. The most flexible and universal approach to simulate ion implantation in non standard conditions is the Monte Carlo technique.

In order to calculate the distribution of the ions, the Monte Carlo model simulates atomic collisions in the targets using the Binary Collision Approximation (BCA). The algorithm follows out the sequence of energetic ions launched from an external beam into a target. The targets may have many material regions, each with its own crystal structure (crystalline or amorphous). The slowing-down of the ions is followed until they either leave the target or their energy falls below some predefined cut-off energy.

The Monte Carlo method is rapidly gaining acceptance as a means for the simulation of ion implantation due to its capability of simulating channeling and damage accumulation phenomena in multi-dimensional structures. A well-known disadvantage of the Monte Carlo approach is its considerable demand for computer resources to obtain results with satisfying statistical accuracy.

The traditional Monte Carlo approach for crystalline targets is based on the calculation of a large number of ion trajectories, i.e., each trajectory is usually
followed from the ion starting point at the surface of the target up to the stopping point of the ion. Since the majority of ion trajectories ends at the most probable penetration depth inside the structure, the statistical representation of this target region is good.

The trajectory split method ensures a much better statistical representation in regions with a dopant concentration several orders of magnitudes smaller than the maximum. As a result, the time required to perform a simulation with comparable statistical accuracy is drastically reduced and is applicable for two- and three-dimensional simulations [52] [53].

Figure 23 shows the boron ($B^+$) profile using different models in Athena. The energy used for the implantation is 2 keV with a dose of $3 \times 10^{13}$ cm$^{-2}$, tilt=$7^\circ$ and rotation=$22^\circ$ for all the three models. The Monte-Carlo and the Dual-Pearson models have almost the same profile.

![Boron profile using different models in Athena](image)

Figure 23: Boron profile using different models in Athena. The implantation energy is 2 keV and the dose is $3 \times 10^{13}$ cm$^{-2}$ for all the three models.
4.3.2 Choice of Ion Dose and Energy

To reduce the leakage current for the device and also reduce the dead layer of the X-ray window, the junction of the active-area (anode region) should be shallow [54, 55]. To achieve this, the implantation energy should be as low as possible and the dose should be low.

Figure 24 shows the leakage current throughout the device for different implantation energies for the boron ($B^+$) in the active-area.

As the implantation energy increases, the leakage current also increases. By choosing 2 keV for the $B^+$ implantation energy rather than the two other higher energies, the leakage current has reduced by one order of magnitude and the breakdown voltage increased to 300 V. The dose for $B^+$ used in this simulation is $3 \times 10^{13}$ cm$^{-2}$, tilt=7° and rotation=22°. Si resistivity= 5 kΩ-cm, annealed at 950 °C for 5 s.

![Figure 24: I-V characteristic for different implantation energies for B+ in the active-area. B+ dose is 3X10^13 cm^2, Si resistivity= 5 kΩ-cm, annealed at 950 °C for 5 s.](image-url)
Figure 25 shows the $B^+$ concentration in the active-area for different ion doses and the implantation energy of 2 keV. The higher the dose, the more the ions penetrate through the wafer and the thicker the junction becomes. If the junction depth is thicker, the dead layer also gets thicker, which will reduce the X-ray detectors efficiency.

For this reason, we chose to apply a dose of $3 \times 10^{13}$ cm$^{-2}$ for the active-area. Too low dose would reduce the $B^+$ concentration on the surface and the leakage current would consequently increase.

![Boron profile for the active-area for different doses](image)

Figure 25: $B^+$ concentration vs. depth for different $B^+$ doses. Si resistivity= 5 k$\Omega$-cm, $B^+$ implantation energy=2 keV.

Figure 26 shows how the junction depth and the peak concentration changes by using different energies for the $B^+$ implantation in the active-area with the same dose of $3 \times 10^{13}$ cm$^{-2}$, tilt=7° and rotation=22°.
For this project, the active-area was implanted with 2 keV $B^+$, $3 \times 10^{13}$ cm$^{-2}$, tilt=7° and rotation=22°. The selection of 2 keV, $3 \times 10^{13}$ cm$^{-2}$ ion implantation results in an ion distribution with the average depth of 0.085 micron and a peak concentration of $2 \times 10^{19}$ cm$^{-3}$.

![Boron profile for the active-area for different energies](image)

**Figure 26:** $B^+$ concentration vs. depth for different $B^+$ implantation energies. $B^+$ dose is $3 \times 10^{13}$ cm$^{-2}$, Si resistivity= 5 kΩ-cm.

There are methods to reduce the junction depth. For example, amorphisation, oxidation of the surface before the $B^+$ implantation or BF$_2^+$ implantation. In the pre-amorphisation, the ion channeling which results in an extended tail is suppressed and secondly the incorporation of the dopants within the lattice is much higher in the amorphised layer than in the crystalline Si, resulting in a shallow junction [56]. Many groups have published contradicting reports regarding whether or not Transient Enhanced Diffusion (TED) still occurs if pre-amorphysation is used. Some groups reported enhances [57] but other suggested that TED was completely retarded [56].
is well known that the implantation conditions, dose, energy, pre-amorphisation, annealing conditions affect the EOR and hence the level of enhanced diffusion.

In this project, amorphisation of the surface has not been considered due to the crystal damage it introduces. Moreover, the surface constitutes the X-ray window and it should be free of defects and damage to provide good radiation absorption, hence amorphisation would not have been appropriate.

In this project $BF_2^+$ was used to implant the active-area on some of the detectors in order to compare the electrical performance of these detectors with the performance of the detectors implanted with $B^+$.

Figure 27 shows the boron profile for $BF_2^+$ and $B^+$ implantations used for this project. The Dual-Pearson model in Athena is used for characterisation of the profile. The $B^+$ dose is $3 \times 10^{13} \text{ cm}^{-2}$ and the $BF_2^+$ dose is $5 \times 10^{12} \text{ cm}^{-2}$ but both with an energy of 2 keV, tilt=7° and rotation=22°. The reason behind the choice of the energy and the dose for the $BF_2^+$ was to achieve a shallower junction while maintaining the same peak concentration as for the $B^+$ implantation.
Boron Dose=3e13/cm² Energy=2 keV
BF₂ Dose=5e12/cm² Energy=2 keV

Figure 27: Boron profile for B⁺ and BF₂⁺ implantations for the active-area of the detectors using Dual-Pearson model. Si resistivity= 5 kΩ-cm.

Athena provides the implantation profiles through multiple layers. In this project, two layers were utilised: oxide on Si.

To apply any of the described analytical distribution functions for structures that are comprised from several different material layers, a scaling method must be used in Athena. This is because the ions' stopping powers and range parameters are different in different materials.

In all the implantation models described above, the range parameters in each layer are considered independent of the presence of other layers. This, however, does not correctly model ion implantation behaviour: the distribution of ions stopped in the deeper layers depends on the thickness and the stopping characteristics of the upper layers. The scaling methods used in Athena take this layer position dependency effect into account.
Another important issue is to correctly identify the mesh in the upper layer, which in our case is the oxide layer.

To reduce the junction depth in the active-area for this project, $B^+$ and $BF_2^+$ were implanted through 10 nm of an oxide layer.

The simulation in Figure 28 shows $B^+$ implantation through 10 nm thick oxide layer. The $B^+$ dose is $3 \times 10^{13}$ cm$^{-2}$ with an energy of 2 keV and the $BF_2^+$ dose is $5 \times 10^{13}$ cm$^{-2}$ with an energy of 2 keV, both with a tilt=7° and rotation=22°.

In comparison to Figure 27 the oxide layer reduces the range from about 82 nm to 72 nm for the $B^+$ implanted wafer and from 35 nm to 9.5 nm for the $BF_2^+$ implanted wafer. The oxide layer also reduces the $B^+$ concentration in the interface between the oxide and Si.

The peak concentration has reduced by three orders of magnitude in the interface for the $BF_2^+$ implanted wafer. This implantation through the oxide layer has been applied on some of the wafers processed for this project and the results have been analysed and compared with the wafers implanted directly without an oxide layer. See chapter 6 for the electrical measurements results.

![Figure 28 a) $B^+$ implantation through 10nm oxide and Si. b) $BF_2^+$ implantation through 10 nm oxide and Si. Si resistivity= 5 kΩ-cm.](image-url)
4.3.3 Choice of Annealing Schedule

The Si substrate undergoes a series of cascade and recoils during the implantation creating vacancy/interstitial defects. During the annealing the generated Si interstitials and vacancies recombine leaving a net excess of interstitials equal to the number of implanted ions [57]. The resulting of Si interstitials evolve into extended defects [58]. The Si interstitials are the underlying cause for the diffusion of boron during the annealing [59].

Annealing is required to repair the lattice damage after implantation and to electrically activate the dopant atoms. The success of the annealing process is not only measured in terms of the fraction of the dopants that are electrically active or to repair the damage in the crystal, which any long high temperature anneal will achieve, but also minimising the diffusion of the dopant and hence retain a shallow junction.

This is achievable with RTA (Rapid Thermal Annealing), where annealing times are in the order of seconds or even nanoseconds. Reference [60] has demonstrated that RTA is the most suitable industrial approach for the formation of shallow electrically active junctions.

Laser annealing has been used for a long time but due to integration issues hasn’t been implemented as an industrial process, for this reason it hasn’t been used for this project.

Figure 29 shows the activated $B^+$ concentration after two different annealing schedules. Some of the wafers processed for this project were annealed at 850 °C for 10 seconds and the others were annealed for 950 °C for 5 seconds. The energy used for this ion implantation in the active-area is 2 keV with a dose of $3 \times 10^{13}$ cm$^{-2}$, tilt=7° and rotation=22°. Figure 29 also shows that all the $B^+$ is electrically activated after the two annealing schedules. The differences between the electrical performances of the detectors annealed with these two different schedules are analysed in chapter 6.
Figure 29: a) Carrier profile for the atomic B⁺ as implanted and b) BF₂⁺ as implanted and the electrically active B⁺ after different furnace annealing.

The guard-rings needed another annealing schedule due to the different ion dose and energy in these regions.

Figure 30 shows the carrier profile for 1×10¹⁵ cm⁻², 100 keV, tilt=7° and rotation=22° atomic B⁺ as implanted in the guard-rings and the electrically active B⁺ after annealing for 2 minutes at 1050 °C.

Figure 30: Carrier profile for the 100 keV, 1×10¹⁵ cm⁻² atomic B⁺ as implanted and the electrically active B⁺ after RTA annealing for 2min at 1050 °C in the guard-rings.
4.4 Creating Two-Dimensional Implant Profiles in Athena

Athena calculates 2D implant profiles using a convolution method described as follows.

The implantation front (perpendicular to the direction, see Figure 22) is divided into a number of slices \( N_s \) usually \( > 100 \). The implant concentration in each grid point \( i \) with coordinates \((x_i, y_i)\) is calculated by the summation of contributions from each slice \( k \) [46]:

\[
C(x_i, y_i) = \sum_{1 \leq k \leq N_s} C_k(x_i, y_i)
\]

The contribution from each slice \( C_k \) is calculated by integration of the point source 2D frequency function \( F_{2D}(x, y) \) (with the starting point at the intersection of the normal \( n \) to the central of the slice with the structure surface) over slice width:

\[
C_k(x_i, y_i) = \phi \int_{-a/2}^{a/2} f_{2D}(d_i, t_i) dt
\]

where \( d_i \) is the depth along implant direction (i.e., distance between the starting point and the projection of the point \( i \) on the vector \( n \)) and \( t_i \) is the transversal distance (i.e., distance between the point \( i \) and the vector \( n \)).

The simplest type of the 2D frequency function is a product of longitudinal function \( f_l(x) \), which can be a Gaussian, Pearson, Dual-Pearson and depth-independent transversal function \( f_t(y) \) [61].

\[
f_{2D}(x, y) = f_l(x)f_t(y)
\]

This approximation is used in Athena by default.

Figure 31 shows the 2D implantation profile for the guard-rings. The guard-rings were implanted with \( B^+ 100 \text{ keV} \) with a dose of \( 1 \times 10^{15} \text{ cm}^{-2} \), \( \text{tilt}=7^\circ \) and \( \text{rotation}=22^\circ \).
Figure 31: 2D boron implantation profile for the guard-rings. The implantation energy is 100 keV, the dose is $1 \times 10^{15}$ cm$^{-2}$, tilt=7° and the rotation=22°.

4.5 The I-V Characteristic

There are three sources for the leakage current. The bulk, the surface and the diffusion all contribute to the leakage current. The bulk contribution comes from thermally generated charge carriers for example due to generation centres such as displaced atoms and impurities. The surface leakage current comes from the disruption of the Si lattice structure. The lattice disruptions introduce energy levels in the band gap and attract impurities. The diffusion current comes from the p$^+$ n and the n$^+$ n junction. This current is much smaller than the bulk and the surface currents. The leakage current is dominated by the surface leakage current for devices without biased guard-rings. See chapter 6 for more details.

The bulk leakage current is demonstrated by the formula below. The formula shows current density’s relationship to the depletion width [24].
\[ J_{vol} \approx -q \frac{n_i W}{\tau_g} \approx -q \frac{n_i}{\tau_g} \sqrt{\frac{2 \varepsilon_0 \varepsilon_{si} V}{q N_D}} \]

\( J_{vol} \) = the volume generation current per unit area

\( q \) = the elementary charge

\( n_i \) = intrinsic carrier density

\( \tau_g \) = the carrier generation life-time

\( W \) = depletion width

\( \varepsilon_0 \) = Permittivity in vaccum

\( \varepsilon_{si} \) = Si permittivity

\( N_D \) = donor impurity density

\( V \) = applied voltage

In absence of radiation, if a reverse bias is applied to the pin-diode detector, the current increases smoothly with the increase of voltage. As the voltage increases further, breakdown occurs which destroys the device, so the detector has to be operated at voltages below breakdown voltage.

Once the detector is produced the improvement of the noise is limited since we can't modify the capacitance or the transconductance of the input JFET. Therefore to achieve a high resolution the most effective solution is to reduce the leakage current. The I-V characteristic of the detector is important for the testing of the device as this determines the leakage current and the breakdown voltage. The performance of the pin-diode will depend on its leakage current. Low leakage current diodes will need less cooling to give good low noise.

Figure 32 shows the leakage current throughout the device. The leakage current is about 80 nA and the breakdown voltage is 140 V. The implantation energy for the active-area has been chosen at 2 keV with a dose of \( 3 \times 10^{13} \) cm\(^{-2} \).
Figure 32: The I-V characteristic.

Figure 33 shows the current density distribution throughout the device. The highest current density is at the edge of the anode around the active-area. The voltage applied on the anode is -300 V.

Figure 33: Current density distribution throughout the device.
Figure 34 shows how the leakage current increases in a different thermal environment. As the temperature increases by 100 K, the leakage current increases. This is the reason behind using a cooling system for X-ray detectors.

![Figure 34: I-V characteristic for various temperatures.](image)

4.6 The Depletion Voltage

When n-type and p-type semiconductor materials are placed together to form a junction, electrons diffuse into the p-side and holes into the n-side leaving behind a positive ion on the n-side, and likewise the hole leaves a negative ion on the p-side. The result is a region with no mobile carriers called the depletion region.

Chapter 2.2.3.4 described how the pin-diode can operate partially depleted. In order to ensure optimal efficiency for the detector, it is better to operate the pin-diode fully depleted. For this reason, the depletion voltage needed to fully deplete the detector must be known.

The total depletion width is the sum $W = W_n + W_p$. 

58
\( \mathcal{W}_p \) = depletion width in the p-region

\( \mathcal{W}_n \) = depletion width in the p-region

A full derivation for the depletion width is presented in reference [17]. This derivation is based on solving the Poisson equation in one dimension. Treating each region separately and substituting the charge density for each region into the Poisson equation eventually leads to a result for the depletion width as following [17].

\( v_{\text{dep}} \) = the potential needed to extend the depletion zone over the whole thickness of the wafer.

\( W \) = depletion width

\( v_{\text{bi}} \) = built-in potential

\( \mu_n \) = electron mobility

\( q \) = the elementary charge

\( \varepsilon \) = semiconductor permittivity

\( \varepsilon_0 \) = Permittivity in vacuum

\( N_D \) = donor impurity density

\( N_A \) = acceptor impurity density

\( n_i \) = intrinsic carrier density

\[
N_D = \frac{1}{q\mu_n \rho}, \text{ with the Si resistivity} = 5 \text{ k}\Omega\text{-cm chosen for this project}
\]

\[
N_D = \frac{1}{1.6 \times 10^{-19} \times 1500 \times 5000} = 8.3 \times 10^{11} \text{cm}^{-3}
\]

\[
v_{\text{bi}} = \frac{KT}{q} \ln \frac{N_A N_D}{n_i^2} = 0.0259 \ln \frac{2 \times 10^{19} \times 8.3 \times 10^{11}}{(1.4 \times 10^{16})^2} = 0.66 V
\]
\[ W = \sqrt{\frac{2\varepsilon_0 (N_A + N_D)}{qN_A N_D}} (v_{bi} - v) = \sqrt{\frac{2\varepsilon_0}{qN_D}} (v_{bi} - v) \quad \text{because } N_A >> N_D \]

To fully deplete the device with the wafer thickness of \( W = 450 \mu\text{m} \) for this project,

\[ v = v_{bi} - \frac{qN_D W^2}{2\varepsilon_0} = -128V \]

Thus, a 128 V reverse bias voltage is needed to fully deplete the device.

Figure 35 shows the depletion edge in the detector when a reverse bias of 128 V is applied on it. The red line throughout the detector indicates the edge of the depletion region and it shows that all the device thickness is depleted.

![Figure 35: The depletion edges (throughout the device) marked with a red line.](image)

### 4.7 The Potential and the Electrical Field

To investigate where in the device the breakdown occurs, we need to look at the potential and the electrical field diagrams for the device.
Figure 36 a) shows a potential diagram at equilibrium for a junction formed by p-type, intrinsic and n-type material. The Fermi potential is constant everywhere and is represented by $\phi$ [62].

The free hole (p) and electron (n) concentration in the equilibrium condition are:

$$p = n_i e^{\left(\frac{-q\psi}{kT}\right)}$$

$$n = n_i e^{\left(\frac{q\psi}{kT}\right)}$$

Where

$\psi$ is the potential of an electron at mid-gap position.

$n_i$ is the intrinsic carrier concentration.

Figure 36 b) shows a potential diagram of a p-i-n material in the non-equilibrium condition with positive voltage $V_a$ applied to the n-layer. $\psi_p$ is the potential deep inside the p-type material, $\psi_s$ is the potential at the surface and $Q_s$ is a net positive charge at the surface [62].

The free hole (p) and electron (n) concentration in the non-equilibrium condition are:

$$p = n_i e^{\left(\frac{q(\phi_p - \psi)}{kT}\right)}$$

$$n = n_i e^{\left(\frac{q(\psi - \phi_n)}{kT}\right)}$$

Where

$\phi_p$ is the quasi-Fermi level for the holes and $\phi_n$ is the quasi-Fermi level for the electrons.
Figure 36: Potential diagrams for a p-i-n junction a) at equilibrium and b) at non-equilibrium condition [62].

Under reverse bias due to the very light doping in the n type bulk, the depletion width extends primarily into the n region and hence the majority of the potential-drop exists across the bulk substrate.

Figure 37 shows the voltage distribution throughout the device when a bias voltage of 300 V is applied to the cathode (n-type layer). The highest voltage is located around the edge of the anode.

Figure 37: A cross-section of the device showing the potential distribution.
Figure 38 shows the electrical field through the pin-diode detector. The electrical field between the charged carriers are the highest in the intersection region between the \( B^+ \) doped anode and the phosphorous (\( P^+ \)) doped substrate (anode’s edges). Usually the breakdown occurs in this region for this reason. This is the reason behind the placing the guard-rings in this region: to ease the electrical field in the edge and consequently increase the breakdown voltage. A 300 V bias voltage has been applied to the cathode for this simulation.

![ATLAS The Electrical Field Throughout the Device](image)

Figure 38: A cross-section of the device showing the electrical field.

### 4.8 Guard-rings design

The simulations described in the previous sections showed that the pin-diode detector breaks down early and the leakage current is not as low as we expect. For this reasons, some guard-rings have been placed around the anode (see Figure 45 for their location in the detectors).

The breakdown occurs at the edge of the \( p^+ \) anode because the electrical field is the highest in this area. See Figure 38.
The guard-rings relax the electrical field at the edge of the anode and prevent the breakdown from occurring early. When placing the guard-rings, the electric field actually divides between them.

The guard-rings have been implanted with a dose of $1 \times 10^{15}$ cm$^{-2}$, 100 keV $B^+$, tilt=$7^\circ$ and rotation=$22^\circ$. See Figure 30 for the carrier profile.

**4.8.1 Modified I-V Characteristic**

Figure 39 shows the I-V characteristic for the pin-detector with different numbers of guard-rings. With the placing of guard-rings in the pin-diode detector, the leakage current reduces from 80 nA to 5 nA and the breakdown voltage is significantly higher. The more guard-rings in the structure, the higher the breakdown voltage becomes. The breakdown voltage is about 700 V, 850 V and 1300 V for pin-diode detectors with one, two and three guard-rings respectively.

The breakdown voltage is sensitive to the distance between the innermost guard-ring and the anode, the distance between the guard-rings, and also their widths. See chapter 4.9 for the structures.

Two, or in some detectors three, guard-rings have been placed around the anode. Their widths and distances have been optimised using Silvaco's VWF to get the highest breakdown voltage and the lowest leakage current.
Figure 39: I-V characteristic for the device without and with different numbers of guard-rings.

Figure 40 shows the current density distribution throughout the device with 3 guard-rings when breakdown occurs. There is some current generated from the guard-rings. This is shown with in a red colour, indicating the highest current density in the structure.

Figure 40: Current density distribution throughout the device with 3 guard-rings.
4.8.2 Modified Depletion Voltage

Figure 41 shows the depletion edge of the device. The guard-rings have pushed the depletion edge further from the anode and have made a bigger area depleted compared to the device without guard-rings. Compare with Figure 35.

![Depletion Edges](image)

Figure 41: The depletion edges for the device with 3 guard-rings.

4.8.3 Modified Voltage and the Electric Field

The purpose of the guard-rings is to distribute the potential drop from the centre to the edge of the device when a reverse voltage is applied. Figure 42 shows the cross-section of the detector with 3 guard-rings. It shows the potential distribution across the device. The guard-rings have pushed the potential away from the anode. Compare with Figure 37.
Figure 42: The potential distribution in the device with 3 guard-rings.

Figure 43 shows the electrical field between the anode and the innermost guard-ring and also between the guard-rings. The electrical field is the highest in these areas. Figure 43 b) shows a magnified picture of the area around the anode to have a better idea of the electrical field's distribution in this region.

Figure 43: a) The electrical field throughout the device with 3 guard-rings, b) A magnified picture of the region around the guard-rings.
4.9 Pin-diode Detector Structures

We designed a total of nine different pin-diode detectors for this project using Atlas. The structural differences lay in the number of guard-rings, choice of floating or contacted guard-rings, oxidised or Al contacted active-area, and also the presence of phosphorous doped edge called n⁺ layer. Figure 44 has been taken from the mask designed using Silvaco Expert and shows the chip used during the processing runs. There are nine pin-diode detector designs and some other devices for process evaluation purposes on the chip on the top right corner.

![Figure 44: The chip with nine different pin-diode detectors and some measuring devices](image)

A cross-section diagram for each of the detectors is shown in Figure 45: the grey colour indicates the oxide layer and the green¹ colour is the metal contact. The active-area is implanted with $BF_2^+$ or $B^+$ depending on the processing run and wafer (see chapter 6). The guard-rings are implanted with $B^+$. The n⁺ layer and the back of the devices are implanted with $p^+$.

Four pin-diodes (devices 1–4 inclusive) have 3 guard-rings each and the other five have 2 guard-rings. The guard-rings are floating in devices 1 and 7, while in the other devices they are covered by metal contacts. Notice that only one pin-diode (device 4) does not have an n⁺ layer around the edge of the device. Two devices 5 and 6 have an

¹ Reading note: darker shade if document is read in black and white
oxide layer on the active-area and the other devices have this region covered with AlSi 1%.

1) Device 1, with 3 floating guard-rings, n⁺ layer, deep implantation under the anode's contact and metalised active-area.

2) Device 2, with 3 contacted guard-rings, n⁺ layer, shallow implantation under the anode's contact and metalised active-area.

3) Device 3, with 3 contacted guard-rings, n⁺ layer, deep implantation under the anode's contact and metalised active-area.

4) Device 4, with 3 contacted guard-rings, no n⁺ layer, deep implantation under the anode's contact and metalised active-area.
5) Device 5, with 2 contacted guard-rings, n\(^+\) layer, shallow implantation under the anode’s contact and oxidised active-area.

6) Device 6, with 2 contacted guard-rings, n\(^-\) layer, deep implantation under the anode’s contact and oxidised active-area.

7) Device 7, with 2 floating guard-rings, n\(^-\) layer, deep implantation under the anode’s contact and metalised active-area.

8) Device 8, with 2 contacted guard-rings, n\(^+\) layer, shallow implantation under the anode’s contact and metalised active-area.
9) Device 9, with 2 contacted guard-rings, n+ layer, deep implantation under the anode’s contact and metalised active-area.

Figure 45: Schematics of device 1 to device 9 on the chip.

Figure 46 shows the 3-dimensional structure of Device 2 as an example. The active-area, the 3 guard-rings and the n+ layer are all covered by metal contacts in this design.
The pin-diode is 5x5 mm² with an active-area of 10 mm².

Figure 46: 3-Dimensional pin-diode detector.

Figure 47 shows one of the Silvaco Expert layouts for the devices for process evaluation shown in the top-right corner of the chip (Figure 44).

There are two small pin-diodes in the bottom to investigate the effect of size on the pin-diode’s electrical performance. These pin-diodes have an active-area of 1 mm² each. One has two guard-rings and the other one has 3 guard-rings. On the top there is one Cross-Bridge Kelvin Resistor (CBKR) device to measure the contact resistance (are explained in details in chapter 5.6), one device to measure the sheet resistance and one device to measure the carrier life-time. There are also 4 diodes in different sizes.
For measuring the carrier life-time

For measuring the contact resistance

For measuring the sheet resistance

Two small Pin-diode detectors

Figure 47: Metal layout in Expert for the test structures.

As illustrated in Figure 48, the chip is repeated on the glass mask - this gives an idea about the number of pin-diode detectors produced on a four inch wafer, which was used for this project.

Figure 48: Illustration of pin-diode detectors on a four-inch wafer.
5 Device Manufacture

Nine different pin-diode detectors have been processed at the University of Surrey's cleanroom and their electrical performance have also been analysed at the university's laboratories.

The processing techniques described in this chapter all have been applied on the wafers processed for this project in order to manufacture the pin-diode detectors. Where appropriate, the experimental results have been included in the subsections.

5.1 Oxidation

One of the first steps in the Si wafer processing is the oxidation of the wafer. When Si is exposed to an oxidizing ambient the oxygen or water vapour, builds a layer of oxide on the surface of the Si. This process is known as oxidation.

There are different methods to oxidise the Si wafer, namely by deposition and thermal oxidation. The thermally grown oxide has been used in this project.

5.1.1 Thermal Oxide Growth

There are two processing methods to grow the oxide layer thermally, namely dry or wet oxidation. If the oxidation ambient contains O\textsubscript{2} the process is called dry oxidation and if water vapour is also present in the oxidation system the process is called wet oxidation. For wet oxidation the oxygen is passed through a water container heated to 95 °C. This oxygen is then used together with the water vapour.

The chemical reaction for dry and wet oxidation is as following:

Dry oxidation: \( Si + O_2 \rightarrow SiO_2 \)

Wet oxidation: \( Si + H_2O \rightarrow SiO_2 + 2H_2 \)
The oxidation reaction occurs at the Si/SiO₂ interface. Therefore as the oxide layer grows, Si is consumed and the interface moves into the Si substrate. The amount of the consumed Si is about 44% of the final oxide thickness and it depends on relative densities and molecular weights of Si and SiO₂. The SiO₂ layer shields the incoming oxygen molecules from reaching the Si surface and the oxidation eventually stops. At room temperature the thickness of the native oxide layer is 1-2 nm [63].

The growth rate of the oxide depends on various factors such as the temperature, pressure, amount of oxidant in the system, type of oxidant, Si crystallographic orientation, dopant type and dopant concentration in the Si, the presence of a chlorine gas in the ambient and the partial pressure of water present during the oxidation [63-65].

To grow a specific thickness of oxide, it is more time consuming to use dry oxidation than the wet oxidation method [64].

Si atoms at the interface are partially bonded to Si atoms below the interface and bonded to the oxygen atom above the interface. The oxidation growth rate is derived from the concentration of Si-Si bonds available for reaction with oxygen. The bond availability depends on its angle relative to the surface plane. These and other geometric effects result in the oxidation rate to be orientation dependent.

The oxidation rate is highest for (111) Si followed by (110) Si and (100) Si for both dry and wet oxidation [66, 67].

Dopant types and their densities in the Si substrate also affect the oxidation rate. The commonly used group III (B) and group V (P, As) dopants in Si enhance the oxidation rate when present in high concentration on the Si surface. In the case of B the dopant segregates into the oxide and remains there during the oxidation. This weakens the bond structure in the oxide and provides a path for the oxidant to diffuse further in the oxide and reach the interface, thus enhancing the oxidation rate. Other group III dopants like Ga, In and Al also pile up in the oxide but rapidly diffuse away from it and do not enhance the oxidation growth [68].

The mechanism is the opposite for p⁺ doped Si. When the p⁺ doped Si is oxidised the Phosphorus segregates into the Si and very little is incorporated into the oxide. The
high concentration of Phosphorous at the surface shifts the Fermi level, which in turn increases vacancies in the Si surface. The excess vacancy concentration increases the chemical reaction of the oxidant with the Si, therefore the oxidation rate increases [69-71].

The presence of water vapour during dry oxidation is another factor, which affects the oxidation growth rate. There are several sources for the water molecules: 1) absorbed water on the wafer. 2) residual water in the oxygen source gas. 3) residual hydrogen or hydrocarbons which react with oxygen to form water. 4) the diffusion of water vapour into the furnace from the surrounding area [65].

In practice it is extremely difficult to exclude all traces of water during dry oxidation. However the residual hydrogen and hydrocarbons in the Oxygen can be removed by passing the oxygen through a combustion of these materials to form water and then remove the water from the system. To minimise the water contribution from the surrounding area to the furnace, a double-wall furnace tube can be used with a gas filled gap. Reference [67] concludes for each Si orientation and at each experimental temperature the overall rate of oxidation is increased with the addition of as little as 25 ppm of water added to very dry oxidation.

SiO$_2$ has many uses in semiconductor devices. SiO$_2$ is used as a screen oxide to mask the areas on the Si surface, which will not be implanted. The required oxide thickness for masking the wafer can be determined by using a simulation program such as Athena and it depends on the implantation energy of the ions and the dose. The oxide is also used to create a shallow junction in the Si substrate.

In this project the SiO$_2$ is used as a layer with no electrical function and is used to pattern the surface for alignment marks in photolithography. It is also used as a passivation layer to protect the Si surface from the environment [72].

In the first step for this project the wafers were oxidized at 1000 °C for 2 hours to have a layer of 500 nm oxide on the wafers. This oxide layer has been used as a passivation layer and also by etching patterns on it, creating alignment marks on the surface for the photolithography purpose. Later a layer of 10 nm oxide was grown on the Si as a passivation layer and also to create a shallow $B^+$ junction on the surface, see chapter 4.
5.1.2 Oxidation System

There are several thermal processing equipment for various applications in the semiconductor industry. A horizontal furnace is used for the oxidation of the wafers for this project. The wafers in the horizontal furnace sit on the edge of the boat.

During the loading or unloading of the wafers it is better to run a flow of Nitrogen gas. This will help to prevent the wafers from suddenly heating up or cooling down, which can cause stress in the oxide layer.

When the wafer cools down from the oxidation temperature to the room temperature, the Si contracts more than the oxide and this builds in stress in the oxide. This stress originates from the difference between the thermal coefficients of expansion of the two materials (Si and the oxide). Another source of stress comes during the growth of the oxide as a result of the way the oxide is grown and it occurs in the Si/ SiO₂ interface. Reference [67] calculates the stress and shows that for temperatures up to 950 °C the oxide is in a state of compressive stress and the stress disappears for the temperature of 975 °C.

5.1.3 Rapid Thermal Processor Systems

Rapid Thermal Processor (RTP) is a key fabrication technology for semiconductor devices and are used for oxidation purposes and annealing process [73].

RTP is a single wafer, fast ramp thermal processing that is capable of heating up the wafer from the room temperature to 1100 °C in a matter of seconds.

Accurate temperature measurement is considerably more challenging in an RTP system than in a traditional furnace since it is the temperature of the wafer, not the furnace, which must be measured and controlled. The wafer itself is the most important and unpredictable variable in an RTP system, as its properties vary depending on the doping concentration and surface layers. The heating cycles for lightly and heavily doped wafers are different because their optical properties are
different. Lightly doped wafers absorb very little of the heat, and so heat up very slowly. Heavily doped wafers absorb the heat efficiently, and heat up much faster [74].

A nitrogen ambient permits heat transfer by conduction and reduces the influence of the wafer's optical properties on the thermal cycles. The heating rates are therefore considerably higher in nitrogen than in vacuum.

In the RTP furnace the wafer is loaded into the system by being placed on a plate and there are pins, which separate the wafer from touching the plate. The wafer is heated by halogen lamps located on top of the wafer. See the image in Figure 49. The lamps are arranged in a honeycomb structure to give the closest packing of radiant energy. A thermocouple is used for temperature control and measurement, by placing it in direct contact with the back of the wafer.

![Figure 49: Simplified schematic of a rapid thermal processor used for this project [75].](image)

The measured temperature is compared with the recipe temperature (desired temperature) in the controller. Then through a complex algorithm this will change the power of each lamp to adjust the heat [76, 77].

RTP systems are smaller and symmetrically designed than the traditional furnaces. This allows them to benefit from a uniform gas distribution. Also in the RTP systems the wafers can be loaded and unloaded through a vacuum loadlock.
The latest technology in the field of thermal furnaces are fast ramp and small bench furnaces, which are competing with the Rapid Thermal Processors (RTP) systems [78-81].

5.1.4 Measurement Methods of Oxide Thickness

There are several techniques available to measure the thickness of the oxide: optical interference, capacitance measurements, physical thickness measurements and ellipsometry.

The optical measurement’s method is based on the interference that occurs between light reflected from the air/oxide and the Si/oxide interface. To perform the measurement a spectrophotometer is used, which supplies light from the ultra violet to the visible range. The intensity of the reflected light from the sample is measured as a function of wavelength. The measurements are then fitted to calculate the film thickness. A number of points are easily and rapidly measured across the wafer (thickness map), which shows the variation of the thickness across the wafer. This system is capable of measuring the thickness of multiple layers and from a thickness less than 10 nm to more than 1000 nm.

The capacitance measurement can be used to theoretically measure the thickness of the oxide according to the formula below. This requires the fabrication of a MOS capacitor.

\[ t_{ox} = \frac{C_{ox} A}{\varepsilon_{ox} \varepsilon_0} \]

- \( C_{ox} \) is the oxide capacitance in a F/cm\(^2\)
- \( A \) is the area of the gate electrode in cm\(^2\)
- \( \varepsilon_{ox} \) is the dielectric constant of the oxide
- \( \varepsilon_0 \) is the permittivity of free space
$C_{ac}$ has to be measured in the accumulation mode (negative voltage on the gate for P-type and positive voltage for n-type) to ensure that the Si capacitance doesn’t contribute to the measurement. Wafer map is possible by measuring several points across the wafer.

The most accurate measurement of the film thickness is obtained by preparing a cross section of the film on the substrate and to take a high resolution transmission electron microscope picture. Since the Si lattice can be seen in the picture, this can be used as the distance for the interface. In addition the roughness of the interface can also be seen. Since sample preparation is time consuming and expensive this method is not favourable and it is not possible to determine the uniformity of the oxide layer using this method.

The ellipsometry technique is the most common used method to measure the thickness of an oxide. It is based on change of polarisation of the light when it hits the Si/ SiO$_2$ interface. The polarisation change depends on the optical constants (the refraction index and the extinction coefficient) of Si, the angle on incidence of the light and the optical constants of the film and the film’s thickness. Complex algorithm is used to calculate the thickness of the film in ellipsometry. The mean thickness value along with maximum and minimum film thickness on the wafer is displayed on the ellipsometer. The standard deviation in percentage of mean is also shown. It is also possible to measure thin thicknesses as the native oxide from 1 nm and to map the whole wafer [82-85].

The ellipsometer for this project was used to measure different thicknesses of oxide grown on the wafers, the metal layer deposited on the wafers and also the thicknesses of multi-layer films such as photoresist on SiO$_2$ on Si.

5.1.5 Experimental Results for the Oxidation

Wet and dry oxidation techniques have been used for this project. The oxidation technique chosen for this project depended upon the thicknesses of the oxide required. A horizontal furnace has been used for the wet and dry oxidations.
Prior to any oxidation, it is important to analyse the furnace's temperature profile. This will help to accurately reach the desired temperature in the furnace and where to place the wafers in the furnace.

In the case investigated below the aim was to oxidize wafers processed for this project at a temperature of 1000 °C.

Figure 50 shows the temperature profile for the furnace in a wet oxidation environment for different gas flows under similar settings on the temperature regulators on the furnace. It shows that the temperature is constantly at 1000 °C, 23 inches to 25 inches from the opening of the elephant when the gas flow is 50 L/h.

In order to expand the area where the temperature is constant, the temperature regulators were tuned. There are three temperature regulators on the furnace, one in the back, one in the middle and one in the front of the furnace. For the experiment below, the regulator in the front of the furnace was constantly set at 500 °C, the middle regulator was set constantly at 513 °C and the regulator on the back was tuned to temperatures between 600 and 700 °C as shown in Figure 51. These combinations of settings warmed up the furnace temperature from 1000 to 1050 °C. The oxidation method was wet process and the gas flow was 50 L/h.
When the back regulator was set at 675 °C, the temperature in the furnace was constantly 1000 °C from 10 to 32 inches from the opening of the elephant, meaning that any wafers placed in this region are warmed up to 1000 °C; moreover, over a long distance of 22 inches the furnace temperature is constant. This setting was used to oxidise the wafers for the first time in order to grow 500 nm of oxide on the wafers.

![The Temperature Profile for the Furnace for Different Furnace Settings](image)

**Figure 51: The temperature profile for the furnace for different furnace settings.**

Various thicknesses of oxide layers were grown on test Si wafers to experiment for this project in order to find the right recipe for the actual Si wafers.

A thick layer of oxide 510 nm was grown on the actual wafers processed for this project. The purpose of this thick layer of oxide was to pattern the alignment marks on the wafers in the photolithography step and to use it as a passivation layer. A thin layer of oxide about 10 nm was also grown on the wafers to screen the active-area on the X-ray detectors to be able to create a thin junction during the $B^+$ implantation. It also was used as a passivation layer to cover and protect the active-area on the detectors without a metal layer on these regions. See the structure in chapter 4.

Table 5 shows the oxide thickness measurements using the ellipsometer for different temperatures, duration times and oxidation types.
σ₁ and σ₃ in Table 5 indicate the first and the third standard deviation in the normal or Gaussian distribution respectively.

To achieve a thickness of 500 nm of oxide it is suitable to carry out wet oxidation because this is a thick layer and it requires a long time. At 1000 °C it will take 2 hours to grow this thickness. To grow thinner oxide layers, dry oxidation method was used as shown in Table 5.

<table>
<thead>
<tr>
<th>Mean Thick (nm)</th>
<th>σ₁ (nm)</th>
<th>σ₃ (nm)</th>
<th>Min Thick (nm)</th>
<th>Max Thick (nm)</th>
<th>Gas flow (L/h)</th>
<th>Duration time (min)</th>
<th>Furnace Temp. (°C)</th>
<th>Type of oxidation</th>
</tr>
</thead>
<tbody>
<tr>
<td>510</td>
<td>9</td>
<td>27</td>
<td>488</td>
<td>523</td>
<td>50</td>
<td>120</td>
<td>1000</td>
<td>Wet</td>
</tr>
<tr>
<td>491</td>
<td>11</td>
<td>34</td>
<td>472</td>
<td>511</td>
<td>25</td>
<td>120</td>
<td>1000</td>
<td>Wet</td>
</tr>
<tr>
<td>361</td>
<td>8</td>
<td>23</td>
<td>350</td>
<td>372</td>
<td>25</td>
<td>60</td>
<td>1000</td>
<td>Wet</td>
</tr>
<tr>
<td>275</td>
<td>5</td>
<td>10</td>
<td>263</td>
<td>289</td>
<td>25</td>
<td>45</td>
<td>1000</td>
<td>Wet</td>
</tr>
<tr>
<td>40</td>
<td>2</td>
<td>10</td>
<td>36</td>
<td>45</td>
<td>25</td>
<td>120</td>
<td>905</td>
<td>Dry</td>
</tr>
<tr>
<td>20</td>
<td>0.8</td>
<td>2</td>
<td>19</td>
<td>24</td>
<td>25</td>
<td>15</td>
<td>960</td>
<td>Dry</td>
</tr>
<tr>
<td>17</td>
<td>0.8</td>
<td>2</td>
<td>16</td>
<td>20</td>
<td>25</td>
<td>45</td>
<td>905</td>
<td>Dry</td>
</tr>
<tr>
<td>10</td>
<td>0.3</td>
<td>1</td>
<td>10</td>
<td>11</td>
<td>25</td>
<td>30</td>
<td>905</td>
<td>Dry</td>
</tr>
</tbody>
</table>

Table 5: Various thicknesses of oxide layers using wet/dry oxidation for different temperates and duration times.

Figure 52 shows the result of the 510 nm oxide layer mentioned in Table 5 measured by using the ellipsometer. It shows how uniform the oxide layer is on the Si substrate.
5.2 Sources of Contamination in Wafer Processing

The effects of contamination on semiconductor devices are complex and depend on the nature and the quantity of the specific type of contaminant but one aspect they have in common is that they degrade the electrical performance of the device.

Particles can block an implant or disrupt a pattern during photolithography. Particles can also be deposited on a wafer’s surface before the deposition of a layer over it.

If the particle is interfering with the contact regions, a short or an open circuit in the manufactured detector can occur. A single particle has the potential to make the detector not function correctly.

Metallic contaminations such as Cu and Fe diffuse inside the Si bulk especially during thermal processing. These metals introduce energy levels near the middle of the Si energy band gap. This leads to reduced minority carrier life-time, increased junction leakage current and reduced breakdown voltage. Sources of metal contaminations in wafer processing include ion implanters and dry stripping and etching equipment.

Figure 53 shows the solid solubility of impurity elements in Si in the temperatures between 500-1400 °C.
Contamination can be particles generated from cleanroom personnel and processing equipment, dust and even bacteria grown in the Deionised water (DI) supply system.

Residues from solvents can contain metallic and ionic contaminations. Photoresist used in the processing of the wafer can also damage the wafer by being contaminated; also during the developing of the film, some dry photoresist can stick to the wafer.

Organic film residue can carbonise and if it is present on the wafer and being heated, the residue will form SiC on the surface of the wafer.

Processing equipment can introduce particles in the system through pumping, venting, gas flow and valve operation. If an oil-sealed vacuum pump is used in any processing equipment, oil particles can be carried in the air or the gas and contaminate the wafer.

The containers for the processing chemicals and the cassettes for holding the wafers are a major source of particles.

Human beings are immense generators of particles. Particles originate from hair, skin flakes, cosmetics (especially powders and hair spray). Humans create numerous water droplets and particles into the air with every exhalation.
5.3 Wafer Handling

Clean wafers are critical for fabrication of detectors with high yields and long term functionality. Cleaning of the wafers is essential during the processing of the wafer to eliminate any existing particle from the surface. The cleaning process is crucial before the thermal processing of the wafer. This will minimise the particle diffusion in the wafer during the annealing and also enable us to grow a high quality oxide layer during the oxidation.

The cleaning procedure has to be done without damaging the wafer and with minimal production of hazardous chemical wastes.

5.3.1 Cleaning Process for the Wafers

The first step toward the reduction of the contamination in the cleanroom is to minimise human contamination introduced to the cleanroom. For this reason, users have to wear special uniforms, boots, hoods, gloves and face masks. The fabrics of the garments are special woven fibre covered with PTFE (Polytetrafluoroethylene). Such fabric is particle tight but still allows air to go through. Special care is taken with these garments during the laundering and storing.

Gases used in the cleanroom are highly pure. They can also be filtered before the use to remove some unwanted particles. For this project DI water, chemicals and solvents in high purity grade where used.

There are various wafer cleaning procedures depending on the type of contaminations. The main categories are dry or wet cleaning procedures. Liquid chemical cleaning processes are generally referred to as wet cleaning. The other cleaning methods, which operate without using liquid chemicals, are classified as dry cleaning.
5.3.1.1 Wet Cleaning Procedures

Wet cleaning remains dominant over dry cleaning because of overall higher cleaning strength. The disadvantages of using wet cleaning over dry cleaning are that it is usually more costly, wafer drying difficulties and chemical waste disposal.

The disadvantages of using the dry etching are that they cause surface roughness. This is because most of the gas-phase chemistries cannot selectively interact with the surface metallic contaminants without reacting with the Si substrate at the same time.

Dry cleaning processes do not replace the wet cleaning [86, 87], but can be used in processes where wet cleans are impractical or inadequate or to complement the wet cleaning as it was used for this project.

5.3.1.1.1 RCA Cleaning

In 1965 the first wafer cleaning procedure was developed by Werner Kern while working for RCA (Radio Corporation of America). The cleaning process was applied on both bare and oxidised Si wafers. Since then this cleaning process has been widely used and it is still carrying the same name (RCA cleaning).

The first step in the RCA cleaning process is called Standard Clean-1 (SC-1). In this step all organic contamination, some metals (i.e., Au, Ag, Cu, Ni, Cd and Cr) and particles are removed from the wafer's surface. RCA SC-1 is performed with solutions of $\text{H}_2\text{O}/\text{H}_2\text{O}_2/\text{NH}_4\text{OH}$ (5:1:1 volume) at 70°C. This cleaning treatment results in the formation of a thin layer of oxide (10 Å) on the Si surface. To remove this, Hydrofluoric acid (HF) is used [65].

Concentrated HF (typically 49% water) etches SiO$_2$, but the etching is too quick using this chemical. For more controllable etching process, Buffered HF is used.

Buffered HF contains 6 volumes of ammonium fluoride ($\text{NH}_4\text{F}$ ) 40% in water, and 1 volume of HF. Buffered HF is used to etch thin films of oxide or Si nitride ($\text{Si}_3\text{N}_4$). The etch rate of thermal oxides at room temperature in buffered HF is about 1000
A/min but varies with temperature, etch solution and also the oxide density. The difference in the density is caused by the oxidation temperature, pressure and also wet or dry oxidation effect (see chapter 5.1 for oxidation).

SiO$_2$ is attacked by hydrofluoric acid (HF) and produces Hexafluorosilicic acid and water.

$$ SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O $$

The second step in the RCA cleaning is called Standard Clean-2 (SC-2). In this step all inorganic ions, alkali ions and heavy metals (Li, Al, Ti, Zn, Cr, Fe, Ag, Pd, Au, S, Cu, Ni, Co, Pd, Mg, Nb, Te, W, Na) are removed from the surface of the wafer. RCA SC-2 solution is performed with a 1:1:6 solution of HCl + H$_2$O$_2$ + H$_2$O at 75 or 80 °C.

5.3.1.1.2 Piranha Cleaning

This solution has earned the name of Piranha cleaning because it attacks organic materials aggressively. The Piranha solution is made of 3 volumes of hydrogen peroxide (30% H$_2$O$_2$) added to 7 volumes of Sulphuric acid (98%H$_2$SO$_4$). If photoresist is present on the wafers, it is removed by immersion in this solution at 100-130 °C for about 10 min. Upon removal, the wafers are rinsed in DI water.

Challenges for currently used cleaning techniques include the need for continued performance improvement in submicron particle removal, environmental impact from the considerable chemical consumption and chemical waste, drying difficulties, and impact on production cost.

In this project, RCA cleaning and Piranha cleaning were used to clean the wafers during the processing. Buffered HF and concentrated HF were also used to remove thin and thick oxide layers.

5.3.1.1.3 Photoresist Removal

One of the important aspects in wafer cleaning is the removal of the photoresist.
Photoresist is made of organic solvents, polymers and photoactive compounds. The vast majority of the elements are Carbon (C), Oxygen (O) and Nitrogen (N).

The main objective in resist stripping is to ensure that all the photoresist is removed without attacking any underlying surface materials. Piranha solution at 120 °C can be used to remove the resists from non-metalized wafers. H$_2$O$_2$ in the Piranha solution is an oxidant and in the Sulphuric acid will help the acid to break down the photoresist. The H$_2$O$_2$ will oxidize the carbon from the bath and build CO$_2$ or CO. H$_2$O$_2$ also reacts with the water in the bath resulting in high temperature.

Photoresist that has not been exposed to high energy processes such as ion implantation is relatively easy to strip. Simple solvents are generally sufficient to remove this photoresist.

Acetone, Trichloroethylene (TCE), phenol-based strippers are used to remove positive photoresists. Methyl ethyl ketone (MEK) (CH$_3$COCH$_3$) and Methyl isobutyl ketone (MIBK) (CH$_3$COCH$_2$CH$_3$) are used on negative photoresists [88].

For this project, cleaning was carried out using the solvents Acetone, Methanol, Isopropanol so as to remove the photoresist when the photoresist hadn’t gone through an ion implantation. Photoresist loses hydrogen and oxygen during the ion implantation and forms a highly carbonised layer that is resistant to chemical cleaning. If this layer is not removed completely, it can affect the detector’s properties [89].

In cases where the photoresist was hardened after the implantation of the wafers, plasma asher with oxygen (dry etching) was used as in addition to the wet cleaning. Dry strippers such as oxygen plasma break down the Oxygen molecule O$_2$ in the resist to atomic oxygen or form Ozon (O$_3$). The oxygen atoms also react with the carbon in the photoresist to form CO$_2$ or CO and hence the photoresist is removed.

### 5.3.2 Wafer Drying and Storage

An important aspect of wet cleaning is the final drying step. Any water marks following the drying of the wafer, introduce particle recontamination from static
charges. The drying method, utilised for this project, consisted of blowing the wafers with dry nitrogen and then heating them on a hot plate.

After drying the wafers, they were removed to a cassette and transferred as rapidly as possible to the appropriate process tool. They were also stored in closed containers in the cleanroom.

5.4 Photolithography

Photolithography involves the following steps:
- Surface preparation
- Spin Coating
- Prebaking
- Mask alignment
- Light exposure
- Development
- Post-baking

5.4.1 Surface Preparation

The surface preparation involved the cleaning of the wafer. Contaminants and residue of previous photoresist were removed prior to the photoresist coating.

Before coating the photoresist, adhesion promoters are used to assist the resist coating. Primers are used as adhesion and they form bonds with the wafer’s surface and produce an electrostatic surface. Primers used for Si are Hexamethyldisilazane (HMDS) ((CH₃)₃SiNHSi(CH₃)₃)), Trichlorophenylsilane (TCPS) (C₆H₅SiCl₃) and Bistrimethylsilylacetamide (BSA) ((CH₃)₃SiNCH₃COSi(CH₃)₃) [88].
HMDS was used on the wafers processed for this project. It was sufficient to keep the surface of the wafer over the primer for 1 minute. The vapour reaches the wafer and leaves a coat on the surface.

5.4.2 Spin Coating

After using the primer, the wafer was held on a spinner chuck by vacuum and the photoresist was coated.

There are two types of photoresist, namely positive and negative. For the positive resists, after being exposed to the UV light, the chemical structure of the resist changes so that it becomes more soluble in the developer. The exposed resist is then washed away by the developer solution, leaving windows of the bare underlying material.

Negative resists function in the opposite manner. Exposure to the UV light causes the negative resist to become polymerized and more difficult to dissolve. Therefore, the negative resist remains on the surface wherever it is exposed, and the developer solution removes only the unexposed parts. Figure 54 shows the pattern differences generated from the use of positive and negative resist.

Figure 54: Process flow for Photolithography.
The manufacturer’s data sheet for the photoresist, provides the information required to properly select the spinning time and speed to meet process dependent thickness specifications. It also covers the handling precautions and the storage method of the photoresist [90]. We have used a positive photoresist for this project. It would not have made any difference if we had chosen a negative photoresist. Our choice was dictated by availability.

Photoresist should be stored and developed under yellow light. Therefore the photolithography was carried out in the yellow-room in the cleanroom.

### 5.4.3 Prebaking

After the spin coating, prebaking also known as soft-baking is used to evaporate the resist solvent and to densify the resist. Usually hotplates are used. Commercially, microwave heating or IR lamps are also used in production lines. The thickness of the resist is usually decreased by 25% during the prebake for both the positive and negative resists. The photoresist becomes photosensitive or imageable only after soft-baking. The prebaking duration time and temperature were determined carefully through several experiments.

Too much prebaking will degrade the photosensitivity by either reducing the developer solubility or actually destroying the sensitizer (chemical compounds in the resist capable of light emission). On the other hand, too short prebaking period will prevent light from reaching the sensitizer.

### 5.4.4 Mask Alignment

Following the prebaking stage, the wafer is aligned to the mask using a mask aligner. There are three methods to do so, namely contact, proximity and the projection alignments.

In the contact printing, the resist-coated Si wafer is brought into physical contact with the photomask and exposed with UV light while the wafer is still in contact position
with the mask. Because of the contact between the resist and the mask, very high resolution is possible in contact printing (0.5 or 1 micron). The problem with contact printing is that particles trapped between the resist and the mask can damage the mask and cause defects in the pattern on the wafer.

The proximity exposure method is similar to contact printing except that a small gap, usually of 10 to 25 microns, is maintained between the wafer and the mask during the exposure. This gap minimizes the mask damage.

For contact and proximity alignments, the mask is the same size and scale as the printed pattern on the wafer.

Projection printing avoids mask damage entirely. An image of the patterns on the mask is projected onto the resist-coated wafer, which is a few centimetres away. The image on the mask is focused and reduced by a lens, and projected onto the surface of the wafer. Projection printers are capable of approximately 1-micron resolution.

In more complex research systems, the technology goes one step further and uses direct writing on the wafer without using any masks. This can be accomplished using lasers for geometries of 1-2 microns; electron beams for geometries of 0.1-0.2 micron; and focused ion beams for geometries of 0.05-0.1 micron.

For this project, proximity printing was used during the photolithography of the wafers.

The photolithography masks are usually made of Fe$_2$O$_3$ on soda lime glass, Cr on soda lime glass or Cr on quartz glass (most expensive). There are also light and dark field mask types. Figure 55 shows how to print a pattern on a wafer using a light or dark-field mask. The shaded brown color indicates the Chrome on the mask.
For this project eight different light-field masks made of Cr on quartz glass were used during numbers of photolithography processes applied on the project wafers.

5.4.5 Light Exposure

The exposure parameters required in order to achieve accurate pattern transfer from the mask to the photoresist depend primarily on the wavelength of the radiation source and the dose. Different photoresists exhibit different sensitivities to different wavelengths. The dose also varies with the thickness of the photoresist. The manufacturer’s data sheet provides the information needed for this step of photolithography [90].

5.4.6 Development

After the exposure the wafer will be developed in a suitable solvent. The developer removes the exposed photoresist. There are different developers depending on the
type of the photoresist. Developing requires an accurate timing. Under or over-developing will result in destroying the patterns on the wafer.

5.4.7 Post-baking

The final step in the photolithography is the post-baking (or hard-baking) of the photoresist. This will stabilise and harden the remaining photoresist on the wafer.

The post-baking protects the photoresist so as not to come off easily during the etching, ion implantation or other processes. The post-baking's temperature is usually 5-15 °C higher than that for soft-baking and it lasts for about 20-30 minutes. Some shrinkage of the photoresist may occur following the post-bake.

Figure 56 shows a photo of the photolithography applied to one of the wafers processed for this project. The mask-aligner is in the background.

Figure 56: Photolithography applied on one of the wafers processed for the project.
5.5 Ion Implantation

In the 1970s ion implantation took over from diffusion as a way to introduce controlled amounts of dopants into the wafers. In the implantation the doping atoms are ionized, accelerated and shot directly to the wafer. The regions that are not implanted can be masked by using a layer of material such as photoresist, polysilicon or oxide. The thickness of these materials has to be adjusted for the penetration depth of the ions.

The penetration of the ions and hence the doping profile can be adjusted by choosing the implantation energy.

Ion implantation equipment typically consists of an ion source, where ions of the desired element are produced, an accelerator, where the ions are accelerated to a high energy, and a target chamber, where the ions impinge on the targeted wafer.

Typical machines used in the manufacture of electronic devices use beam energies in the range 200eV up to 2MeV.

Ion implantation is a clean process but great care has to be taken in designing and operating the implanter to achieve low contamination levels [91].

Figure 57 shows a plan view schematic of Surrey Ion Beam Center’s Danfysik 1090 ion implanter, implant range 2 keV to 200 KeV. This ion implanter was used for all the implantations carried out on the wafers processed for this project.
The major factors affecting the successful exploitation of ion implantation are the range distribution of the implanted atoms, the lattice disorder created, the location of the implanted atoms within the unit cell of the crystal, channeling, the annealing treatment and the subsequent electrically activated ions.

We will consider all of these factors briefly in the present chapter in order to obtain an overall picture of the problems involved.

The periodical placement of the Si atoms leads to channelling of the doping atoms. Channeling plays an important role and has an effect on the electrical characteristics of the detector.

In order to prevent channeling, the wafers are tilted by 7 degrees with respect to the (100) plane of the crystal and rotated 22 degrees.

With ion doses below $1 \times 10^{14} /\text{cm}^2$, channeling effects become more serious even for the common 7° tilt angle and can cause a variation of sheet resistance value if implantation angles are not optimized [92-95].
The secondary-ion mass spectrometry (SIMS) technique was used to obtain the ion concentration profile for one of the wafers processed for this project. The measurement was performed at Cascade Scientific Ltd.

Figure 58 shows the SIMS measurement and the Monte Carlo simulation result for one of the wafers implanted with 2 keV $B^+$, $3 \times 10^{13}$ cm$^{-2}$. The Monte Carlo model is a good fit to the SIMS result.

![SIMS and Monte-Carlo B profile for the active-area](image)

**Figure 58:** Sims analysis on one of the wafers implanted with 2 keV $B^+$ $3\times10^{13}$ cm$^{-2}$ in comparison to the Monte-Carlo model.

### 5.6 Annealing

After the implantation, the doping atoms are usually not in regular places in the crystal lattice and are not electrically activated. In addition the crystal is damaged by the implantation. For light ions like $B^+$ the lattice damage occurs mainly at the end of the projected range, while for heavy ions like arsenic the damage occurs over the whole track.
An annealing process after completion of the implantation is required to repair the lattice damage and activate the implanted ions. The most important aspect in any annealing process is to achieve a high dopant activation, while at the same time maintaining the shallow junction and removing of end of range damage [96-100].

During annealing, point defects (interstitials) extend into the bulk and cause TED, which is one of the issues when fabricating high quality shallow junctions. There is also a movement of the interstitials to the surface causing broadening in the concentration peak in the surface [101-103].

Experimental observation has showed that laser and RTA annealing make initial electrical activation up to a level of $10^{21}$ cm$^3$ possible and also maintain a shallow junction. However, deactivation occurs during additional thermal treatments [102, 104-109].

For this project several annealing processes were carried out. The first annealing was carried out after the implantation of the p$^+$ in the n$^+$ layer and the back of the wafer, and the $B^+$ implantation of the guard-rings. This annealing was for 2 min at 1050 °C. For the shallow junction $B^+$ implantation on the active-area, annealing was carried out for 5s at 950 °C on some of the wafers and for some other wafers these parameters were changed to 10s at 850 °C (See the simulation results in chapter 4.3.3). This process gave us an opportunity to have a split in the processing of the wafers. The results of each batch has been analysed in chapter 6 and the best processing configuration has been determined.

5.6 Metallization

Metallization is a technique used to deposit a thin film of a metallic material on the surface of the substrate.

Metallization was used to provide low resistivity contacts on the detectors. The contact metal should be a good conductive, non-reactive, thermally and electrically stable. The most common metal used as an interconnect material is Al because of its low resistivity $\rho=2.7 \,\mu\Omega$cm and good adhesion on Si and oxide.
Al can either be evaporated or sputtered.

For this project we sputtered the metal contacts on the detectors. The advantages with sputtering over the evaporation are that less damage occurs on the surface of the substrate and the deposited film is more uniform.

In the sputtering method plasma at higher pressure is used to knock metal atoms out of the target. The substrate such as a Si wafer is placed in the path of these ejected atoms and a thin layer of the target material will be coated on the wafer.

Si is highly dissolvable in Al. Therefore there is a risk that the Si might dissolve into the Al during the annealing and Al spikes will grow into the Si. To avoid this phenomenon (spiking), a small amount of Si is usually added to the Al. A mixture of 1% of Si in Al (AlSi1%) was used for the sputtering of the contacts in this project.

A good ohmic contact to the Si substrate is provided only if the Si regions under the contacts are highly doped. Furthermore For obtaining a good electrical contact to the Si a sintering step is necessary [63].

Sintering was carried out after the deposition of the metal contacts. This step is necessary to ensure creation of an ohmic contact. To determine whether the annealing time and temperature were sufficient, some experiments were carried out on the test structures (Cross-Bridge Kelvin Resistor) provided for evaluation of the contacts.

Cross-Bridge Kelvin Resistor (CBKR) structures are the most widely used test structures to characterize whether the metal–semiconductor contacts are ohmic or not. The measurement principle consists of forcing the current between pad 1 and 2 and measure the voltage drop between pad 3 and 4 [110]. See Figure 59.
The measured Kelvin resistance can then be found as:

\[ R_k = \frac{V_{34}}{I} \]

In the 1-D Model approach, the contact resistance can be calculated directly from the contact area \( A \) and the contact resistivity \( \rho_c \).

\[ R_c = \frac{\rho_c}{A} \]

The 1-D Model above does not account for the current flowing in the overlap region \( (\delta) \) of the underlying layer. See Figure 59. If \( \delta > 0 \), in this case the so-called 2-D Model should be applied. The measured \( R_k \) is then a sum of the \( R_c \) and the resistance due to the current flow around the contact in the overlap region \( (R_{\text{geom}}) \) [111, 112].

\[ R_k = R_c + R_{\text{geom}} \]

\[ R_k = \frac{\rho_c}{A} + \frac{4R_{sh}\delta^2}{3W_xW_y} \left[ 1 + \frac{\delta}{2(W_x - \delta)} \right] \]

\( R_{sh} \) is the sheet resistance of the underlying layer. The contact geometry parameters \( W_x, W_y \) and \( \delta \) are all defined in Figure 59.
If the I-V characteristic of the device is linear and symmetric, the contact is ohmic. If the I-V characteristic is non-linear and asymmetric, the contact is a blocking or Schottky contact.

Figure 60 shows the I-V characteristics for the CBKR devices for one of the wafers under investigation. a) after sintering for 3 min at 470 °C and b) after sintering for 6 min at 470 °C. CBKR 1 and 2 represent two of the devices located on two chips on the top of the wafer, CBKR 3 to 5 represent three of the devices on three chips in the centre of the wafer and the remaining CBKR 6 and 7 were taken from two chips on the bottom of the wafer.

The figure shows that ohmic contacts were achieved for the devices located on top of wafer after being sintered for 3 min at 470 °C. This is shown from the linearity of the I-V characteristic for CBKR 1 and 2. The 3 min duration for sintering obviously was not sufficient for all the devices. After sintering for 6 min at 470 °C, all the devices on the wafer obtained an ohmic contact as shown in Figure 60 b).

![I-V Characteristics for Kelvin contact resistor devices after sintering for 3 min at 470 °C](image1)

![I-V Characteristics for Kelvin contact resistor devices after sintering for 6 min at 470 °C](image2)

Figure 60: I-V characteristics for the Kelvin contact resistor devices for one of the wafers under investigation a) after sintering for 3 min at 470 °C and b) after sintering for 6 min at 470 °C.
Figure 61 shows one of the pin-diode detectors with 2 guard-rings. The guard-rings and the n+ layer as shown are covered with a metal contact while the active-area is covered with 10 nm oxide. The pin-diode detector is sitting on the FET. This is a picture of the final product, designed, modelled and manufactured for this project.

Figure 61: One of the manufactured pin-diode detectors connected to a FET.
6 Measurement Analysis

Chapter 6 describes the electrical measurements performed on the detectors. The results are then analysed and the best device configuration is determined.

The pin-diode detectors differ in structure (See chapter 4) and in the processing technologies used to manufacture them.

Table 6 Describes the structure of the nine pin-diode detectors (referenced as devices 1 to 9). In Table 6 shallow implantation under the anode’s contact means that this region has been implanted with 2 keV \( B^+ \times 10^{12} \text{ cm}^{-2} \), tilt=7° and rotation=22° and the deep implantation means that this region has been implanted with an additional 10 keV \( B^+ \times 10^{14} \text{ cm}^{-2} \), tilt=7° and rotation=22°.

<table>
<thead>
<tr>
<th>Device</th>
<th>Number of guard-rings</th>
<th>Type of Guard-ring</th>
<th>( n^+ ) layer</th>
<th>Imp. under the anode’s contact</th>
<th>Active-area’s surface</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device 1</td>
<td>3</td>
<td>Floating</td>
<td>Yes</td>
<td>Deep</td>
<td>Metallised</td>
</tr>
<tr>
<td>Device 2</td>
<td>3</td>
<td>Contacted</td>
<td>Yes</td>
<td>Shallow</td>
<td>Metallised</td>
</tr>
<tr>
<td>Device 3</td>
<td>3</td>
<td>Contacted</td>
<td>Yes</td>
<td>Deep</td>
<td>Metallised</td>
</tr>
<tr>
<td>Device 4</td>
<td>3</td>
<td>Contacted</td>
<td>No</td>
<td>Deep</td>
<td>Metallised</td>
</tr>
<tr>
<td>Device 5</td>
<td>2</td>
<td>Contacted</td>
<td>Yes</td>
<td>Shallow</td>
<td>Oxidised</td>
</tr>
<tr>
<td>Device 6</td>
<td>2</td>
<td>Contacted</td>
<td>Yes</td>
<td>Deep</td>
<td>Oxidised</td>
</tr>
<tr>
<td>Device 7</td>
<td>2</td>
<td>Floating</td>
<td>Yes</td>
<td>Deep</td>
<td>Metallised</td>
</tr>
<tr>
<td>Device 8</td>
<td>2</td>
<td>Contacted</td>
<td>Yes</td>
<td>Shallow</td>
<td>Metallised</td>
</tr>
<tr>
<td>Device 9</td>
<td>2</td>
<td>Contacted</td>
<td>Yes</td>
<td>Deep</td>
<td>Metallised</td>
</tr>
</tbody>
</table>

Table 6: Structural descriptions of the nine different pin-diode detectors.

As part of this project, we manufactured the detectors in two iterations.

The first processing run put all the theory gained using the Silvaco simulation programme into practice. We processed and analysed 4 wafers:

- On the first wafer, we implanted the entrance window (active-area) of the devices with 2 keV \( BF_2^+ \times 10^{12} \), tilt=7° and rotation=22°.
• On the second wafer, the entrance window was implanted with 2 keV 

\[ BF^+_2 \times 10^{12} \text{, tilt}=7^\circ \text{ and rotation}=22^\circ \text{ through a 10 nm oxide} \]

• The third wafer had its entrance windows implanted with 2 keV \( B^+ \times 10^{13} \), 

\[ \text{tilt}=7^\circ \text{ and rotation}=22^\circ. \]

• On the fourth wafer, the entrance window was implanted with 2 keV 

\[ B^+ \times 10^{13} \text{, tilt}=7^\circ \text{ and rotation}=22^\circ \text{ through a 10 nm oxide.} \]

We analysed the results of the first run and identified a number of areas where there was some flexibility in the manufacturing process.

This led to the second processing run, with only 2 keV \( B^+ \times 10^{13} \), tilt=7° and rotation=22° were used to implant the entrance window of the devices. Two wafers were processed and analysed as part of the second run:

1) For wafer 1, the entrance window was annealed for 5s at 950 °C

2) For wafer 2, the entrance window was annealed for 10s at 850 °C.

Each wafer was split into 2 halves, the region under the contact on the active-area being implanted with a different quantity of \( B^+ \) in each half.

Due to the fact that the wafers were split into 2 sides for implantation, there were a total of 4 different batches of devices to analyse.
6.1 Measurements Schematics

To measure the I-V characteristics of the devices in both processing runs, two measurement techniques were utilised:

1) Reverse bias of each device without biasing the guard-rings

2) Reverse bias of each device with biasing the innermost guard-ring

Figure 62 shows the measurement schematic for a typical device when the device is reverse biased without biasing any guard-ring.

$I_{IG}$ is where the Pico-amp meter is connected, which reads the leakage current out from the substrate. $V_{IG}$ is the applied voltage on the active-area and the substrate.

Figure 62: Measurement schematic without biasing the guard-ring.
Figure 63 shows the measurement schematic for a typical device when the active-area and the innermost guard-ring are reverse biased.

$I_{1G}$ is the leakage current, which is generated out from the active-area.

$I_{2G}$ is the leakage current, which is generated out from the guard-ring.

$I_{1G} + I_{2G}$ is where the Pico-amp meter is connected, which reads the total leakage current generated from the active-area and the guard-ring.

$V_{1G}$ and $V_{2G}$ are the applied voltages on the active-area and the innermost guard-ring respectively.

Figure 63: Measurement schematic with biasing the guard-ring.
6.2 First Process Run Analysis

For this processing run, we will only show the active-area leakage current of the detectors with biasing the innermost guard-ring (I_{1G}). The chapter describing the second processing run will show more detailed leakage current results.

- On the first wafer, we implanted the entrance window (active-area) of the devices with 2 keV $BF_2^+ \times 10^{12}$, tilt=7° and rotation=22°.

- On the second wafer, the entrance window was implanted with 2 keV $BF_2^+ \times 10^{12}$, tilt=7° and rotation=22° through a 10 nm oxide.

- The third wafer had its entrance windows implanted with 2 keV $B^+ \times 10^{13}$, tilt=7° and rotation=22°.

- On the fourth wafer, the entrance window was implanted with 2 keV $B^+ \times 10^{13}$, tilt=7° and rotation=22° through a 10 nm oxide.

6.2.1 Wafer 1 – BF$_2^+$ Used for Implantation

Figure 64 shows the leakage current with biasing the innermost guard-ring (I_{1G}), for all devices (1 to 9) on the wafer with $BF_2^+$ implanted in the entrance window. The implantation dose was $5 \times 10^{12}$ cm$^2$ with an energy of 2 keV, tilt=7° and rotation=22°.

Pin-diode detectors 5 to 9 with 2 guard-rings exhibit less leakage current than the detectors 1 to 4 with 3 guard-rings. Pin-diode detectors 2 and 4 yield higher leakage current than all the other detectors.
6.2.2 Wafer 2 – BF$^{+2}$ Used for Implantation through a 10nm Oxide

Figure 65 shows the leakage current with biasing the innermost guard-ring ($I_{1G}$), for all detectors (1 to 9) on the wafer with $BF^{+2}$ implanted through a 10 nm oxide in the entrance window. The implantation dose was $5 \times 10^{12}$ cm$^{-2}$ with an energy of 2 keV, tilt=7° and rotation=22°.

Pin-diode detectors 5 to 9 with 2 guard-rings have lower leakage current than detectors 1 to 4 with 3 guard-rings. Pin-diodes 2 and 4 yield the highest leakage current.
6.2.3 Wafer 3 – B⁺ Used for Implantation

Figure 66 shows the leakage current with biasing the innermost guard-ring ($I_{1G}$) for detectors 1 to 9 on the wafer with $B^+$ implanted in the entrance window. The implantation dose was $3 \times 10^{13}$ cm⁻² with an energy of 2 keV, tilt=7° and rotation=22°.

All the pin-diode detectors displayed almost the same leakage current, regardless of the number of guard-rings.
6.2.4 Wafer 4 – B⁺ Used for Implantation through a 10nm Oxide

Figure 67 shows the leakage current with biasing the innermost guard-ring ($I_{1G}$), for all detectors (1 to 9) on the wafer with $B^+$ implanted through a 10 nm oxide in the entrance window. The implantation dose was $3 \times 10^{13}$ cm⁻² with an energy of 2 keV, tilt=7° and rotation=22°.

All the pin-diodes showed almost the same leakage current regardless of the number of guard-rings except for device 4 (with 3 guard-rings).

Moreover, devices 2 and 3 (both with 3 guard-rings) have a breakdown around 38 V and 30 V respectively.
Figure 67: The leakage current with biasing the guard-ring for all the detectors on the wafer with B+ implanted through a 10 nm oxide in the entrance window.
6.2.5 Analysis of the Results

Ion implantation in silicon results in the creation of large concentrations of interstitials and vacancies which, during annealing, tend to recombine and eventually condense to form defects of various types. Among them are the “extended” defects which can be defined as those defects that can be imaged by Transmission Electron Microscopy. The interactions between these defects and the dopant atoms are at the origin of the TED phenomenon. There has been much debate in the literature concerning the formation mechanism and the atomic structure of defects that are introduced by various processes such as oxidation and ion implantation. The smallest defects that the TEM can resolve are already 2 nm-long {113} defects containing at least 40 atoms. Once these {113}s are formed, they grow in size and reduce their density. While they can dissolve if a highly recombining surface is close enough to them, they can transform into dislocation loops if they grow up to a certain size. The dislocation loops are the most common and well known type of End-Of-Range (EOR) defects. These loops are interstitial in nature [58].

During the first batch production two of the wafers were implanted with \( BF_2^+ \). The objective was to obtain a shallow junction [113-117]. However interstitial cluster, vacancy cluster, and/or coupled with other defects increase the total \( B^+ \) diffusion during the annealing process, which makes maintaining a shallow junction difficult [118].

It has been reported that \( BF_2^+ \) implanted Si includes the pileup of fluorine in the \( B^+ \) peak and reduces the \( B^+ \) concentration in this region [119], this consequently increases the leakage current. See Figure 28. It has been shown that Fluorine implants can increase the leakage current of the device [120, 121].

Another reason behind the high leakage current in the Fluorine implanted wafers can be that the etching rate changes with the presence of fluorine in the Si. The etching of the contact area just before metal deposition is important to remove the oxide layer. However, over-etching of the contact area results in loss of \( B^+ \) dopants [104] and increasing the leakage current.
Two of the wafers (wafer 2 and 4) were implanted through a thin layer of oxide. The purpose again was to achieve a shallow junction. The oxide layer was kept on the wafers throughout the processing. This oxide layer is essential and acts as a passivation layer. At the end of the production just before depositing the contacts we could have removed this layer and replaced it with a fresh layer of oxide but putting the wafers though an oxidation process after the $B^+$ implantations would diffuse the $B^+$ even further and consequently increase the leakage current. For this reason this layer of oxide was not removed and probably this damaged oxide layer could be the reason behind the increased leakage current in these wafers compared to the bare implanted wafers.

Oxide damage by ion implantation is a well-known effect. Point defects in the oxide layer provide charge trapping in the material and affect the long-term performance and the leakage current of the devices.

Devices with 2 guard-rings exhibit lower leakage current than the devices with 3 guard-rings, as shown by the I-V characteristics. This can be due to the way the contacts were placed on the devices. Chapter 6.5 analyses this concept in more detail.

After analysing the results of the first processing run, we decided to implant the entrance window of the wafers for the 2nd run with $B^+$ only, since it gave the best results with lower leakage current.
6.3 Second Processing Run Analysis

Two wafers were processed during the second production run.

For wafer 1 the entrance window (active-area) was annealed for 5s at 950 °C. For wafer 2 the entrance window (active-area) was annealed for 10s at 850 °C.

For both wafers, the surface was split into 2 halves. On one half, the region under the contact on the active-area (anode) was implanted with 2 keV $B^+$ $3 \times 10^{13}$ cm$^{-2}$, tilt=7° and rotation=22°, while on the other half, the anode was implanted with an additional 10 keV $B^+$ $2 \times 10^{14}$ cm$^{-2}$, tilt=7° and rotation=22°.

Due to the fact that for implantation the wafers' surfaces were split into 2 sides, there were a total of 4 different batches of devices to analyse:

Batch 1 – Section of Wafer 1 (annealed for 5s at 950 °C), anode implanted with 2 keV $B^+$ $3 \times 10^{13}$ cm$^{-2}$, tilt=7° and rotation=22°.

Batch 2 - Section of Wafer 1 (annealed for 5s at 950 °C), anode implanted with an additional 10 keV $B^+$ $2 \times 10^{14}$ cm$^{-2}$, tilt=7° and rotation=22°.

Batch 3 – Section of Wafer 2 (annealed for 10s at 850 °C), anode implanted with 2 keV $B^+$ $3 \times 10^{13}$ cm$^{-2}$, tilt=7° and rotation=22°.

Batch 4 – Section of Wafer 2 (annealed for 10s at 850 °C), anode implanted with an additional 10 keV $B^+$ $2 \times 10^{14}$ cm$^{-2}$, tilt=7° and rotation=22°.

For both wafers the contacts were annealed for 6 minutes at 470 °C.

All the pin-diodes were analysed on each of the 4 wafer batches mentioned above.

This chapter will describe the I-V characteristics of the 4 analysed batches for the 9 devices and the little pin-diode detectors with an active-area of 1mm$^2$.

Each device in a batch is compared with the same device in the other three batches. The results are then analysed in chapter 6.5.
6.3.1 Batch 1 – Section of Wafer 1 Implanted with 2 keV B⁺ 3x10¹³ cm⁻² Annealed for 5s at 950 °C

The following results are for the half of wafer 1 where the region under the contact on the active-area was implanted with 2 keV B⁺ 3x10¹³ cm⁻², tilt=7° and rotation=22°.

Figure 68 shows the I-V characteristics when the detectors are reverse biased without biasing any guard-ring. The measurement schematic is according to Figure 62.

Figure 68 also shows that pin-diodes 1 to 4 (with 3 guard-rings) yield higher leakage current than devices with 2 guard-rings.

![Image of I-V characteristics](image-url)

**Figure 68**: The leakage current without biasing any guard-ring for the section of wafer 1 where the region under the contact on the active-area was implanted with 2 keV B⁺ 3X10¹³ cm⁻² annealed for 5s at 950 °C.

Figure 69 shows the I-V characteristics when the detectors are reverse biased with biasing any guard-ring. The measurement schematic is according to Figure 63.
Again all the devices with 3 guard-rings exhibit higher leakage current than the devices with 2 guard-rings. Also by biasing the innermost guard-ring, the leakage current on all the devices with 2 guard-rings has been suppressed to 10 μA and stabilised around this value.

![Image: The leakage current with biasing the innermost guard-ring for the section of wafer 1 where the region under the contact on the active-area was implanted with 2 keV B⁺ 3x10¹³ cm⁻² annealed for 5s at 950 °C.](image)

Figure 69: The leakage current with biasing the innermost guard-ring for the section of wafer 1 where the region under the contact on the active-area was implanted with 2 keV B⁺ 3x10¹³ cm⁻² annealed for 5s at 950 °C.

6.3.2 Batch 2 - Section of Wafer 1 Implanted with an Additional 10 keV B⁺ 2x10¹⁴ cm⁻² Annealed for 5s at 950 °C

The following results are for the half of wafer 1 where the region under the contact on the active-area was implanted with an additional 10 keV B⁺ 2x10¹⁴ cm⁻², tilt=7° and rotation=22°.

Figure 70 shows the I-V characteristics when the detectors are reverse biased without biasing any guard-ring.
Similar to the Batch 1 electrical measurements, devices with 3 guard-rings yield a higher leakage current than devices with 2 guard-rings.

Figure 70: The leakage current without biasing any guard-ring for the section of wafer 1 where the region under the contact on the active-area was implanted with 10 keV B⁺ 2X10¹⁴ cm⁻² annealed for 5s at 950 °C.

Figure 71 shows the leakage current when the active-area and the innermost guard-ring are reverse biased.

By biasing the innermost guard-ring, the leakage current has been reduced for all the devices with 2 guard-rings and devices 1 and 4 with 3 guard-rings.
6.3.3 Batch 3 – Section of Wafer 2 Implanted with 2 keV $B^+$ $3 \times 10^{13}$ cm$^{-2}$ Annealed for 10s at 850 °C

The following results are for the half of wafer 2 where the region under the contact on the active-area was implanted with 2 keV $B^+$ $3 \times 10^{13}$ cm$^{-2}$, tilt=7° and rotation=22°.

Figure 72 shows the I-V characteristics when the devices are reverse biased without biasing any guard-ring.

Detectors 1 to 4 (with 3 guard-rings) that displayed a high leakage current in batches 1 and 2 also yielded high leakage current in batch 3. Detectors 5 to 9 (with 2 guard-rings) exhibit lower leakage current than the corresponding devices in batches 1 and 2.
Figure 72: The leakage current without biasing any guard-ring for the section of wafer 2 where the region under the contact on the active-area was implanted with 2 keV B⁺ 3X10¹³ cm⁻² annealed for 10s at 850 °C.

Figure 73 shows the leakage current when the active-area and the innermost guard-ring are reverse biased.

Figure 73 shows that the leakage current for the devices with 3 guard-rings has been reduced to the same level as for devices with 2 guard-rings.

However, devices 2 and 4 (with 3 guard-rings) have a breakdown around 30 V.
Figure 73: The leakage current with biasing any guard-ring for the section of wafer 2 where the region under the contact on the active-area was implanted with 2 keV B⁺ 3×10¹³ cm⁻² annealed for 10s at 850 °C.

6.3.4 Batch 4 – Section of Wafer 2 Implanted with an Additional 10 keV B⁺ 2x10¹⁴ cm⁻² Annealed for 10s at 850 °C

The following results are for the half of wafer 2 where the region under the contact on the active-area was implanted with an additional 10 keV B⁺ 2×10¹⁴ cm⁻², tilt=7° and rotation=22°.

Figure 74 shows the I-V characteristics when the devices are reverse biased without biasing any guard-ring. Similarly to the three previous batches, devices 1 to 4 with 3 guard-rings exhibit higher leakage current than devices 5 to 9 with 2 guard-rings.
Figure 74: The leakage current without biasing any guard-ring for the section of wafer 2 where the region under the contact on the active-area was implanted with 10 keV B$^+$ 2X10$^{14}$ cm$^{-2}$ annealed for 10s at 850 °C.

Figure 75 shows the leakage current when the active-area and the innermost guard-ring are reverse biased.

The leakage current on devices 1 and 3 has been reduced by biasing the inner guard-ring.

Devices 2 and 4 break down, as was the case for the same devices in batch 3. The breakdown, however, occurred earlier, at around 25 V.
Figure 75: The leakage current with biasing any guard-ring for the section of wafer 2 where the region under the contact on the active-area was implanted with 10 keV B⁺ 2×10¹⁴ cm⁻² annealed for 10s at 850 °C.

6.3.5 Batches 1-4 - 1mm² Pin-diode Detectors with 2 Guard-rings

All of the 1mm² pin-diode detectors with 2 guard-rings had very similar characteristics; likewise, all of the 1mm² pin-diode detectors with 3 guard-rings showed almost the same result. For this reason, this thesis will only describe the characteristics of one instance of a 1mm² pin-diode detector with 2 guard-rings and one instance of a 1mm² pin-diode detector with 3 guard-rings.

The 1mm² pin-diode detector with 2 guard-rings below, was taken from batch 4, where the contact region on the active-area was implanted with an additional 10 keV B⁺ 2×10¹⁴ cm⁻², tilt=7° and rotation=22°.

Figure 76 shows the leakage current without biasing the guard-ring for the 1mm² pin-diode detector with 2 guard-rings.
Figure 76: The leakage current without biasing the guard-ring for the 1mm² pin-diode detector with 2 guard-rings.

Figure 77 shows the leakage current for the 1mm² pin-diode detector with 2 guard-rings with biasing the innermost guard-ring.

The leakage current has reduced by 2 orders of magnitude by biasing the guard-ring. This means that the unbiased guard-rings contribute to the leakage-current by 2 order of magnitudes.
6.3.6 Batches 1-4 - 1mm² Pin-diode Detectors with 3 Guard-rings

For the 1mm² pin-diode detector with 3 guard-rings, the detector below was taken from batch 2, where the contact region on the active-area was implanted with an additional 10 keV $B^+ \times 2 \times 10^{14}$ cm$^{-2}$, tilt=7° and rotation=22°.

Figure 76 shows the leakage current without biasing the guard-ring for the 1mm² pin-diode detector with 3 guard-rings.
Figure 78: The leakage current without biasing the guard-ring for the 1mm$^2$ pin-diode detector with 3 guard-rings.

Figure 79 shows the leakage current with biasing the inner guard-ring for the 1mm$^2$ pin-diode detector with 3 guard-rings.

As for the 1mm$^2$ pin-diode detector with 2 guard-rings, the leakage current reduces by 2 orders of magnitude when the inner guard-ring was biased. This indicates that the unbiased guard-rings' contribution to the leakage current has been eliminated by biasing the inner guard-ring.
6.4 Device Comparison

This section analyses the effect on the leakage current and breakdown voltage resulting from variations in the following parameters:

- The number of the guard-rings.
- Devices with floating guard-rings and devices with metal contacts on the guard-rings.
- Deep implantation under the active-area’s contacts.
- Devices with metal or oxide layer on the active-area.
- Devices with or without the n⁺ layer.
- Devices with different areas.
The reason behind the leakage currents and the breakdowns are explained in section 6.5.

6.4.1 Devices with a Different Number of Guard-rings

For this project, devices with 2 and 3 guard-rings were manufactured and examined. In this chapter, the number of the guard-rings is analysed and the best device configuration is determined.

Device 2 and device 8 have the same structure except for the number of the guard-rings. Device 2 has 3 guard-rings and device 8 has 2 guard-rings. The guard-rings are also covered with Al.

Figure 80 shows the comparison of leakage current without biasing any guard-ring for devices with 2 and 3 contacted guard-rings in the second processing run batches 1 to 4. It shows that pin-diodes with 3 guard-rings yield higher leakage current than pin-diodes with 2 guard-rings.
Comparison of leakage current without guard-ring bias for devices with 2 and 3 metallised guard-rings

Device 2=3 contacted guard-rings  Device 8=2 contacted guard-rings

15 20 25
Voltage (V)

Comparison of leakage current without guard-ring bias for devices with 2 and 3 metallised guard-rings

Device 2=3 contacted guard-rings  Device 8=2 contacted guard-rings

1.0E-02

1.0E-03

1.0E-04

1.0E-05

0.1

10

1.0

1.0E-00

1.0E-01

1.0E-02

1.0E-03

Anode’s contact implantation 2kev B 3e13; annealed for 5s @ 950C

Anode’s contact implantation 10kev B 2e14; annealed for 5s @ 950C

Comparison of leakage current without guard-ring bias for devices with 2 and 3 metallised guard-rings

Device 2=3 contacted guard-rings  Device 8=2 contacted guard-rings

15 20 25
Voltage (V)

Comparison of leakage current without guard-ring bias for devices with 2 and 3 metallised guard-rings

Device 2=3 contacted guard-rings  Device 8=2 contacted guard-rings

1.0E-02

1.0E-03

1.0E-04

1.0E-05

0.1

10

1.0

1.0E-00

1.0E-01

1.0E-02

1.0E-03

Anode’s contact implantation 2kev B 3e13; annealed for 5s @ 950C

Anode’s contact implantation 10kev B 2e14; annealed for 5s @ 950C

Figure 80: Comparison of leakage current without biasing any guard-ring for device 2 with 3 guard-rings and device 8 with 2 guard-rings in batches 1 to 4.

Device 3 and Device 9 both have the same structure but device 3 has 2 guard-rings and device 9 has 2 guard-rings. These two devices have a deep implantation under the contact on their active-area, which distinguishes them from the other devices with 2 and 3 guard-rings e.g. device 2 and device 8 above.
Figure 81 shows the comparison of leakage current without biasing any guard-ring for devices with 2 and 3 guard-rings and with a deep implantation under anode's contacts in the second processing run batches 1 to 4. It shows that pin-diodes with 3 guard-rings yield higher leakage current than pin-diodes with 2 guard-rings.

Figure 81: Comparison of leakage current without biasing any guard-ring for device 3 with 3 guard-rings and device 9 with 2 guard-rings in batches 1 to 4.
6.4.2 Devices with a Different Number of Floating Guard-rings

Devices 1 and 7 have the same structure with floating guard-rings but the difference is that device 1 has 3 guard-rings and device 7 has 2 guard-rings.

Figure 82 shows the comparison of leakage current without biasing any guard-ring for devices with 2 and 3 floating guard-rings in the second processing run batches 1 to 4. Pin-diodes with 3 floating guard-rings yield higher leakage current than pin-diodes with 2 floating guard-rings.
Comparison of leakage current without guard-ring bias for devices with 2 and 3 floating guard-rings

6.4.3 Comparing Devices with Floating Guard-rings and Devices with Metal Contacts on the Guard-rings

Device 1 and device 3 both have 3 guard-rings and the same structure but the guard-rings in device 1 are floating and in device 3 they have a layer of metal contact on top.

Figure 83 shows the comparison of leakage current without biasing any guard-ring for devices with 3 floating and contacted guard-rings in the second processing run batches 1 to 4. Pin-diodes with 3 floating guard-rings exhibit lower leakage current than pin-diodes with 3 Al covered guard-rings.
Comparison of leakage current without guard-ring bias for devices with metallised and floating guard-rings

Device 1 = 3 floating guard-rings

Device 3 = 3 contacted guard-rings

\[ 1.0 \times 10^{-11} \]

\[ 1.0 \times 10^{-12} \]

Voltage (V)

Figure 83: Comparison of leakage current without biasing any guard-ring for device 1 with 3 floating guard-rings and device 3 with 3 metal contacted guard-rings in batch 1 to batch 4.

Device 7 and device 9 have both 2 guard-rings and the same structure but the guard-rings in device 7 are floating and in device 9 they have metal contacts on top.
Figure 84 shows the comparison of leakage current without biasing any guard-ring for devices with 2 floating and contacted guard-rings in the second processing run batches 1 to 4.

Figure 84: Comparison of leakage current without biasing any guard-ring for device 7 with 2 floating guard-rings and device 9 with 2 metal contacted guard-rings in batch 1 to batch 4.
6.4.4 Comparing Devices with an Oxide Layer or Metal Contact on the Active-area

Device 5 and device 8 are similar, both with 2 guard-rings and a shallow implantation under the anode's contact. The only difference is that device 5 has a thin layer (10 nm) of oxide on the active-area while device 8's active-area is covered with AlSi1%. Figure 85 shows the comparison of leakage current without biasing any guard-ring for devices with metallised (device 8) and oxidised (device 5) active-area in the second processing run batches 1 to 4.

Devices with oxidised active-area yield lower leakage current than devices with metallised active-area.
Device 6 and device 9 are similar, both with 2 guard-rings and deep implantation under the anode’s contact. This deep implantation region distinguishes these devices from device 5 and 8 mentioned above. The only difference between device 6 and 9 is that device 6 has an oxide layer (10 nm) on the active-area while device 9’s active-area is covered with a thin layer of AlSi1%.

Figure 86 shows the comparison of leakage current without biasing any guard-ring for devices with oxidised and meallised active-area in the second processing run batches 1 to 4. pin-diodes with an oxide layer on the active-area yield a lower leakage current than pin-diodes with an Al layer on the active-area.
Comparison of leakage current without guard-ring bias for devices with metallised and oxidised active-area

- Device 6: oxidised active-area
- Device 9: metallised active-area

Anode's contact implantation 2e16 B 3e13; annealed for 5s @ 950C

Batch 1

Batch 2

Batch 3

Batch 4

Figure 86: Comparison of leakage current without biasing any guard-ring for device 6 with an oxide layer on the anode and device 9 with a metal layer on the anode in batch 1 to batch 4.
6.4.5 Analysing the Effect of Deep and Shallow Implantation under the Active-area’s Contact

Device 2 and device 3 have the same structure and number of the guard-rings. The only difference between their structures is that device 2 has a shallow implantation under the anode’s contact (2 keV $B^+$, $3 \times 10^{13}$ cm$^{-2}$, tilt=7° and rotation=22°) while device 3 has a deep implantation (10 keV $B^+$, $2 \times 10^{14}$ cm$^{-2}$, tilt=7° and rotation=22°) in this region.

Figure 87 shows the comparison between device 2 and device 3 for the leakage current in second processing run batches 3 and 4. Only these two batches were implanted with 10 keV deep implantation. Pin-diodes with 3 guard-rings and a deep implantation under the active-area’s contact exhibit lower leakage current than pin-diodes with 3 guard-rings but shallower implantation under the active-area’s contact.

![Graphs showing comparison of leakage current](image)

Figure 87: Comparison of leakage current without biasing any guard-ring for device 2 with 2 keV $B^+$ implantation under the anode’s contact and device 3 with 10 keV $B^+$ implantation, in batch 3 and 4.
Device 5 and device 6 have the same structure; both have 2 guard-rings and have the active-area covered with an oxide layer. The only difference between their structures is that device 5 has been implanted with a shallow implantation (2 keV $B^+$, $3 \times 10^{13}$ cm$^{-2}$, tilt=7° and rotation=22°) under the anode's contact while this region has been implanted with an additional 10 keV $B^+$, $2 \times 10^{14}$ cm$^{-2}$, tilt=7° and rotation=22° in device 6.

Figure 88 shows the leakage current for device 6 and device 5 in second processing run batches 3 and 4. Pin-diodes with 2 guard-rings and a deep implantation under the active-area's contact exhibit lower leakage current than pin-diodes with 2 guard-rings but shallower implantation under the anode's contact.

![Comparison of leakage current without guard-ring bias for devices with a deep and a shallow implantation under the active-area's contact](image)

Figure 88: Comparison of leakage current without biasing any guard-ring for device 5, with 2 keV $B^+$ implantation under the anode's contact and device 6 with 10 keV $B^+$ implantation in batch 3 and 4.

Device 8 and device 9 have both 2 guard-rings and the same structure with a metallised anode except for the region under the anode's contact. Device 8 has been implanted with 2 keV $B^+$, $3 \times 10^{13}$ cm$^{-2}$, tilt=7° and rotation=22° under the anode's
contact while this region has been implanted with an additional 10 keV $B^+$, $2 \times 10^{14} \text{ cm}^{-2}$, tilt=7$^\circ$ and rotation=22$^\circ$ in device 9.

Figure 89 shows the leakage current for device 8 and 9 in second processing run batches 3 and 4. Pin-diodes with 2 guard-rings and a metallised anode but a deep implantation under the active-area's contact exhibit lower leakage current than pin-
diodes with the same structure but shallower implantation in this region.

![Comparison of leakage current without guard-ring bias for devices with a deep and a shallow implantation under the active-area's contact](image)

Figure 89: Comparison of leakage current without biasing any guard-ring for device 8 with 2 keV $B^+$ implantation under the anode's contact and device 9 with 10 keV $B^+$ implantation in batch 3 and 4.

### 6.4.6 Analysing the Effect of the n$^+$ Layer

Device 3 and device 4 are similar, both have 3 guard-rings but device 4 doesn't have an n$^+$ layer at the edge.

Figure 90 shows the comparison of leakage current without biasing any guard-ring for device 3 with an n$^+$ layer and device 4 without an n$^+$ layer in the second processing run batches 1 to 4.
Device 3 provides lower leakage current than device 4 without an n+ layer. Pin-diodes with an n+ layer at the edge of the device yield lower leakage current than pin-diodes without an n+ layer.

Figure 90: Comparison of leakage current without biasing any guard-ring for device 3 with an n+ layer and device 4 without an n+ layer in batch 1 to batch 4.
6.4.7 Analysing the Area's Impact on the Leakage Current

Figure 91 compares the leakage current with biasing the inner guard-ring for devices for two devices with the same structure but one with an active-area of 1 mm$^2$ and the other with an active-area of 10 mm$^2$. The figure is split into two parts:

Part a) references two devices with 2 guard-rings

Part b) references two devices with 3 guard-rings.

The result showed that devices with an active-area of 1 mm$^2$ have about 1 order of magnitude lower leakage current than devices with an active-area of 10 mm$^2$.

Figure 91: Comparison of leakage current with biasing the inner guard-ring for devices with an active-area of 1 mm$^2$ and 10 mm$^2$ and a) 2 guard-rings b) 3 guard-rings.
6.5 Analysis of the Results

The I-V characteristics above showed that devices with 2 guard-rings have lower leakage current than devices with the same structure but 3 guard-rings. The comparison between the number of guard-rings in devices with floating guard-rings also showed the same result.

To explain the behaviour of I-V characteristics and to understand why the leakage current is higher in the devices with 3 guard-rings compared to 2 guard-rings, an explanation is needed of where the leakage current originates from and how the number of the guard-rings affects this leakage current.

Figure 92 shows the leakage current components generated in a p-i-n junction device. The total leakage current $I_R$ is a sum of the bulk leakage current component $I_{RB}$ generated in the bulk depletion layer and the surface leakage current component $I_{RS}$ at the interface [122].

![Diagram of leakage current components](image)

Figure 92: Leakage current generated from a pin-diode [123].

The surface leakage current is dominated by the bulk component at low applied reverse voltage but soon after it becomes dominant. High level of $I_R$ in p-i-n junction devices is due to the $I_{RS}$ current [123-126].

To cast more light on the surface leakage current, this phenomenon is explained in the figure below.
Figure 93 shows a schematic view of the longitudinal cross-section of a pin-diode [62].

Most of the surface leakage current originates in the vicinity of the i-p boundary, in the region labeled “breakdown region”. En is the internal electric field normal to the surface.

Figure 94 illustrates the use of the guard-rings. The insulator which is the oxide is segmented into two parts, one part separating the conducting guard-ring from the negative electrode and the other part separating it from the positive electrode. Most of the voltage drop occurs across the outer segment in which the resulting leakage current does not pass through the measuring instrument. The voltage drop across the inner segment is only the voltage difference across the Amp-meter terminals and can be very small. Therefore the component of leakage current which is added to the signal is greatly reduced compared with the case without the guard-ring [18].
having the innermost guard-ring biased at the same potential as the active-area, one can separate the leakage current that goes through the guard-ring, from the bulk leakage current (active-area’s leakage current).

![Diagram of cylindrical ion chamber with guard-rings](image)

**Figure 94:** A cross section view of one end of cylindrical ion chamber that utilizes guard-ring construction [18].

Guard-ring structures have been widely used in both photo and radiation detectors. As discussed in chapter 4.8 (Guard-rings design), the role of the guard-ring is to relax the electrical field at the periphery of the p-n junction (the edge of the anode) and to prevent the breakdown from occurring early. When placing the guard-rings, the electric field actually divides between them [128-131].

Many guard-rings are favourable to achieving a high breakdown voltage, because the large number of divisions of the potential along the surface by many guard-rings will reduce the maximum electric field at the edge of the anode but an optimal number of guard-rings exist. This depends on the distance available for the guard-rings, between the active-area and the n⁺ layer.

The breakdown voltage is sensitive to the distance between the innermost guard-ring and the anode, the outermost guard-ring and the n⁺ layer, the distance between the guard-rings, their widths and also junction curvature.

Devices with 2 guard-rings exhibit lower leakage current than the devices with 3 guard-rings, as shown in the I-V characteristics. The simulation results we produced using Silvaco show that both devices with 2 and 3 guard-rings generate the same leakage current but the breakdown voltage for the devices with 3 guard-rings is higher than the devices with 2 guard-rings (see chapter 4.8).
The discrepancy is a result of the simplified way in which the Silvaco Atlas tool processes devices. Atlas takes a 2-dimensional cross-section of the device that does not take into account less simple 3-dimensional contact shapes.

Placing the contacts of 3 guard-rings on a physical device in the manner that Atlas used for its simulation (each guard-ring having a small width and with a very short distance between the guard-rings) would have made biasing the guard-rings very difficult.

For this reason, the placement of contacts for devices with 3 guard-rings was more complex than the placement of contacts for devices with 2 guard-rings. See Figure 95.

The way in which the contacts are placed on devices with 3 guard-rings leads to a large and complex extension of the lateral depletion region along the surface and causes a large surface generation current and hence a higher leakage current [132], explaining the results we observed with the manufactured devices.

Figure 95 shows the layouts of the contacts on the guard-rings for devices with 2 and 3 guard-rings respectively using the Silvaco Expert tool. The contacts on the 3 guard-rings are extending out from the guard-rings inside a space dedicated to them in the n\textsuperscript{+} layer region.

Figure 95: An image of the contact mask on the guard-rings in Silvaco Expert Layout Editor a) A device with 2 guard-rings. b) A device with 3 guard-rings.
The breakdown voltage is sensitive to the distance between the innermost guard-ring and the anode, the outermost guard-ring and the n⁺ layer, the distance between the guard-rings, and also their widths. We have optimised these distances for the highest breakdown voltage by using Silvaco simulation tools and also curved the corner of the P⁺ implanted regions (the active-area and the guard-rings). Sharp corners make the electric field in the corners higher and cause an early breakdown. Previous research [133] has revealed no significant difference in the electrical performance of the devices with different curvature of the implanted corners, as long as a moderate curvature of the corners exists. Junction curvature strongly affects the breakdown voltage.

Figure 96 and Figure 97 show the curvature of device with 2 and 3 guard-rings respectively in Silvaco Expert Layout Editor and also the dimension of the n⁺ layer, the guard-rings and the distances between them.

![Figure 96: A detector’s mask with 2 guard-rings in Expert Layout Editor showing the corner of the guard-rings, the dimension of the n⁺ layer, guard rings and the distances between them.](image)
Since the breakdown field in the oxide is higher than avalanche breakdown field in the Si, metal overhangs were incorporated over the p⁺ strips to distribute the voltage-dropping across Si and oxide so as to increase breakdown voltage of the devices [134].

When the pin-diode is reverse biased, the depletion layer spreads vertically to the back side of the detector while it also spreads laterally to a distance comparable to the thickness of the wafer [135-137]. Biassing one or more guard-rings will constrain the lateral extension of the depletion layer and prevents the depletion layer from reaching the edge of the device [137, 138].

The main problem associated with the lateral spread of the depletion is the edge of the device, which is normally damaged by the cutting procedure. If the depletion layer
reaches the damaged edge, a large leakage of current arises. It has been observed that the leakage current can increase by a factor of 7 if the depletion layer reaches the edge of the device [136].

An n+ layer is included in the structures to prevent the spread of the lateral depletion [139-141].

Devices without an n+ layer exhibited higher leakage current than devices with this layer. This is due to the lateral depletion edge, which reaches the edge of the device and hence increases the leakage current [128].

Figure 98 shows the electrical field in a pin-diode detector without an n+ layer in a Silvaco simulation. The electrical field has been extended to the edge of the device compared to Figure 43, which shows the electrical field for the pin-diode detector with an n+ layer.

Figure 98: The electrical field in the pin-diode detector without an n+ layer.
The analysis showed that devices with floating guard-rings provide lower leakage current than devices with their guard-rings covered with metal.

Also devices with an oxide layer on the active-area yielded a lower leakage current than devices with metal covering the active-area.

The reason is that the oxide layer on the surface of the devices, acts as a passivation layer and reduces the generation of the surface leakage current, which thereafter decreases the total leakage current [142, 143].

The result of the measurement analysis showed that devices with an additional 10 keV $B^+$, $2 \times 10^{14}$ cm$^{-2}$ implanted under the active-area's contact result in lower leakage current than the devices implanted with 2 keV $B^+$, $3 \times 10^{13}$ cm$^{-2}$ under this region. This means that these devices have a lower contact resistance (See chapter 5 for more details about ohmic contacts).

Devices with an active-area of 1 mm$^2$ yield at least 1 order of magnitude lower leakage current than devices with an active-area of 10 mm$^2$. The larger the circumference, the larger the surface current is and the higher the total leakage current becomes. The large surface leakage current might derive from the increasing surface conductivity due to the conductive contamination [144]. These charged particles introduce generation-recombination centres and have influence not only in the surface depletion region, but also in the bulk depletion region. The presence of the generation–recombination centres causes significant reduction of the charge carrier life-time [127] and hence increases the leakage current.

The result of the device design using Silvaco simulation packages showed that we should be able to obtain a leakage current of 5 nA (see chapter 4). The lowest observed leakage current on the manufactured devices was about 30 nA (device 6 on wafer 2 in the second processing run), which is less than one order of magnitude higher than the simulation. The difference can be explained in terms of Silvaco's lack of support for changes in the carrier life-time during the different stages of processing of the wafer in a laboratory. No simulation programme will be able to estimate the change in the carrier life-time since each laboratory is unique in terms of contamination level, variety of equipment, number of users and also the same device
can be manufactured and processed differently. However the carrier life-time on one of the wafers was measured to investigate how the processing has affected the carrier life-time on the device and consequently the leakage current.

The measurement of the carrier life-time is normally based on the recombination dynamics of excess carriers which are normally generated optically.

There are different techniques to measure the carrier life-time and they are classified in terms of the time during which the devices are exposed to light [145].

Three methods are normally used to measure the carrier life-time.

1) The first regime involves a sharp pulse of illumination that is rapidly tuned off and a subsequent determination of the excess carrier density without illumination. This is the traditional transient technique, used especially to measure high carrier life-time.

2) the second regime is the steady-state illumination, which is of minor importance due to the problem that the samples will quickly suffer from heating and a changing of carrier life-time.

3) Such effects are avoided in the third regime, where the illumination intensity is slowly reduced to zero over several milliseconds. The decay will be long enough to ensure that the sample remains in steady state in terms of recombination processes. This is the basis of the quasi- steady-state (QSS) method first introduced by Sinton and Cuevas [146-152].

The effective life-time is obtained from:

\[ \tau_{\text{eff}}(\Delta n) = \frac{\Delta n(t)}{G(t) - \frac{d\Delta n(t)}{dt}} \]

Where \( \tau_{\text{eff}} \) is the effective carrier recombination life-time, \( \Delta n \) is the bulk excess carrier concentration and \( G \) is the photogeneration rate within the sample under test.

In the case of transient measurements, the pulse of light is required only to excite the carriers and is switched off during the actual measurement so that \( G(t) = 0 \). For the
QSS measurements, it is assumed that the light is varying very slowly so that $\frac{d(\Delta n)}{dt} = 0$ [153].

The carrier life-time measurement was carried out by a WCT-100 Si wafer life-time tester. The WCT-100 is used for the transient and the quasi-steady-state analysis and is capable to measure both high (several millisecond) and low (few microsecond) carrier life-times.

The results below were obtained using the WCT-100 in the quasi-steady-state mode.

A calibrated solar cell is used to simultaneously measure the illuminated light intensity.

Figure 99 shows the implied open circuit voltage versus the illumination intensity. This curve gives information comparable to the final I-V at each stage of a solar cell process. The implied open circuit voltage (Voc) at 1 sun is 560 mV and for 4 sun is 590 mV.

![Figure 99: Implied open circuit voltage versus the illumination intensity.](image)

Quasi-Steady-State life-time measurement relies on the number of carriers present when the sample is illuminated by a steady light. With the QSS method, the system
applies a slowly-varying light intensity and measures the photoconductance to map the carrier life-time.

Figure 100 shows the illuminated light intensity and the photoconductance (PC) signal generated in the wafer. The illuminated light is in the steady-state mode from 0.07 ms to 0.17 ms in the flat region for about 0.1 ms.

**Figure 100: The illuminated light intensity and the phoconductance signal generated in the wafer.**

In the QSS technique the effective life-time is determined at every carrier density, as shown in Figure 101. The minority carrier life-time is 148.7 μs at the minority carrier density of 5x10^{14} cm^3.
Figure 101: Minority carrier life-time versus carrier density.

After compensating for the change in the carrier life-time in the Silvaco simulation, we observed that the I-V characteristic is comparable to the manufactured device’s characteristic as shown in Figure 102. The leakage current of the manufactured device was surprisingly lower than the simulated device, but still in the same interval. The leakage current was 70 nA at a voltage of 40 V for the manufactured device while it was 80 nA for the simulated device. However for this project, the objective was to achieve as low a leakage current as 5 nA but the lowest leakage current recorded for the manufactured devices was one order of magnitude higher.
Figure 102: Comparison between I-V characteristic for the simulated and the best performing manufactured pin-diode detector.
7 Conclusion

The objective of this project was to design and manufacture a 5X5 mm$^2$ X-ray detector capable of measuring low X-ray energies (<10 keV). There was also a requirement to reduce the leakage current to about 0.5 nA/ cm$^2$ and obtain an efficiency of up to 100% without using a liquid nitrogen dewar to cool down the system. The elimination of the dewar facilitates the manufacture of portable detectors.

Different type of X-ray detectors were designed, manufactured and analysed in order to choose the most suitable detector configuration for industrial use.

The main advantage of using semiconductor detectors rather than other, e.g. gas-filled detectors, lies in the low amount of required ionisation energy. The energy of visible light photons of 2-4 eV is greater than the band gap energy of most semiconductors. Electron-hole pairs can therefore be easily produced by photon interactions, compared with about 20eV ionisation energy required to create an electron-hole pair in a typical gas-filled detector.

Also semiconductor detectors have much higher responsivity (the ratio of induced current to incident flux).

Gas-filled detectors are used for detecting high energy X-rays and $\gamma$-rays. STJ systems need cooling systems and they are more expensive. Semiconductor detectors such as Si(Li) and Ge(Li) are capable of detecting X-ray energies < 10 keV with lower resolution and they also need cooling systems to run. For this reason, manufacturing portable detectors using these devices is not feasible. Other semiconductor X-ray detectors such as SDDs and CCDs are portable and are used to measure low X-ray energies with high resolution but they are more expensive, especially if they come with integrated FETs. The only semiconductor X-ray detector which is relatively inexpensive, portable and able to detect low X-ray energies <10 keV with a high resolution is a pin-diode detector.

These were the main reasons behind our choice of X-ray detector using a pin-diode for this project.
Materials such as CdTe, CdZnTe, HgI₂ and PbI₂ with a high atomic number are used in detectors to detect γ-rays and hard X-rays. Other semiconductor materials such as Ge and GaAs are used for detecting high X-ray energies but do not provide high resolution for low energies. In addition detectors produced with these materials are not portable due to their high leakage current and their need of a cooling system.

Silicon’s properties such as high absorption length and high carrier mobility make it suitable for this project. The high absorption length results in most of the X-ray energy being absorbed. The high charge carrier mobility for both holes and electrons in Si leads to sufficient charge collection efficiency in the X-ray detector. Silicon’s large band gap (1.12 eV) assures that the thermally-generated leakage current at any given temperature will be smaller than for other semiconductor materials. This makes Si suitable for portable X-ray detector production since a cooling system is not needed. Si with a resistivity of 5 kΩ-cm and carrier life-time of 1 ms was chosen for this project. The high carrier life-time makes the detector more efficient since it generates lower leakage current.

The development of the new Si X-ray detector involved the use of the latest technology. Nine different pin-diode detectors were designed, modelled and manufactured for this project. The detectors were designed and modelled using the Silvaco package, which provides complex simulator tools that enabled us to determine the optimal detector configuration. The parameters that control the performance of the detector such as leakage currents and breakdown voltage were investigated.

The Silvaco simulation software enabled us to determine the optimal configuration in terms of choice of material, device dimensions, number of guard-rings, the distance between the guard-rings and their widths, parameters for processing methods such as implantation energy and dose, annealing time and temperature. The electrical performance of the pin-diode detector was also determined by running the simulations.

The electrical simulation indicated that the leakage current is about 80 nA and the breakdown voltage is as low as 140 V for pin-diode detectors without guard-rings. After placing the guard-rings in the pin-diode detectors, the leakage current reduced to 5 nA and the breakdown voltage increased to about 700 V, 850 V and 1300 V for pin-diode detectors with one, two and three guard-rings respectively.
The nine different manufactured pin-diode detectors were designed so as to provide a combination of parameters to test. Thus:

- Four devices were equipped with three guard-rings and the rest had two guard-rings
- Two of the detectors had floating guard-rings and the rest had Al contacted guard-rings
- Two of the pin-diode detectors had an oxide layer on the active-area and the rest had Al contact on.
- One detector was manufactured without an n⁺ layer around the edge whereas the rest all had an n⁺ layer.
- The implantation region under the active-area’s contact was implanted with 2 keV \( B^+ \times 3 \times 10^{13} \), tilt=7° and rotation=22° for three devices, while on the remaining six devices this region was implanted with an additional 10 keV \( B^+ \times 2 \times 10^{14} \), tilt=7° and rotation=22°.

The variety in the design of the nine devices allowed us to investigate the effect of the above parameters (number of guard-rings, floating or contacted guard-rings, devices with an oxide or Al layer on the active-area, deep or shallow ion implantation around the edge of the active-area) on the pin-diode detectors’ electrical performance.

Another parameter was the size of the active-area’s impact on the electrical performance and for this reason two pin-diode detectors with a 1 mm² active-area with 2 and 3 guard-rings respectively were designed and manufactured.

All nine pin-diode detectors were 5X5 mm² and with an active-area of 10 mm².

We also designed and manufactured some test devices on every chip on the wafers so as to measure the contact or sheet resistance and the carrier life-time.

After measuring the carrier-life time for one of the manufactured detectors we found that the carrier life-time reduced from 1 ms to 0.1 ms, which is not desirable as this leads to a higher leakage current.
Silvaco package does not take into account changes in the carrier life-time of the device throughout the processing. After compensating for the change in the carrier life-time in the Silvaco simulation, we observed that the I-V characteristic is comparable to the manufactured detector’s characteristic as shown in Figure 102. The leakage current was 70 nA at a voltage of 40 V for the manufactured device while it was 80 nA for the simulated detector. However for this project, the objective was to achieve as low a leakage current as 5 nA but the lowest leakage current measured for the manufactured detectors was one order of magnitude higher.

The following processing methods were applied on the Si wafers in order to manufacture the pin-diode detectors: oxidation, ion implantation, annealing, photolithography, wafer cleaning, metallization, etching and contact sintering.

During the processing of the pin-diode detectors the following parameters were also refined:

- annealing times and temperature for activating the implanted ions

- annealing times and temperature for sintering the contacts

- Furnace settings to grow various oxide thicknesses

- sputterer configuration for deposition of the metal contacts

- Etch rate for different oxide and metal thicknesses.

- Numbers of parameters controlling the photolithography. Among others the exposed light dose, exposure time, spin speed, spin time, developing time and different temperatures and durations for the pre and post-baking.

As part of this project, we manufactured pin-diode detectors in two iterations.

The first processing run put all the theory gained using the Silvaco simulation programme into practice. We processed and analysed 4 wafers:

1) On the first wafer, we implanted the entrance window (active-area) of the detectors with 2 keV $BF_2^+$ $5 \times 10^{12}$, tilt=7° and rotation=22°.
2) On the second wafer, the entrance window was implanted with $BF_2^+ \times 10^{12}$, tilt=7° and rotation=22° through a 10 nm oxide.

3) The third wafer had its entrance windows implanted with 2 keV $B^+ \times 10^{13}$, tilt=7° and rotation=22°.

4) On the fourth wafer, the entrance window was implanted with 2 keV $B^+ \times 10^{13}$, tilt=7° and rotation=22° through a 10 nm oxide.

We analysed the results of the first run and identified a number of areas where there was some flexibility in the manufacturing process.

In the first processing run, devices with implanted $B^+$ and implanted $B^+$ through a layer of 10 nm oxide showed a lower leakage current than devices with implanted $BF_2^+$ and implanted $BF_2^+$ through a 10 nm oxide. After analysing the results of the first processing run, we decided to implant the entrance window of the detectors for the second run only with $B^+$. Two wafers were processed and analysed as part of the second run:

1) For wafer 1, the entrance window was annealed for 5 s at 950 °C

2) For wafer 2, the entrance window was annealed for 10 s at 850 °C.

Each wafer was split into 2 halves, the region under the contact on the active-area being implanted with a different quantity of $B^+$ in each half.

Due to the fact that the wafers were split into 2 sides for implantation, there were a total of 4 different batches of devices to analyse.

Batch 1 – Section of Wafer 1 (annealed for 5 s at 950 °C), anode’s contact implanted with 2 keV $B^+ \times 10^{13} \text{ cm}^{-2}$, tilt=7° and rotation=22°.

Batch 2 – Section of Wafer 1 (annealed for 5 s at 950 °C), anode’s contact implanted with an additional 10 keV $B^+ \times 10^{14} \text{ cm}^{-2}$, tilt=7° and rotation=22°.

Batch 3 – Section of Wafer 2 (annealed for 10 s at 850 °C), anode’s contact implanted with 2 keV $B^+ \times 10^{13} \text{ cm}^{-2}$, tilt=7° and rotation=22°.
Batch 4 – Section of Wafer 2 (annealed for 10s at 850 °C), anode’s contact implanted with an additional 10 keV $B^+ 2 \times 10^{14}$ cm$^{-2}$, tilt=7° and rotation=22°.

In the second run processing, measurements carried out on wafer 1 showed that:

- Detectors with 3 guard-rings (devices 1, 2, 3 and 4) have a greater leakage current than the detectors with 2 guard-rings (devices 5, 6, 7, 8 and 9) on the chip.

- Detector 6 with 2 guard-rings, an oxide layer on the active-area and a deep implantation with an additional 10 keV $B^+ 2 \times 10^{14}$, under the anode’s contact, yields the lowest leakage current among all the devices in wafer 1.

For wafer 2, again detectors with 3 guard-rings (devices 1, 2, 3 and 4) demonstrated a greater leakage current than the detectors with 2 guard-rings (device 5, 6, 7, 8 and 9) on the chip. As for wafer 1, detector 6 exhibits the lowest leakage current among all the detectors.

For all 4 batches it showed that detectors with an additional of 10 keV, $2 \times 10^{14}$ $B^+$ implantation under the anode’s contact exhibit lower leakage current than detectors with the same structure but without this additional implantation.

Detectors with floating guard-rings or an oxide layer on the active-area demonstrated a lower leakage current than detectors with contacted guard-rings or a layer of metal on the active-area.

Detectors with an n$^+$ layer at the edge exhibit a lower leakage current than detectors without this layer.

Comparing the results for detectors with a 1mm$^2$ active-area with detectors with an active-area of 10 mm$^2$, shows that the area has an impact on the leakage current. Detectors with larger area exhibit greater leakage current.

Wafer 2 in general showed a lower leakage current than wafer 1, meaning that it is better to anneal the active-area at a lower temperature and for a longer period (10s at 850 °C).
These laboratory experiments lead us to conclude that the optimal device configuration is as follows:

- Two guard-rings should be used
- An n⁺ layer should be implanted at the edge of the device
- The active-area should be covered with an oxide layer
- Floating guard-rings should be deployed
- The active-area should be implanted with 2 keV $B^+$ $3 \times 10^{13}$ cm$^{-2}$
- The implantation under the active-area’s contact should be deep enough to provide a good ohmic contact
- The active-area annealing process should last 10s at a temperature 850 °C
8 Future Work

The objective of this project was to produce pin-diode detectors with as low a leakage current as possible.

Si wafers with a resistivity of 5 kΩ-cm and 1ms carrier life-time were used for this project. The Silvaco simulation in Figure 39 shows that with a carrier life-time of 1 ms, the target leakage current is achievable.

However, during device processing, the carrier life-time decreased to about 0.1 ms, which is not desirable as this leads to a higher leakage current.

Since the carrier life-time decreases during the processing of the pin-diode detectors, we should in future choose Si wafers with carrier life-time higher than 1ms. Wafers with higher resistivity and high carrier life-time are usually more expensive. Another problem related to choosing silicon with a higher resistivity is that we do not know by what factor the carrier life-time will reduce as a result of the device processing steps and the laboratory environment.

This carrier life-time reduction factor can be found by processing Si wafers with different resistivities under the same laboratory and procedural conditions, measuring the changes in their carrier life-time at the end of the process.

These experiments would enable us to identify the optimal resistivity for a Si wafer that yields a carrier life-time about 1 ms at the end of the processing.

Devices exposed to particles during processing cause disturbances in the Si lattice that can scatter the carriers and hence increase the leakage current. Therefore, to manufacture pin-diode detectors with a low leakage current, we should carry out any processing in a low classified cleanroom (fewer particles permitted per cubic metre of air). Moreover, chemicals used in the manufacturing of the devices should be of ultra purity grade, where impurities are low. Both of these procedures would increase the cost of the device manufacture.

If the Si wafer resistivity, cleanroom environment or choice of chemicals cannot be modified, future work could be focused on changes to the pin-diode device structure.
- Reduction of the active-area of the pin-diodes will reduce the surface leakage current, which is the dominant component in the total leakage current (see chapter 6). The disadvantage of this approach is that a smaller active-area could result in the X-ray not being detected.

- Wafers with a thickness lower than the 450 \(\mu\)m used for this project would result in a lower leakage current. The disadvantage is the higher cost associated with thinner wafers.
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