REVERSIBLE RECTIFIERS

A Dissertation
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in the Faculty of Engineering of
the University of Surrey

By

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SUMMARY

In present-day variable speed a.c. drives the power system is usually of the D.C. link type. Here a diode bridge rectifier feeds a large capacitor to produce the D.C. link voltage, which in turn feeds an inverter and machine. In such a system, the input current waveform is severely distorted, degrading the power factor, and under regenerating operation of the machine the returned energy is usually dissipated in protection resistors. These drawbacks can be overcome by using active switches and PWM control in the front-end converter, which may then be called a REVERSIBLE RECTIFIER. With proper choice of control strategy power conversion between the mains and the machine, together with excellent waveform and power factor, can be achieved simultaneously.

In this dissertation, various control methods have been fully studied and critically compared, together with discussions of the special problems of each control scheme. It is shown that direct control of the a.c. current, in the so-called current-forced schemes, offers good stability in control of the power flow. Voltage-forced schemes have also been studied for comparison. Conditions for stability in both rectifying and regenerating modes have been analysed. This has led to guidelines for selecting a suitable control strategy in practical applications and to a method of designing a suitable control system.

The design and operation of a low power model reversible rectifier has been presented and two control systems have been built for implementing different control schemes. One control system is a simple analogue system which provides a cheap but still elegant approach to the control of reversible rectifiers. The other is by means of a transputer system, which allows the more refined schemes to be implemented and more importantly provides the possibility of integrated control of the reversible rectifier with that of the machine in the future. The experimental results obtained have shown to be entirely consistent with the theory.
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STYLE

\[ X \] Vector quantity
\[ |X| \] Amplitude of \( X \)
\[ \ddot{X} \] Phasor quantity
\[ X_0 \] Operating point quantity of \( X \)
\[ \Delta X \] Deviation of \( X \), or error
\[ X^* \] Demanded quantity of \( X \)
\[ X_f \] Fundamental value of \( X \)
\[ X_j \] Quantity in phase \( j \) (\( j=A, B, \text{or} C \))

SYMBOLS

\[ A_0 \] Voltage gain: \( -\frac{E_{dc0}}{V_{s0}} \)
\[ C \] Capacitor or capacitance in the d.c. link
\[ E_{dc} \] Instantaneous value of the d.c. link voltage
\[ G \] Transfer function between \( \Delta E_{dc} \) and \( \Delta I_s \)
\[ G_i \] Transfer function between \( \Delta E_{dc} \) and \( \Delta I_0 \)
\[ G_c \] Transfer function of a PI controller: \( K \frac{1 + 1/T_s}{1} \)
\[ G_f \] Transfer function of a first-order filter: \( K_{df} \frac{1 + T_{df}}{1} \)
\[ i_{sj} \] Instantaneous value of the input current in phase \( j \)
\[ i_{sj}^* \] Demanded value of \( i_{sj} \)
\[ i_{sf} \] Fundamental value of \( i_{sj} \)
\[ i_s \] Space vector of the input current
\[ I_{sm} \] Amplitude of \( i_{sj} \)
\[ I_s = \sqrt{\frac{3}{2}} I_{sm} \], or general notation of the input current
\( i_{sd} \) \quad d-axis \quad i_s
\( i_{sq} \) \quad q-axis \quad i_s
\( i_{s\alpha} \) \quad \alpha-axis \quad i_s
\( i_{s\beta} \) \quad \beta-axis \quad i_s
\( i_{\text{out}} \) \quad Instantaneous value of the output current drawn from the d.c. link
\( \bar{I}_0 \) \quad Average value of \( i_{\text{out}} \) at the operating point
\( K_{df} \) \quad Gain of \( G_f \)
\( K_p \) \quad Gain of \( G_c \)
\( L_s \) \quad Inductor or inductance in the a.c. side
\( m \) \quad modulation index
\( n \) \quad n-th sampling instant
\( \text{PF} \) \quad Power factor
\( R_s \) \quad Resistance in the a.c. side
\( R_0 \) \quad Equivalent load resistance at the operating point: \( \frac{E_{dc0}}{I_0} \)
\( S_j \) \quad Switching function in phase \( j \)
\( T_{df} \) \quad Time constant of \( G_{df} \)
\( T_1 \) \quad Time constant of \( G_c \)
\( T_s \) \quad Switching/Sampling period
\( \text{THD}_7 \) \quad Total harmonic distortion
\( V_R \) \quad General notation of the terminal voltage
\( v_{Rj} \) \quad Instantaneous value of the terminal voltage in phase \( j \)
\( v_{Rj0} \) \quad Fundamental value of \( v_{Rj} \)
\( V_R(k) \) \quad Space vector of the terminal voltage \( k=0,1,...,7 \)
\( v_{Rd} \) \quad d-axis \quad \( V_{R} \)(k)
\( v_{Rq} \) \quad q-axis \quad \( V_{R} \)(k)
\( v_{R\alpha} \) \quad \alpha-axis \quad \( V_{R} \)(k)
\( v_{R\beta} \) \quad \beta-axis \quad \( V_{R} \)(k)
\( v_{sJ} \) \hspace{1cm} \text{Instantaneous value of the mains voltage in phase } J

\( V_s \) \hspace{1cm} \text{Space vector of } v_{sJ}

\( V_{sm} \) \hspace{1cm} \text{Amplitude of the mains voltage}

\( V_s = \sqrt{3} \frac{2}{3} V_{sm} \), or general notation of the mains voltage

\( v_{sd} \) \hspace{1cm} \text{d-axis } V_s

\( v_{sq} \) \hspace{1cm} \text{q-axis } V_s

\( v_{s\alpha} \) \hspace{1cm} \text{\( \alpha \)-axis } V_s

\( v_{s\beta} \) \hspace{1cm} \text{\( \beta \)-axis } V_s

\( \omega \) \hspace{1cm} \text{Angular frequency of the mains}

\( \tau_C \) \hspace{1cm} \text{Time constant: } - \frac{R_0 C}{0}

\( \tau_L \) \hspace{1cm} \text{Time constant: } - \frac{L_0}{R_0}

\( \tau_s \) \hspace{1cm} \text{Time constant: } - \frac{L_s}{R_s}

\( X \) \hspace{1cm} \sqrt{\frac{L_s}{C}}
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CHAPTER 1  INTRODUCTION

1.1 Introduction

Advances in the technology of power semiconductors over the last decade have allowed a.c. machines, and especially cheap and robust asynchronous machines, supplied from solid-state variable-frequency variable-voltage sources, to become competitive in the market for variable speed drives. More recently, the advent of microcomputers and VLSI circuits has further stimulated the market. In consequence interest in ac drive systems is growing rapidly.

In implementing a high performance drive system nowadays, whether incorporating d.c. or a.c. machines, power control and conversion will be by means of electronic systems. However, all power electronic converters can add to the inherent power line disturbances by (i) interfering with the waveform of the mains and (ii) producing electromagnetic interference. Recently there have been investigations into a number of solutions to these problems. The research work presented here will focus on solutions to the first problem.

1.2 Supply Sources for AC Drive Systems

Supply sources for a.c. drives incorporating power electronic systems can be classified into two categories, namely a.c./a.c. conversion and a.c./d.c./a.c. conversion.
1.2.1 AC/AC Conversion

In addition to conventional cycloconverters, which can deliver a high-quality sinusoidal waveform at a low output frequency, and hence are superior for very low speed applications [MURPHY 1988], the more recently proposed matrix converters are superficially very attractive [VENTURINI 1980, ALESINA 1981]. In principle, control of voltage or current waveform, frequency and power factor at both input and output is possible, together with power flow in either direction. However, in many embodiments of this principle there must be 9 bidirectional power switches (or 18 back-to-back connected active devices arranged with diodes). Moreover, complicated control is required, which is a current research topic [OYAMA 1989, KWON 1991].

1.2.2 AC/DC/AC Conversion

In practice, except for a few special cases of very high power, low-speed applications, where cycloconverters are used, variable-frequency drives employ inverters with a d.c. link. Thus, power conversion consists of two stages — a rectifier at the front end to convert the mains a.c. to d.c., followed by an inverter at the other end to generate variable-frequency variable-voltage for the machine. In general, there are two types of this indirect power conversion, current-sourced and voltage-sourced configurations. The definition of current-sourced and voltage-sourced is on the basis of whether the dc link behaves as a current source or a voltage source, and their features have been compared by B. K. BOSE [BOSE 1986].
1.3 Harmonics, Power Factor and Regeneration

Fig.1-1 shows the schematic of a conventional voltage-sourced power conversion, which is widely used in a.c. drives. The disadvantages of this configuration are well-known:– (i) the input current waveform is severely distorted (the current contains 17.5% 5th harmonic, 11% 7th harmonic and other order harmonics); (ii) the power factor is correspondingly degraded, and, (iii) the circuit does not permit regeneration of power.

![Fig.1-1 Conventional Voltage-Sourced AC/DC/AC Power Conversion for A.C. Drives](image)

1.3.1 Harmonics in A.C. Line Currents

The applications of static power converter drives, both ac and dc, over the complete range of machine ratings, have grown rapidly in the past two decades. At one time, connecting one small static power converter to a large power system resulted in only a small amount of harmonic distortion in the power system. Now, it is claimed by some authors that harmonic considerations for almost any industrial power system require almost as much attention as short circuit and overvoltage considerations [STRATFORD 1980, SMITH 1984, RICE 1986, KLOSS 1991].
To illustrate the problems due to current harmonics $i_h$ in the input current $i_s$ of power electronic equipment, consider the simple block diagram of Fig.1-2. Because of the non-zero internal impedance of the mains, which is simply represented by $L_u$, the voltage waveform at the point of common coupling to the other loads will become distorted, which may cause them to malfunction. In addition to the voltage waveform distortion, some other problems due to the harmonic currents $i_h$ are as follows:

- If the inductive reactance of the source and the power factor improvement capacitive reactance resonate at the harmonic frequency, additional heating and overvoltage can occur;
- Errors in metering and malfunctioning of utility relays;
- Very poor power factor which can lead to equipment insulation failures, fuse melting, and excessive operation of protective equipment;
- Interference with communication and control signals.
In view of the rapid increase of power electronic equipment connected to the mains, a number of standards and guidelines have been established that specify limits on the magnitude of harmonic currents and supply voltage distortion at various harmonic frequencies in order to maintain good power quality [e.g. IEC NORM 555–3, IEEE-519, EN50 006].

One of the standards cited here is the revised IEEE-519, as shown in Table 1-1 and Table 1-2, which specifies requirements on the user as well as on the utility authority. Table 1-1 lists the limits on the harmonic currents that a user of power electronic equipment and other nonlinear loads is allowed to inject into the mains. Table 1-2 lists the quality of voltage that the utility authority must supply the user. A utility will be able to furnish the voltage as listed in Table 1-2, provided that the harmonics currents injected by the users on a distribution feeder are limited in accordance with Table 1-1.

The voltage distortion at the point of common coupling in Fig.1-2 depends on the internal impedance of the a.c. source, which is usually highly inductive, and the magnitudes of the injected current harmonics. At a harmonic $h$ of the supply frequency $\omega$, the harmonic voltage at the common point is:

$$V_h = ( h \omega L_u ) I_h$$  \hspace{1cm} (1-1)

where $I_h$ is the $h$-th harmonic current injected into the a.c. supply.
Table 1-1

Harmonic Current Distortion \( \frac{I_h}{I_f} \) in %: Harmonic current limits for a nonlinear load connected to a public utility at the point of common coupling with other loads at voltages of 2.4 to 69KV

<table>
<thead>
<tr>
<th>( I_{ss}/I_f )</th>
<th>( h &lt; 11 )</th>
<th>11&lt;h&lt;17</th>
<th>17&lt;h&lt;23</th>
<th>23&lt;h&lt;35</th>
<th>35&lt;h</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt; 20</td>
<td>4.0</td>
<td>2.0</td>
<td>1.5</td>
<td>0.6</td>
<td>0.3</td>
</tr>
<tr>
<td>20 - 50</td>
<td>7.0</td>
<td>3.5</td>
<td>2.5</td>
<td>1.0</td>
<td>0.5</td>
</tr>
<tr>
<td>50 - 100</td>
<td>10.0</td>
<td>4.5</td>
<td>4.0</td>
<td>1.5</td>
<td>0.7</td>
</tr>
<tr>
<td>100 - 1000</td>
<td>12.0</td>
<td>5.5</td>
<td>5.0</td>
<td>2.0</td>
<td>1.0</td>
</tr>
<tr>
<td>&gt; 1000</td>
<td>15.0</td>
<td>7.5</td>
<td>6.0</td>
<td>2.5</td>
<td>1.4</td>
</tr>
</tbody>
</table>

Notes:
1. \( I_{ss} \) is the maximum short-circuit current at the common coupling point.
2. \( I_f \) is the maximum fundamental frequency load current at the common point.
3. Even harmonics are limited to 25% of the odd harmonic limits above.

Sources:
(1) MOHAN[1989], pp.412-413
(2) DUFFEY[1988]

Table 1-2

Harmonic Voltage Limits \( \frac{V_h}{V_f} \) in % for Power Producers

<table>
<thead>
<tr>
<th>( \frac{V_h}{V_f} )</th>
<th>2.3 -69 kV</th>
<th>69-138kV</th>
<th>&gt;138kV</th>
</tr>
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<td>Maximum for individual harmonic</td>
<td>3.0</td>
<td>1.5</td>
<td>1.0</td>
</tr>
<tr>
<td>Total harmonic distortion (THD)</td>
<td>5.0</td>
<td>2.5</td>
<td>1.5</td>
</tr>
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</table>

Notes: This table lists the quality of the voltage that the power producer is required to furnish a user. It is based on the voltage level at which the user is supplied.

The internal inductance \( L_u \) is often specified in terms of the short circuit
current $I_{ss}$. On a per-phase basis, $I_{ss}$ will be the per-phase r.m.s. current supplied by the a.c. source to the fault, if all three phases are shorted to ground:

$$ I_{ss} = \frac{V_{\text{rms}}}{\omega L_u} \quad (1.2) $$

where $V_{\text{rms}}$ is the r.m.s. value of the per-phase internal voltage of the a.c. source. From Eqns.(1-1) and (1-2), the harmonic voltage can be expressed as:

$$ V_h \% = \frac{V_h}{V_{\text{rms}}} \times 100 = \frac{I_h}{I_{ss}} \times 100 \quad (1.3) $$

If $I_f$ is the rms value of the fundamental component of the current drawn by the power electronic load, then dividing both $I_h$ and $I_{ss}$ in Eqn.(1-3) by $I_f$ results in:

$$ V_h \% = \frac{(I_h/I_f)}{(I_{ss}/I_f)} \times 100 \quad (1.4) $$

where $(I_{ss}/I_f)$ represents the capacity of the mains with respect to the fundamental-frequency volt-amperes of the load. This equation shows that for an acceptable harmonic voltage distortion, a higher harmonic current ratio $(I_h/I_f)$ is allowed for a higher $(I_{ss}/I_f)$ ratio in Table 1-1. In addition, the harmonic voltage distortion is proportional to the harmonic order $h$, and therefore the maximum allowable harmonic current ratio $(I_h/I_f)$ decreases with increasing value of $h$, as shown in Table 1-1.
To quantify the distortion in the current waveform, a quantity called the *total harmonic distortion* (THD) is defined as:-

\[
\text{THD}\% = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_{\text{total}}} \times 100
\]  

(1.5)

where \(I_{\text{total}}\) is the total current (r.m.s.) drawn from the mains. It should be noted that the *total harmonic distortion* allowed in Table 1-1 increases with the ratio \(I_{\text{ss}}/I_f\). Examples of the application of Tables 1-1 and 1-2 can be found in the work of Duffey [DUFFEY 1988].

Conventional diode rectifiers, which are widely used for interfacing power electronic equipment to the mains, may easily exceed the limits on both individual current harmonics and the total harmonic distortion specified in Table 1-1 [STRATFORD 1980, SMITH 1984].

### 1.3.2 Power Factor

The power factor, PF, at which an equipment operates is the product of the current ratio \(I_f/I_{\text{total}}\) and the displacement power factor, DPF:

\[
\text{PF} = \frac{\text{power}}{\text{volt-ampere}} = \frac{I_f}{I_{\text{total}}} \cdot \text{DPF}
\]  

(1.6)

A large distortion in line current will result in a small value of the current ratio \(I_f/I_{\text{total}}\), and hence a small value of PF, even if DPF is close to unity.
The power factor indicates how effectively the equipment draws power from the mains; at a low power factor, the rms current drawn by the equipment will be relatively large, thus requiring increased volt-ampere ratings of the utility equipment such as transformer, transmission lines, and generator.

In general, the current drawn from the mains by conventional rectifiers contains a large amount of harmonics. Therefore, the power factor at which a conventional rectifier operates from the mains is degraded even though the displacement power factor is good.

1.3.3 Regeneration

In many applications, the machine speed has to be reduced, even to standstill, quickly and repeatedly. In regenerative operation, the braking energy (usually originally kinetic) is sent back from the machine to the d.c. link by reversing flow of the d.c. link current. Since the current direction through the conventional diode rectifier cannot reverse, some mechanism must be implemented to handle this energy during braking; otherwise the d.c. voltage can reach destructive levels.

A widely used strategy at present is to switch a resistor in parallel with the d.c. link capacitor, as shown in Fig.1-1, when the capacitor voltage exceeds a preset level, in order to dissipate the returned energy. This clearly reduces efficiency, and is considered to be unacceptable in some applications; the added equipment also increases the size and cost.
1.4 Solutions to the Problems

To solve the problem of harmonics injected into the mains, which may easily breach the increasingly stringent regulations, and the problem of uni-directional power flow in conventional rectifiers, there have been investigations into a number of possible ways of improving the input current waveforms and regenerative capability of the converters.

The solutions may be divided into three broad groups. The first consists of passive techniques for improving the current waveform [see 1.4.1.1]; the second consists of active circuits which can either improve the waveform [see 1.4.1.2] or provide a regenerative capability [see 1.4.2], but not both; the third, the subject of this dissertation, is an active circuit with both the waveshaping and the regenerative capability.

1.4.1 Input Current and Power Factor

1.4.1.1 passive techniques

The simplest approach is to add inductance on both the a.c. and the d.c. side of the rectifier bridge. The added inductor on the d.c. side reduces the d.c. current ripple and also reduces somewhat the a.c. current harmonics; thus the power factor is improved. The inductors in the a.c. side increase the commutation time and consequently slow down the sharp rising and falling edges of the currents, further reducing the harmonic content of the a.c. However, in practice the reduction of the harmonics is limited since the allowable value of the inductance is limited by the voltage drop on the a.c.
side and dynamic demands on the d.c. side. A method for calculating harmonic currents of a bridge rectifier with the filters has been described by Sakui [SAKUI 1989].

Another approach to using passive filters is shown in Fig.1-3. On the a.c. side, three series LC filters are connected between the phases, thus filtering the voltage harmonics determined by the parameters of the filters. In view of the variations of the parameters of the mains, such as short-circuit impedance, transmission line effects, harmonic voltage levels, the design of a proper filter still needs further investigation. In addition, introducing such filters in the system may cause resonance [V.d. BOSSCHE 1992].

![Fig.1-3 Passive LC Filters on the A.C. Side](image)

In general, passive waveshaping techniques have the advantage of being easy to understand, easy to implement, and reliable. However, they also have several disadvantages, which include:

- bulk and weight;
- the relatively high costs of reactive components;

- a narrow range of operating points for which the input power factor can be optimized;

- the relatively large input inductor which results in a significant reduction in d.c. voltage and in power regulation, and also has an adverse effect on the inverter control.

These disadvantages can be eliminated through the use of active input current waveshaping techniques, discussed in what follows.

1.4.1.2 active shaping techniques

Current shaping techniques have been widely used in pre-regulation of a single-phase diode bridge rectifier [KOCHER 1983, PRASAD 1988, MULKERN 1988, REDL 1985]. The basic principle centres on a boost type switch mode converter. By suitably activating the boost switch, the input current waveform can be made sinusoidal and in phase with the supply voltage. This shaping technique has also been introduced into three-phase diode bridges. Fig.1-4 shows a three-phase rectifier using three single-phase diode bridges with a current-shaping circuit in each bridge [KOCHER 1983]. Various shaping techniques used in the single-phase bridge may be used in this configuration [REDL 1985]. However, this configuration has some disadvantages, such as (i) requiring of electrical isolation, (ii) complicated input synchronization logic, (iii) the existence of triplen harmonics in the line current due to the variations in power circuit control parameters among the three individual rectifiers, and (iv) requiring more components.
Recently, another configuration has been proposed, as shown in Fig.1-5 (PRASAD 1991). It needs only one boost switch $Q$, in conjunction with a conventional three-phase diode bridge. Since the discontinuous current mode is used to control the a.c. current it has the disadvantages of substantially increasing the current rating of the switching devices and the high frequency ripple-content of the a.c. input currents. Such techniques for three-phase diode bridges are still the subject of current research topic [KOLAR 1992, PFORR 1992].
1.4.2 Regenerative Capability

With a voltage-sourced link configuration, there are several possibilities for achieving a bi-directional power flow. One well-known approach used in the past has been to employ two back-to-back connected line-frequency thyristor converters, as is shown in Fig.1-6. During the normal mode, converter 1 acts as a rectifier and the power flows from the a.c. input to the d.c. link. During regenerative mode, the gate pulses to the thyristors of converter 1 are blocked and converter 2 operates in an inverter mode where the polarity of d.c. voltage remains the same but the direction of d.c. current is reversed and the power flow is reversed. The drawbacks associated with this approach are obvious:— (i) the input current has a distorted waveform and the power factor is poor; (ii) the d.c. voltage is limited in the inverter mode because of the minimum extinction angle requirement of converter 2 while it operates in an inverter mode; and (iii) there is a possibility of commutation failure in the inverter mode due to a.c. line disturbances.

Fig.1-6 Back-to-Back Configuration for Bidirectional Power Flow
Another approach uses an auxiliary circuit to reverse the polarity of the connection to the d.c. link filter capacitor during regeneration [SCHAUDER 1988], as shown in Fig. 1-7. It was successfully used in commercial PWM inverter products. But the problems of the a.c. current harmonics and the poor power factor still remain. A passive filter discussed above has to be used to eliminate harmonics injected into the mains to meet the regulations.

![Fig.1-7 An Auxiliary Circuit in the D.C. Link for Bidirectional Power Flow](image)

A better alternative is to use a four-quadrant converter, a so-called *reversible rectifier*, to replace a conventional diode or thyristor bridge, as shown in Fig. 1-8. Such a reversible rectifier is capable of supplying sinusoidal input current at a unity power factor; in addition, the power flow through the converter is reversible. The history of previous work on this technique is given later, in section 1.6.

1.5 Control Systems of a Reversible Rectifier

The technology of the reversible rectifier divides into two areas of interest. One is that of the power electronic devices, their driving circuits, and any auxiliary components for protection. The circuit is
essentially a three phase inverter for which this aspect of the technology is quite well known, and so is not discussed further in the present work. The other area concerns control, which again subdivides into two areas, as shown in Fig.1-9. The two areas arise from the two functions of the reversible rectifier — to achieve good waveform the a.c. currents must be controlled, while to regulate the power flow it is most convenient to control the d.c. link voltage. A brief outline follows, but the detail is the subject of this dissertation.

In essence, the power circuit of a three-phase reversible rectifier, shown in Fig.1-8, looks like a conventional inverter, but with the important difference that the input is the a.c. side, and the quantities to be controlled are the d.c. voltage $E_{dc}$ and the a.c. currents $I_s$. Although
Control of the A.C. Currents

- Current-Forced (Chapter 3)
  - monitoring a.c. currents
  - generation of current references
  - tracking the references
    - hysteresis
    - simple
    - space vector based
    - ramp comparison
    - predictive

- Voltage-Forced (Chapter 4)
  - phase locked loop
  - calculations
  - modulations
    - sinusoidal PWM
    - 3rd harmonic injection
    - harmonic elimination
    - space vector modulation

Control of the D.C. Link Voltage

- Measurement
- Filtering
- Regulations (Chapter 5)
  - P controller
  - PI controller
  - PI controller plus load
    - information injection

Fig.1-9 Classification of Control Schemes

Several different switching and control strategies are available, they may be divided into two categories, namely current-forced schemes and voltage-forced schemes, according to the principle of control of the a.c. currents. Fig.1-10 shows the block diagram of the control system, where a typical dual-loop system is used to control both the a.c. current and the d.c. link voltage.

1.5.1 Voltage-Forced Schemes

From the mathematical models discussed later, it will be seen that the input currents are governed by controlling the terminal voltages $V_R$. In voltage-forced schemes, the a.c. currents are not monitored directly. Instead, the fundamental value of the terminal voltage $V_R$ is controlled, by appropriately actuating the power devices, to be of such magnitude and phase that voltages across the inductors $L_s$ are in quadrature with the supply voltages $V_s$. This is equivalent to forcing the power factor to be unity; of
course, if some other phase angle were to be chosen the power factor could be controlled arbitrarily. The sinusoidal current waveforms are guaranteed by employing a suitable modulation technique and selecting an appropriate value of input inductance and d.c. link voltage. The power flow is governed by the magnitude of the voltages across the input inductors; it is normally controlled by the second loop which regulates the d.c. link voltage.

1.5.2 Current-Forced Schemes

In this scheme, the a.c. currents are monitored and compared with reference currents. The differences (errors) can be directly used to determine the switching of the power devices in the rectifier (hysteresis comparison) or to calculate the required instantaneous value of the terminal voltage (predictive control scheme). If a suitable method of comparison is chosen, the actual currents can be "forced" to track the reference. The shape of
the reference waveform, which is usually made sinusoidal, is generated separately, and it is phase-locked to the mains. The amplitude of the reference currents should be of just the right value for the power drawn from the supply to balance the power supplied by the load, usually an inverter fed to an a.c. machine. This balance is regulated by controlling the d.c. link voltage; it will be seen that better performance is possible if there is also injection of information about the load.

1.6 Literature Survey and Objective of Present Research

Studies on reversible rectifiers seem to have started about a decade ago [KATAOKA 1979], and there were a few reports of such rectifiers in drive systems for asynchronous machines [OOI, 1988] and synchronous machines [DIXON, 1987]. Some standard current-control schemes for inverters, such as the simple hysteresis comparison (or bang-bang control) scheme, were directly used in the control of reversible rectifiers [NISHIMOTO 1987, OOI 1987,1988, GREEN 1988]. When the presented research started in 1989, discussions in the literature regarding current-forced schemes had been found to be restricted to simple implementations using hysteresis comparison techniques for controlling the a.c. current. In parallel with the present research work, other current-forced schemes were also being implemented, such as predictive control schemes [WU 1990, HABETLER 1991]. In addition, there were a few reports of voltage-forced schemes [WERNEKINCK 1987, DIXON 1988, GREEN 1988, SUGIMOTO 1988]. Some authors studied the stability of control system [BOYS 1989, DIXON 1988], but the important aspect of designing a suitable controller appears so far not to have been addressed. Injection of load information to improve control of power flow was proposed by Sul and
Lipo in their paper on a 20KHz resonant link asynchronous machine drive system [SUL 1990]. However, the effect of the load information injection has apparently not yet been studied in detail.

The objective of the present research work may be summarized as follows:

(a) To derive the mathematical models of a reversible rectifier and develop simulation programs for further investigation;

(b) To investigate and compare various control schemes relevant to the a.c. current control, and discuss the problems peculiar to each, thereby giving a framework and guidelines for the selection of the best scheme for any particular application;

(c) To investigate the power flow control, stability and transient response of the control system and to propose a method for designing a suitable controller;

(d) To build a prototype reversible rectifier in order to understand completely operation of the power circuit;

(e) To build various control systems in order to investigate them experimentally and verify the theoretical analysis;

There are eight chapters in this dissertation. The present chapter is an introduction. In Chapter 2, the operation of the power circuit of the reversible rectifier is described and its mathematical models are derived, based on the general knowledge of a three-phase inverter and the theory of the a.c. machine. Various tracking techniques presented in Chapter 3 are studied with reference to previous work on the control of three-phase inverters, but some analysis, discussion and the comparison between these techniques used in the control of reversible rectifiers are believed to be
original. Basic principles of the voltage-forced scheme are presented in Chapter 4; here the discussion about the minimum value of the d.c. link voltage and the application of the third harmonic injection to reduce this value have not been found reported in the literature. In Chapter 5, the stability and transient analysis, with emphasis on designing a suitable PI controller, are entirely original. A preliminary study of a novel control scheme using the theory of variable structure systems is presented in Chapter 6, based on the idea from HABETLER [HABETLER 1989]. The practical work reported in Chapter 7 is also entirely original. It should be noted that prior to my work, there was no experience of reversible rectifiers at the University of Surrey. The prototype rectifier and experimental set up were all designed and constructed independently, allowing this research work to start and continue. Finally, future work on reversible rectifiers is suggested in Chapter 8.
CHAPTER 2. FUNDAMENTAL CIRCUIT EQUATIONS

2.1 Introduction

This chapter starts with a brief description of the operation of the power circuit. The reasonable assumption is made that, because of the input line inductances, the a.c. currents are continuous throughout each switching cycle. As a result, all the power devices (switching device/diode pairs) can be treated as ideal bi-directional switches, and mathematical models using switching function developed. Models for different reference frame are derived. A suitable form of the models will be used later in the analysis, simulation and design of the control system.

2.2 Power Circuit Operation

The operation of a voltage-sourced reversible rectifier can be readily illustrated with the help of a single-phase rectifier, as shown in Fig.2-1.

![Diagram](image)

Fig.2-1 A Single-Phase Reversible Rectifier
(a) Power Circuit          (b) Simplified Diagram
The rectifier differs from a conventional voltage-doubling rectifier in that an inverse parallel power switch is added across each diode in order to provide a controllable path for bi-directional current flow. In addition, there is an input inductor, \( L_s \), as a buffer between the dc link and the supply.

Before the rectifier can be controlled in the desired mode, the two capacitors \( C_p \) and \( C_n \) must have become charged to the peak voltage of the supply \( v_s \) through two diodes. Once the capacitors are fully charged, the diodes are reverse-biased, and the voltages \( E_{dcp} \) and \( E_{dcn} \) can be switched in series with the supply, \( v_s \), through the two power switching devices \( Q_p \) and \( Q_n \).

In order to preclude a short-circuit of the d.c. link voltage the drive circuit must ensure that only one of the devices is switched on at any given time. Moreover, because of the presence of the inductance, \( L_s \), when a device switches off the current commutates into the diode of the other switch/diode pair. When a continuous current is flowing out of the centre point of the bridge, the upper switching device \( Q_p \) and lower diode \( D_n \) conduct alternately. When the current is flowing into the centre point, the lower device \( Q_n \) and upper diode \( D_p \) conduct. In essence the two switch/diode pairs behave as a two-pole bi-directional switch. Therefore, the power circuit in Fig.2-1(a) can henceforth be represented by a simplified diagram as shown in Fig.2-1(b), where all the power devices and diodes pair are replaced by a single ideal, "two-pole switch".

The power circuit of a three-phase voltage-sourced reversible rectifier
shown in Fig.1-8 has the same configuration as that of the well-know three-phase bridge inverter. The commutation occurs between the switching devices and diodes just as in the single-phase rectifier described above. In detail the commutation is analogous to that in voltage-sourced inverters, and can be found in reference [GRANT 1987].

2.3 Mathematical Models

2.3.1 Model of a Single-Phase Rectifier

Consider Fig.2-1(b) with the ideal switch being turned to the positive rail. The current $i_s$ then flows through the upper components, $Q_p$ or $D_p$ and its rate of change is governed by:–

$$\frac{di_s}{dt} = v_s - E_{dcp}$$  \hspace{2cm} (2.1)

Similarly, when the ideal switch is turned to the negative rail, current $i_s$ flows through the lower components, $Q_n$ or $D_n$, and its rate of change is:–

$$\frac{di_s}{dt} = v_s + E_{dcn}$$  \hspace{2cm} (2.2)

The instantaneous value of the input current $i_s$ is determined by Eqns.(2.1) and (2.2), in accordance with the two switching states. In the normal operating case, the d.c. link voltages $E_{dcp}$ and $E_{dcn}$ are larger than the peak value of the supply $v_s$. So, the current $i_s$ will increase when $Q_n$ or $D_n$ is conducting, since $di_s/dt$ is positive (governed by Eqn.(2.2)), and
decrease when \( Q_p \) or \( D_p \) is on as \( di_s/dt \) is negative (governed by Eqn.(2.1)).

Equations (2.1) and (2.2) can be rewritten in terms of a switching function, \( S \), which is defined as taking a value either 1 or 0 according to the position of the ideal switch. Thus:

\[
\frac{di_s}{dt} = \frac{v_s}{L} - SE_{dcp} + (1-S)E_{dcn} \tag{2.3}
\]

where

\[
S = 1 \text{ corresponds to the switch being turned to the positive rail (} Q_p \text{ or } D_p \text{ is on), and } S = 0 \text{ corresponds to the switch being turned to the negative rail (} Q_n \text{ or } D_n \text{ is on).}
\]

From the d.c. link, the following equations are obtained:

\[
\frac{dE_{dcp}}{dt} = Si_s - i_{out}
\]

\[
\frac{dE_{dcn}}{dt} = -(1-S)i_s - i_{out} \tag{2.4}
\]

where \( i_{out} \) is load current.

Equations (2.3) and (2.4) describe the dynamic behaviour of the single-phase reversible rectifier in terms of the switching function. If the switching devices are actuated appropriately, that is, a suitable variation of switching function through the switching period is chosen, both
the input current $i_s$ and the dc link voltage $E_{dc} \ (= E_{dep} + E_{dcm})$ may be controlled.

2.3.2. Model of a Three-Phase Rectifier

An exact mathematical description for a three-phase rectifier in terms of switching functions can be derived in a similar manner. The power circuit is simplified, as shown in Fig.2-2(a), by replacing the device/diode pairs by three ideal two-pole switches. The state of these switches depends on the value of the corresponding switching functions $S_j \ (j = A, B, and C)$.

![Simplified Circuit of a Three-Phase Rectifier](image)

(a) Simplified Circuit  
(b) Per-Phase Equivalent Circuit

When an ideal switch is turned to the positive rail the relevant switching function takes the value 1, and conversely the value 0.
For phase A, the following equation is obtained:

\[ L_s \frac{di}{dt}_{sA} + R_s i_{sA} = v_{sA} = v_{sA} - (v_{AM} + v_{MN}) \] (2.5)

The voltage between \( A \) and \( M \), \( v_{AM} \), is equal to the d.c. link voltage \( E_{dc} \) when the switching function \( S_A \) has the value 1; and \( v_{AM} \) is zero (if the voltage drop across the power device is ignored) when \( S_A \) takes value 0. In terms of the switching function, Eqn.(2.5) becomes:

\[ v_{LaA} = L_s \frac{di_{sA}}{dt} = -R_s i_{sA} + v_{sA} - (S_A E_{dc} + v_{MN}) \] (2.6)

Equations for phase B and C are identical except for an appropriate change of subscript.

Often in practice there will be no neutral line, and so the line current will sum to zero:

\[ i_{sA} + i_{sB} + i_{sC} = 0 \] (2.7)

Then, the voltage \( v_{MN} \) can be obtained by adding the three equations like Eqn.(2.6), and using (2.7) to eliminate the currents. The result is:

\[ v_{MN} = -\frac{1}{3} (S_A + S_B + S_C) E_{dc} + \frac{1}{3} (v_{sA} + v_{sB} + v_{sC}) \] (2.8)

Substituting Eqn.(2.8) in (2.6), and the other two similar equations,
yields:

\[ v_{LA} = L_s \frac{di_{sA}}{dt} = -RI_{sA} - v_{RA} + \left( \frac{2}{3}v_{sA} - \frac{1}{3}v_{sB} - \frac{1}{3}v_{sC} \right) \]

\[ v_{LB} = L_s \frac{di_{sB}}{dt} = -RI_{sB} - v_{RB} + \left( -\frac{1}{3}v_{sA} + \frac{2}{3}v_{sB} - \frac{1}{3}v_{sC} \right) \quad (2.9) \]

\[ v_{LC} = L_s \frac{di_{sC}}{dt} = -RI_{sC} - v_{RC} + \left( -\frac{1}{3}v_{sA} - \frac{1}{3}v_{sB} + \frac{2}{3}v_{sC} \right) \]

where

\[ v_{RA} = \left( \frac{2}{3}S_A - \frac{1}{3}S_B - \frac{1}{3}S_C \right)E_{dc} \]

\[ v_{RB} = \left( -\frac{1}{3}S_A + \frac{2}{3}S_B - \frac{1}{3}S_C \right)E_{dc} \quad (2.10) \]

\[ v_{RC} = \left( -\frac{1}{3}S_A - \frac{1}{3}S_B + \frac{2}{3}S_C \right)E_{dc} \]

Another differential equation can be obtained from the d.c. link:

\[ C \frac{dE_{dc}}{dt} = i_{sA} S_A + i_{sB} S_B + i_{sC} S_C - i_{out} \quad (2.11) \]

Eqns (2.9) and (2.11) constitute a complete differential equation set describing behaviour of the rectifier.

If the phase-neutral voltages of the supply are symmetrical, that is:

\[ v_{sA} + v_{sB} + v_{sC} = 0 \quad (2.12) \]

the differential equation set in Eqn.(2.9) may be rewritten in the
Thus, it is possible to represent a three-phase rectifier by its per phase equivalent circuit shown in Fig.2-2(b). Note that the variables \( v_{sj} \), \( v_{RJ} \) and \( i_{sj} \) are instantaneous values. In addition, the terminal voltage \( v_{RJ} \) at the terminal of the rectifier, is a discontinuous function depending on the switching function \( S_j \). This equivalent circuit is always valid provided that the supply is balanced and three input inductors are identical.

2.3.3 Model in the Stationary \( \alpha-\beta \) Frame

The model discussed above, expressed in the three-phase system (A–B–C frame), is sometimes inconvenient to use in analysis. Transforming the model into a two-phase system, such as a stationary \( \alpha-\beta \) or a rotating d–q reference frame, will simplify representation and analysis. In this section, the model in the \( \alpha-\beta \) frame will be derived.

Although the input inductors of rectifier do not have to be placed symmetrically in space, unlike the winding of three-phase machine, it is nevertheless convenient to use the axis arrangement of Fig.2-3. This also helps in defining and explaining the concept of space vector, to be discussed later.
It is clear from Fig. 2-3 how the balanced supply voltages in the A-B-C frame can be transferred to those in the $\alpha$-$\beta$ frame. The other quantities, such as currents $i_{s1}$ and terminal voltages $v_{r1}$, can be transformed in a similar manner. To derive the transformation relation it is convenient to set the $\alpha$-axis to be coincident with the A-axis and ignore the zero-sequence component. Then, the transformation relation can be given as:

$$
\begin{bmatrix}
    v_{s\alpha} \\
    v_{s\beta}
\end{bmatrix} = T_{\alpha\beta/ABC} \begin{bmatrix}
    v_{sA} \\
    v_{sB} \\
    v_{sC}
\end{bmatrix}
$$

(2.14)

where

$$
T_{\alpha\beta/ABC} = \sqrt{\frac{2}{3}} \begin{bmatrix}
    1 & -1/2 & -1/2 \\
    0 & \sqrt{3}/2 & -\sqrt{3}/2
\end{bmatrix}
$$

(2.15)

and the corresponding inverse transformation as:
\[
\begin{bmatrix}
v_{s\alpha} \\
v_{s\beta} \\
v_{s\gamma}
\end{bmatrix} = T_{ABC/\alpha\beta}
\begin{bmatrix}
v_{s\alpha} \\
v_{s\beta}
\end{bmatrix}
\] (2.16)

where

\[
T_{ABC/\alpha\beta} = \sqrt{\frac{2}{3}} \begin{bmatrix}
1 & 0 \\
-\frac{1}{2} & \sqrt{\frac{3}{2}} \\
-\frac{1}{2} & -\sqrt{\frac{3}{2}}
\end{bmatrix}
\] (2.17)

The coefficient \( \sqrt{\frac{2}{3}} \) is used to keep the power constant after transformation. Applying transformation (2.15) in Eqns. (2.13) and (2.11) yields:

\[
\begin{align*}
L_s \frac{dl_{s\alpha}}{dt} &= -R_s l_{s\alpha} - v_{R\alpha} + v_{s\alpha} \\
L_s \frac{dl_{s\beta}}{dt} &= -R_s l_{s\beta} - v_{R\beta} + v_{s\beta}
\end{align*}
\] (2.18)

\[
C \frac{dE_{dc}}{dt} = S_{\alpha} l_{s\alpha} + S_{\beta} l_{s\beta} - l_{out}
\] (2.19)

where

\[
\begin{align*}
v_{R\alpha} &= S_{\alpha} E_{dc} = \sqrt{\frac{2}{3}} \left[ S_A - \frac{1}{2} S_B - \frac{1}{2} S_C \right] E_{dc} \\
v_{R\beta} &= S_{\beta} E_{dc} = \sqrt{\frac{2}{3}} \frac{\sqrt{3}}{2} \left[ S_B - S_C \right] E_{dc}
\end{align*}
\] (2.20)
\[ S_\alpha \text{ and } S_\beta \text{ are defined by:} \]
\[
\begin{bmatrix}
S_\alpha \\
S_\beta
\end{bmatrix}
= T_{\alpha\beta/ABC}
\begin{bmatrix}
S_A \\
S_B \\
S_C
\end{bmatrix}
\]
\[
= \sqrt{\frac{2}{3}}
\begin{bmatrix}
S_A - \frac{1}{2} S_B - \frac{1}{2} S_C \\
\frac{\sqrt{3}}{2} S_B - \frac{\sqrt{3}}{2} S_C
\end{bmatrix}
\]  
\hspace{1cm} (2.21)

The variables \( S_\alpha \) and \( S_\beta \) are defined in order to simplify the notation, and they only have a meaning when they are multiplied by the a.c. currents or the d.c. link voltage. If a switching function vector \( S = S_\alpha + j S_\beta \) is defined, as will be shown later, \( S_\alpha \) and \( S_\beta \) are the projections of the vector \( S \) to the \( \alpha \)-axis and \( \beta \)-axis, respectively.

2.3.4. Space Vector-Based Model

In studying a.c. machines, certain quantities are found to have variables which are sinusoidal in time, or sinusoidally distributed in space, and often both. For three-phase rectifiers, all quantities concerned are functions in time, but not in space. However, it is still beneficial to "borrow" the concept of space vector for studying rectifiers; the "space" can mathematically be regarded as a complex plane, rather than a physical space.

If the \( \alpha \)-axis is defined as the real-axis and \( \beta \)-axis as the imaginary-axis in the space plane, a space vector model of a rectifier can be obtained.
Define a space vectors (Park vectors) as:

(1) Supply voltage space vector $V_s$:

$$V_s = v_{sA} + j v_{sB} = \sqrt{\frac{2}{3}} \left( v_{sA} + \alpha v_{sB} + \alpha^2 v_{sC} \right)$$  \hspace{1cm} (2.22)

(2) Input current space vector $i_s$:

$$i_s = i_{sA} + j i_{sB} = \sqrt{\frac{2}{3}} \left( i_{sA} + \alpha i_{sB} + \alpha^2 i_{sC} \right)$$  \hspace{1cm} (2.23)

(3) Switching function space vector $S(k)$:

$$S(k) = S_A + j S_B = \sqrt{\frac{2}{3}} \left( S_A + \alpha S_B + \alpha^2 S_C \right)$$  \hspace{1cm} (2.24)

(4) Rectifier terminal voltage space vector $V_R(k)$:

$$V_R(k) = v_{rA} + j v_{rB} = \sqrt{\frac{2}{3}} \left( v_{rA} + \alpha v_{rB} + \alpha^2 v_{rC} \right)$$

$$= \sqrt{\frac{2}{3}} \left( S_A + \alpha S_B + \alpha^2 S_C \right) E_{dc}$$

$$= S(k) E_{dc}$$  \hspace{1cm} (2.25)

where

$$\alpha = e^{j(2\pi/3)} = -\frac{1}{2} + j \frac{\sqrt{3}}{2}$$

$$\alpha^2 = e^{j(-2\pi/3)} = -\frac{1}{2} - j \frac{\sqrt{3}}{2}$$

Then, the equation (2.18) can be expressed in terms of space vectors as:
\[
\frac{di_s}{dt} = -R_s i_s - V_R(k) + V_s
\]

\[= -R_s i_s - S(k) E_{dc} + V_s \quad (2.26)\]

It should be noted that a vector quantity must be specified by both its magnitude and its direction in space. In the space vector model, the supply voltage vector \(V_s\) rotates at the angular frequency \(\omega\) of the supply on the space plane, with a constant magnitude, \(\sqrt{\frac{2}{3}} \cdot \frac{3}{2} V_{sm}\), where \(V_{sm}\) is the magnitude of the phase-neutral voltage of the mains. Projections of the supply voltage vector \(V_s\) and the input current vector \(i_s\) to the phase axes give the corresponding instantaneous phase-neutral quantities, multiplied by a factor of \(\sqrt{\frac{2}{3}} \cdot \frac{3}{2}\).

![Space Vectors of the Terminal Voltage](image)

The terminal voltage vector \(V_T(k)\), as well as the switching function vector \(S_R(k)\), however, has the eight distinct components in the plane shown in Fig.2-3. This is because it depends on the switching functions \(S_A, S_B\) and
S^c, each of which has two logic states, 1 or 0, and so only \(2^3 = 8\) combinations are available. For convenience a decimal number \(k\) is used to represent these eight distinct components. The decimal number \(k\) is converted from a 3-bit binary number, with \(S^c\) being the least significant bit(LSB) and \(S^a\) the most significant bit(MSB). If the combination of the switching function \(S^a S^b S^c\) has a state of 100, for example, the corresponding decimal number \(k\) is 4 and the terminal voltage vector therefore has a component \(V^{R}(4)\).

Vectors \(V^{R}(1) \sim V^{R}(6)\) are called active vectors or nonzero voltage vectors which have a length of \(\sqrt{\frac{2}{3}} E^{dc}\). Correspondingly, two non-active vectors or zero voltage vectors, \(V^{R}(0)\) and \(V^{R}(7)\), have a zero length, which is a consequence of either all the upper devices or all the lower devices being on.

Combinations of the switching functions in a switching cycle generate a corresponding \(V^{R}(k)\). The current vector \(i^s\), which is governed by Eqn.(2.26), will hence be able to be determined. Proper selection of the switching functions will allow production of the correct \(V^{R}(k)\) instantaneously to "force" \(i^s\) to be of the required form.

2.3.5. Model in the Rotating d-q Frame

In some circumstances, a model in a frame rotating at the angular speed \(\omega\) of the supply is preferable. The time-varying parameters are eliminated and the variables and parameters are expressed in components along the orthogonal and mutually decoupled direct (d) and quadrature (q) axes.
With reference to Fig.2-3, the voltages in the stationary $\alpha$-$\beta$ frame are converted to the rotating d-q frame as follows:

\[
\begin{pmatrix}
    v_{sd} \\
    v_{sq}
\end{pmatrix}
= T_{dq/\alpha\beta}
\begin{pmatrix}
    v_{s\alpha} \\
    v_{s\beta}
\end{pmatrix}
= T_{dq/\alpha\beta} T_{\alpha\beta/ABC}
\begin{pmatrix}
    v_{sA} \\
    v_{sB} \\
    v_{sC}
\end{pmatrix}

= T_{dq/ABC}
\begin{pmatrix}
    v_{sA} \\
    v_{sB} \\
    v_{sC}
\end{pmatrix}
\]

(2.27)

where

\[
T_{dq/\alpha\beta} = \begin{pmatrix}
    \cos\theta & \sin\theta \\
    -\sin\theta & \cos\theta
\end{pmatrix}
\]

(2.28)

\[
T_{dq/ABC} = T_{dq/\alpha\beta} T_{\alpha\beta/ABC}
= \sqrt{\frac{2}{3}}
\begin{pmatrix}
    \cos\theta & -\frac{1}{2}\cos\theta + \frac{\sqrt{3}}{2}\sin\theta & -\frac{1}{2}\cos\theta - \frac{\sqrt{3}}{2}\sin\theta \\
    -\sin\theta & \frac{1}{2}\sin\theta + \frac{\sqrt{3}}{2}\cos\theta & \frac{1}{2}\sin\theta - \frac{\sqrt{3}}{2}\cos\theta
\end{pmatrix}
\]

(2.29)

The other quantities, such as currents and terminal voltages, can be transformed in a similar manner. From the Eqns.(2.18), (2.19), the following equations are obtained by means of the transformation (2.29):--
\[\begin{align*}
\frac{d}{dt} L \frac{di}{ds} &= -R_i s_{sd} - v_{Rd} + v_{sd} + \omega L \frac{i}{s_{sq}} \\
\frac{d}{dt} \frac{di}{sq} &= -R_i s_{sq} - v_{Rq} + v_{sq} - \omega L \frac{i}{s_{sd}} \\
C \frac{dE_{dc}}{dt} &= S_i s_{sd} + S_i s_{sq} - i_{out}
\end{align*}\] (2.30)

where

\[ v_{Rd} = S_i E_{dc} \text{ and } v_{Rq} = S_i E_{dc} \]

\[ S_d = S_\alpha \cos\theta + S_\beta \sin\theta \]
\[ = \sqrt{\frac{2}{3}} \left( S_A - \frac{1}{2} S_B - \frac{1}{2} S_C \right) \cos\theta + \sqrt{\frac{2}{3}} \frac{\sqrt{3}}{2} \left( S_B - S_C \right) \sin\theta \]

\[ S_q = -S_\alpha \sin\theta + S_\beta \cos\theta \]
\[ = -\sqrt{\frac{2}{3}} \left( S_A - \frac{1}{2} S_B - \frac{1}{2} S_C \right) \sin\theta + \sqrt{\frac{2}{3}} \frac{\sqrt{3}}{2} \left( S_B - S_C \right) \cos\theta \]

In the d-q frame, the sinusoidal variables appear as dc quantities. The variables \( S_d \) and \( S_q \), introduced to simplify the notation, are the projections of the switching function vector \( S \) to the d-axis and q-axis, respectively. The coupling terms, \( \omega L_i s_{sd} \) and \( \omega L_i s_{sq} \) in Eqn.(2.30), result from the rotation of the coordinate frame.

### 2.4 Summary

In this chapter a large signal model describing the dynamic behaviour of a three-phase reversible rectifier in real time domain has been derived in
terms of switching functions. It is also helpful to extend the concept of
the space vector, introduced originally in a.c. machines, by deriving a
space vector model which will be used in the discussion and analysis of the
control schemes in the following chapters. Other forms of the model, such
as the model in d-q frame, are found to be convenient to be used in some
circumstances. The details of derivation have been given and the
transformations between these models provided.
CHAPTER 3. CURRENT-FORCED CONTROL SCHEMES

— DIRECT CONTROL OF A.C. CURRENTS

3.1 Introduction

In this chapter, a number of strategies for the direct control of a.c. current, which are generally termed current-forced schemes, will be investigated.

There are two areas of interest relevant to current-forced schemes. One is the generation of the reference currents which have sinusoidal waveforms together with the desired amplitude and the phase with respect to the mains. The other is the tracking techniques which force the actual currents to follow the references.

Various tracking techniques for the control of inverters have been summarized by Brod [BROD 1985]. However, there are some differences between inverters and rectifiers in the quantities to be controlled, which require that these techniques be investigated further in the present work. Generally, the tracking techniques can be divided into three categories, namely:- hysteresis comparison, ramp comparison and predictive control. All of these techniques will be studied fully and compared in this chapter. The results can be used for selecting the most suitable current-forced control system in any specific application.

Section 3.2 will discuss power flow control and generation of the current
3.2 Power Flow Control and Generation of the Reference Current

In any current-forced scheme a template for the input current has to be produced. This reference current should be of just the right value for the power drawn from the mains to balance the power supplied by the machine. The most readily available measure of the degree of unbalance is the rate of change of the d.c. link voltage, but delay associated with d.c. link control loop may degrade the performance, and so it is useful to use information directly from the load, if this is available.

A typical control system employing a current-forced scheme is shown in Fig.3-1. The amplitude of the reference current, $I_{sm}$, is the summation of signals from two control sources: one is the power demand of the machine (load signal); in the other, feedback loop, a PI control is used to hold the d.c. link voltage constant in spite of any residual unbalance in the power-flows. Such a system may be necessary because, on the one hand, it would be difficult to design a PI controller which would be stable and possess a rapid response over the full range of loads, especially when a small d.c. link capacitance and a larger input inductance are used, but, on the other hand, it is not possible to estimate the power with sufficient accuracy. Moreover, different switching frequency between the rectifier and the inverter, the ultimate load on the rectifier, makes the load injection arrangement alone unacceptable. The stability and transient response of the d.c. link voltage control will be discussed in Chapter 5.
and the effect of injection about the load will also be shown.

The shape of the reference waveform, which is normally sinusoidal, is generated separately, and its frequency is phase-locked to the mains. A simple analogue implementation is to use a template derived from the mains. Any phase shift, which can arise if a filter is incorporated for removing harmonics from the mains, can be compensated in the circuit. Moreover, to generate a clean sinusoidal waveform, a phase-locked loop (PLL) can be used in conjunction with a sinusoidal VCO chip, such as the 8038, 2206, etc. If digital implementation is chosen it is even easier to generate a pure sinusoidal waveform: a sinusoidal waveform can be pre-calculated and stored in a ROM; only a simple look-up table instruction is needed as long as a phase signal locked to the mains is available.
3.3 Hysteresis Comparison Techniques

Two hysteresis comparison techniques are available, one employing an independent comparator in each phase, and the other based on space vectors.

3.3.1 Simple Hysteresis Comparison

The simplest way to force the input currents to track the references is to use a hysteresis comparator in each phase, as shown in Fig.3-2, where the reference is \( i_{s,j} \) and the actual current is \( i_{s,j} \) (\( j = A, B, \) or \( C \)). This method has excellent dynamic performance and can be realised at very low cost. It is therefore called a simple hysteresis comparison.

![Simple Hysteresis Controller](image)

Fig.3-2 Simple Hysteresis Controller

The technique is based on direct comparison of currents. As the current error exceeds a prescribed amount, defined by the hysteresis band \( \Delta i_h \), the output of the comparator which is the switching function \( S_j \), changes its state. Switching then takes place in corresponding phase in an attempt to restore the actual current to be the desired value.
An example of this tracking technique is shown in Fig.3-3. In Fig.3-3(a), the waveform of the current in phase A together with its reference and hysteresis windows is plotted for one cycle of the supply. The top curves in Fig.3-3(b) show these waveforms, together with the switching function $S_A$ at the expanded time scale (3.5ms - 4.5ms). The switching functions $S_B$ and $S_C$ are shown in the middle and bottom of Fig.3-3(b). It can be seen from Fig.3-3(b) that when the actual current $i_{sA}$ in phase A reaches its upper boundary, $+\Delta I / 2$ at $t = t_A$, the corresponding switching function $S_A$ changes its state from 0 to 1 and the upper switching device/diode pair in the pole A is activated "on". As a result, the derivative of $i_{sA}$ with respect to time becomes negative and the current $i_{sA}$ is forced to decrease since the terminal voltage $v_{RA}^*$, defined by Eqn.(2.10), is such that $(-v_{RA}^* + v_{sA}^*)$ is always $< 0$.

The essential condition for successful tracking, as can be seen, is that the dc link voltage must be sufficiently high for the currents to be forced in the desired direction [OOG 1987, 1988, GREEN 1989]. The minimum d.c. link voltage for hysteresis comparison technique is equal to the amplitude of the line-to-line voltage of the mains.

In a particular situation, where all the switching functions have the same value (zero or one), the terminal voltages $v_{RA}$, $v_{RB}$ and $v_{RC}$ become zero; some instantaneous values of the supply voltages which then determine the change of the currents cannot force the currents to the desired direction, so the error can reach double the hysteresis band [BROD 1985]. This can be explained by considering the simulation results shown in Fig.3-3.
Fig. 3-3  Results of the Simple Hysteresis Comparison Technique:

(a)  Line current and current reference
(b)  Waveforms of (a) and switching functions at the expanded time scale
(c)  Current error in the space plane
(d)  Spectrum of the line current
It can be seen from Fig.3-3(b) that before time $t_1$ the switching function $S_A$ is zero, forcing $i_{sA}$ to increase. As $i_{sA}$ reaches the upper boundary at time $t_1$, switching function $S_A$ changes its state from 0 to 1, so making current $i_{sA}$ decrease. At time $t_2$ the current $i_{sC}$ reaches its upper boundary, and the switching function $S_C$ changes its state to 1. The slope of the current $i_{sA}$ consequently changes, due to the coupling between the phases, though still forcing $i_{sA}$ down. At the time $t_3$ when the current $i_{sB}$ reaches its upper boundary, $S_B$ changes its state to 1, resulting in the switching function states $S_A$, $S_B$, $S_C$ all becoming 1, 1, 1. As a result, the terminal voltage $v_{RA}$ has a zero value and hence the derivative of $i_{sA}$ depends only on the instantaneous value of the supply voltage $v_{sA}$. At this moment the $v_{sA}$ is positive so the current $i_{sA}$ starts to increase, contrary to what is required. The switching will not take place at the time $t_4$ when $i_{sA}$ reaches its upper boundary because the switching state $[1111]$ already established is ineffective, and so the current $i_{sA}$ will overshoot the hysteresis band and continue to increase until $i_{sB}$ and $i_{sC}$ reach their own lower boundary at $t_5$. Then the current $i_{sA}$ starts to decrease because $v_{RA}$ has a negative value due to the state $[S S S 1] = 100$.

In summary, the simple comparison technique with three independent hysteresis comparators can force the actual currents to track their reference waveforms, even with very simple circuits, but it has the disadvantage that the current can overshoot the hysteresis band. This is true in the usual system where there is no connection between the neutral of the supply and the d.c. link, and thus the change of current in one phase is not only determined by its own switching state but is also influenced by the switching state of the other phases. Better performance, at least as far
as the quality of the input current is concerned, can be obtained by using a space vector-based hysteresis comparison technique, in which the switching in one phase will take account of state of the others, and hence the current errors can always be limited within the hysteresis band.

3.3.2 Space Vector-Based Hysteresis Comparison Techniques

The analysis above showed the reason for overshoot of the hysteresis band to be the interaction between the three phases. This interaction can easily be discussed by means of the space vector model.

To simplify matters the resistance of the input impedance is ignored, so the space vector model in Eqn. (2.26) becomes:

\[
\frac{d\hat{i}}{L_s} + \frac{V(s)}{R} = \frac{V_s}{R} \tag{3.1}
\]

Define a current error vector \( \Delta i_s \) by:

\[
\Delta i_s = i_s - i_s^* \tag{3.2}
\]

where \( i_s^* \) is the current reference vector. Substitution of (3.2) in (3.1) yields:

\[
\frac{d\Delta i_s}{L_s} + \frac{V(k)}{R} = \frac{E}{-R} \tag{3.3}
\]
where
\[ E_R = V_s - L_s \frac{d{i^*_s}}{dt} \]

\[ = V_s - L_s \frac{d(g_m V_s)}{dt} \]  \quad (3.4)

when
\[ i^*_s = g_m V_s \]  \quad (3.5)

If \( g_m \) is a constant, Eqn.(3.4) becomes:-

\[ E_R = V_s - L_s g_m \frac{dV_s}{dt} \]  \quad (3.6)

\( E_R \) represents the ideal terminal voltage vector which forces the actual current \( i_s^* \) to be the reference \( i^*_s \) without any deviation, and \( g_m \) is a variable conductance depending on the regulation of the d.c. voltage. It should be noted that \( g_m \) can be treated as a constant within the switching period because \( g_m \) varies 'slowly' with time as the consequence that the a.c. current loop is much faster than the d.c. link voltage control loop.

For the simple hysteresis comparison discussed previously, before the current vector \( i_s^* \) reaches or overshoots the hysteresis band in phase A, at point X in space plane, as shown in Fig.3-4, the switching functions have reached the state \([S_A \ S_B \ S_C] = [1 \ 1 \ 1]\), resulting in the zero vector \( V_s \) (7).

From Eqn.(3.3), \( d{i_s^*} / dt \) is then determined by \( E_R \). Due to the direction of \( E_R \) heading right, the locus of the current error vector \( i_s^* \) continues to move right until \( i_s^* \) reaches its upper hysteresis boundary at the point X.
As a result, switching function $S_A$ keeps its state 1 in an attempt to
decrease phase current $i_{sa}$ or force the $\Delta i_{s}$ to move left. However, the
zero voltage vector $V_R(7)$ has no effect on changing the direction of $\Delta i_{s}$;
the locus of the current error $\Delta i_{s}$ will move along the direction of the $E_R$,
forcing $\Delta i_{s}$ to move further right until $\Delta i_{s}$ reaches the boundaries of the
other two phases at point Y. The switching functions $S_B$ and $S_C$ then
change their states to 0 and the vector $V_R(4)$ forces $\Delta i_{s}$ to move left
because the derivative of the current error vector, $d\Delta i_{s}/dt$, is now heading
left. Therefore, the error for the simple hysteresis comparison can only
be limited inside the six-point star (shaded area), as shown in Fig.3-4.

Fig.3-4  Current Error $\Delta i_{s}$ in the Space Plane

The analysis above indicates that, as soon as $\Delta i_{s}$ reaches the boundary at
the point X, if the vector $V_R(4)$ is selected instead of $V_R(7)$, the current
error vector can be kept inside the hexagon.
3.3.2.1 a scheme with rapid response

For convenience, the hexagon region for the location of the current error vector $\Delta i_s$ is divided into six sections, marked (1) ~ (6); whereas the region for $E_R$ is also divided into six sections, marked I ~ VI, as shown in the Fig.3-5. To reduce the current error $|\Delta i_s|$, it is necessary to choose a proper $V_R(k)$ such that the corresponding $|d\Delta i_s/dt|$ has a component in the opposite direction to $\Delta i_s$. In Fig.3-5, for example, if the current $\Delta i_s$ is located in sector(6), $V_R(4)$ always provides the largest component against $\Delta i_s$ no matter where $E_R$ is located. With $\Delta i_s$ being detected in sector(1), the vector should be $V_R(6)$. So, based on this principle a rapid response to reduce the current error can be achieved by using the switching table summarized in Table 3.1.

The block diagram of this dependent hysteresis comparison is shown in Fig.3-6. With the current error in each phase being measured, the position
of $i_s$ is known. As soon as $i_s$ reaches the hysteresis boundary, represented by a hexagon in the space plane, a proper terminal voltage vector will be chosen by the Table 3.1, to force the current error vector to be inside the hexagon, and hence the current error being limited within the hysteresis band.

![Vector-Based Hysteresis Controller](image)

**Fig. 3-6 Vector-Based Hysteresis Controller**

From the results of simulation, shown in Fig.3-7, it can be seen that the input currents are limited within the hysteresis band throughout a fundamental period of the mains. Comparison of these results with those shown in Fig.3-3 for simple scheme shows that even when $i_{sA}$ does not reach its own hysteresis boundary the switching function $S_A$ can still change its state in response switching in the other phases, whereas in Fig.3-3, the switching function $S_A$ only changes its state when $i_{sA}$ reaches its boundary. Therefore the switching frequency is found to be higher than in the simpler case. This is one of the disadvantages of this scheme.

<table>
<thead>
<tr>
<th>$\Delta i_s$</th>
<th>(1)</th>
<th>(2)</th>
<th>(3)</th>
<th>(4)</th>
<th>(5)</th>
<th>(6)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_R(k)$</td>
<td>$V_R(6)$</td>
<td>$V_R(2)$</td>
<td>$V_R(3)$</td>
<td>$V_R(1)$</td>
<td>$V_R(5)$</td>
<td>$V_R(4)$</td>
</tr>
</tbody>
</table>

**Table 3.1 Switching Table for Rapid Response**
Fig. 3-7 Results of the Vector-Based Hysteresis Comparison Technique with Rapid Response:

(a) Line current and current reference
(b) Waveforms of (a) and switching functions at the expanded time scale
(c) Current error in the space plane
(d) Spectrum of the line current
3.3.2.2 a scheme with zero vector incorporation [KAZMIERKOWSKI 1989, 1991]

An improved scheme uses two three-level hysteresis comparators, yielding the values -1, 0 and 1, in the \( \alpha-\beta \) stationary frame, to incorporate a zero vector at appropriate times in order to reduce the switching frequency. Its block diagram is shown in Fig.3-8(a). The currents \( i_{sA}^*, i_{sB}^* \) and \( i_{sc}^* \) are first converted into \( i_{s\alpha} \) and \( i_{s\beta} \) components, the a.c. currents in \( \alpha-\beta \) frame. Then they are compared with their references, \( i_{s\alpha}^* \) and \( i_{s\beta}^* \). The digital output signals \( d_\alpha \) and \( d_\beta \) of two three-level comparators select the state of switching by looking up a switching table, Table 3.2, which defines the output voltage \( V_R(k) \). As illustrated in Fig.3-8(b), if the outputs of the both comparators are in the active state, -1 or 1, then the output voltage vector is exactly defined; if one of comparator outputs takes

![Diagram of three-level hysteresis comparator](image)
nonactive state, 0, the output voltage vector is selected by the second
comparator which has an active state; if both comparators have the zero state
output then the zero vector is applied. The results of simulation shown in
Fig.3-9 demonstrate that the current error is limited inside a square and
the switching frequency is reduced in comparison with the rapid scheme.

<table>
<thead>
<tr>
<th>d_a</th>
<th>-1</th>
<th>-1</th>
<th>-1</th>
<th>0</th>
<th>0</th>
<th>0</th>
<th>1</th>
<th>1</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>d_b</td>
<td>-1</td>
<td>0</td>
<td>1</td>
<td>-1</td>
<td>0</td>
<td>1</td>
<td>-1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>V_R(k)</td>
<td>V_R(1)</td>
<td>V_R(2)</td>
<td>V_R(3)</td>
<td>V_R(5)</td>
<td>V_R(0)</td>
<td>V_R(2)</td>
<td>V_R(5)</td>
<td>V_R(4)</td>
<td>V_R(6)</td>
</tr>
</tbody>
</table>

Table 3.2 Switching Table for a Three-Level Hysteresis
Comparator to Reduce the Switching Frequency

This scheme, however, has a larger amplitude of current ripple in phase B
and C than that in phase A since the current errors are limited within a
square in the space plane.

3.3.2.3 a scheme with reduction of switching frequency [NABAE 1986]

A more sophisticated space vector–based hysteresis technique can be used to
reduce the switching frequency and simultaneously keep the current error
vector to be within the hexagon. To achieve this, it is necessary to
consider E_R since the derivative of the current error, dΔi_s/dt, is
determined not only by V_R(k) but also by E_R, according to Eqn.(3.3). In
general, more than one voltage vectors V_R(k) can be chosen. The one
selected would be that which makes dΔi_s/dt both opposite Δi_s and have a
lowest amplitude during the switching period. Therefore |Δi_s| will be
reduced, but not as quickly as that in the rapid response schemes.
Fig. 3–9 Results of Vector-Based Hysteresis Comparison

with Zero Vectors Incorporation:

(a) Line current and current reference
(b) Waveforms of (a) and switching functions at the expanded time scale
(c) Current error in the space plane
(d) Spectrum of the line current
Consequently, the slope of the currents is decreased and the switching frequency is then reduced.

Fig. 3-10 Relevant Vectors for Explaining the Principle of the Vector-Based Hysteresis Comparison with Reduction of Switching Frequency

This technique is explained by considering an example shown in Fig. 3-10. If the current error $\Delta i_s$ is detected in region (6), three active vectors, $V_R(4), V_R(6),$ and $V_R(5),$ and two zero vectors, $V_R(0)$ and $V_R(7),$ are available to force $\Delta i_s$ to reduce. $V_R(4)$ is the only choice when $E_R$ is detected in region I (or VI). If $E_R$ is detected in region III (or IV) a zero vector, $V_R(0)$ or $V_R(7),$ is chosen to provide the smallest component opposite to $\Delta i_s,$ since $d\Delta i_s/dt$ is equal to $E_R$ in this situation. When $E_R$ is detected in region II (or V), the vector $V_R(6)$ (or $V_R(5)$) is chosen.

Implementation of this scheme is to replace the switching table, Table 3.1, in Fig. 3-6 by a new switching table, Table 3.3.

Comparison of the results of simulation in Fig. 3-11 and those of the rapid
control in Fig.3-7 shows that the switching frequency is reduced with this technique and the current error vector is still kept inside the hexagon.

<table>
<thead>
<tr>
<th>$E_R$</th>
<th>$\Delta I_s$</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1)</td>
<td>(2)</td>
</tr>
<tr>
<td>$V_R$ (6)</td>
<td>$V_R$ (6)</td>
</tr>
<tr>
<td>$V_R$ (6)</td>
<td>$V_R$ (2)</td>
</tr>
<tr>
<td>$V_R$ (2)</td>
<td>$V_R$ (2)</td>
</tr>
<tr>
<td>$V_R$ (7)</td>
<td>$V_R$ (3)</td>
</tr>
<tr>
<td>$V_R$ (0)</td>
<td>$V_R$ (0)</td>
</tr>
<tr>
<td>$V_R$ (4)</td>
<td>$V_R$ (7)</td>
</tr>
</tbody>
</table>

Table 3.3 Switching Table for Reduction of Switching Frequency

However, implementation of this scheme needs to detect the location of $E_R$ in addition to measuring current errors. Difficulty in detecting $E_R$ in practice, especially under transient conditions, can be seen from Eqn.(3.4), where $g_m$ is a variable dependent on the regulation of the d.c. link voltage. One method for detecting $E_R$ was suggested by A. Nabae [NABAE 1986], where the location of $E_R$ is determined by looking up a table with the entries of the sign of $d\Delta I_s/dt$ and the state of the switching functions. However, if $g_m$ is treated as a constant during the switching period, as defined by Eqn.(3.6), detecting $E_R$ becomes much easier. In fact, an adaptive strategy, in which this scheme is combined with the fast response scheme, seems to offer a better solution. During a transient state of the d.c. link regulation or, the situation where the current errors is be very large, a fast response scheme can be selected to reduce the errors rapidly.
Fig. 3-11 Results of Vector-Based Hysteresis Comparison Technique with Reduction of Switching Frequency:

(a) Line current and current reference
(b) Waveforms of (a) and switching functions at the expanded time scale
(c) Current error in the space plane
(d) Spectrum of the line current
During the steady state of the d.c. link regulation, or when the current errors are small, this scheme may be employed.

3.3.3 The Common Problem of Hysteresis Comparison Techniques

For hysteresis comparison techniques, switching of the power devices is governed by the instants when instantaneous currents reach their hysteresis boundaries. It is obvious that the switching frequency varies throughout a fundamental period of the supply since the current ripple is specified by the hysteresis band. The difficulty of making a comparison of the hysteresis techniques is to define some common bases, although the current error in the space plane, as shown from their results of simulation, can be used to judge the quality of tracking techniques. Another factor, which has been found very effective to be used as a common basis, is so-called average switching frequency. The average switching frequency is obtained by counting the switching pulses per cycle of the mains, divided by the cycle period of the mains. Comparison of the hysteresis schemes and other fixed switching frequency schemes discussed later is made possible. Fig.3-12 compares hysteresis comparison techniques, showing the average switching frequency which depends on $A_{h}\cdot L_s$. It can be seen that space vector hysteresis techniques have the higher switching frequency than the simple scheme at the specific hysteresis band. By employing the switching frequency reduction technique [see 3.3.2.3], the average switching frequency can be significantly reduced in comparison with the rapid response scheme [see 3.3.2.1]. It should be emphasized that the circuit parameters, such as the input inductance $L_s$ and the d.c link voltage $E_{dc}$, also influence the average switching frequency although they are usually chosen
Fig. 3-12 Average Switching Frequency of Various Hysteresis Comparisons

\( V_{\text{sm}} = 339.4 \text{V}, E_{\text{dc}} = 710 \text{V}, I_{\text{sm}} = 20 \text{A} \)

by considering other factors [see 7.2.2].

The instantaneous switching frequency is actually larger than the average switching and is very difficult to determine in the three-phase case. It is observed that similar to that in a single phase rectifier, the highest switching occurs around the crossover of the mains voltage [Appendix I], which is two or three times higher than the average switching frequency. It is believed that variable switching may affect the power switches adversely, and make electromagnetic interference more difficult to control.

There are, of course, several possible way of implementing a fixed switching frequency. An obvious solution to the problem is to regulate the hysteresis boundary, as proposed by A. Nabae. This can be done with a variable hysteresis boundary comparator and a switching frequency feedback loop, but the whole control system becomes more complicated.
3.4 Ramp Comparison Technique

A standard but elegant and simple approach to obtaining a fixed switching frequency is to use a so-called ramp comparison, or carrier comparison technique. The diagram of the ramp comparison technique in one phase is shown in Fig.3-13(a). A ramp comparator can be considered as producing asynchronous sine-triangle PWM with the current error as the modulating function. The current error is amplified, by an amplifier with a gain $K_i$. The output $K_i(i_{sJ} - i_{sJ}^*)$ of the amplifier is compared with a fixed-frequency triangle waveform with an amplitude $A_t$. The resultant error signal generates the switching signal (switching function) activating the power devices in the corresponding rectifier limb. A positive error $(i_{sJ} - i_{sJ}^*)$ and, hence, a positive $K_i(i_{sJ} - i_{sJ}^*)$ results in a larger terminal voltage, thus decreasing $i_{sJ}$ to its reference value.

![Diagram of ramp comparison technique](image)

To ensure intersections between the current error signal and the triangular carrier, a slope condition must satisfy:
slope of \( K_1 (i_{sJ} - i_{sJ}^*) \) < slope of triangular carrier

or,

\[
slope \ of \ K_1 (i_{sJ} - i_{sJ}^*) < 4 A f_s \tag{3.7}
\]

where \( f_s \) is frequency of the triangular carrier.

In essence, the amplifier functions as a proportional controller and hence there is a tracking error between the actual current and the current reference in steady state. With the larger gain \( K_1 \), the error will be reduced but the condition (3.7) may be breached.

\( K_1 \) is a design parameter for the ramp comparison scheme. Consider the steady state where the variables of interest are represented by their phasors, as shown in Fig.3-13(b). The rectifier produces a fundamental terminal voltage \( \tilde{V}_{rJ} \), resulting in a fundamental current \( \tilde{i}_{sJ} \) in phase \( j \), which satisfy the following equation:

\[
\tilde{V}_{sJ} = \tilde{V}_{sJ} Z_s + \tilde{V}_{rJ} \tag{3.8}
\]

where

\[
Z_s = j\omega L_s
\]

Let

\[
K_e = \frac{E_{dc}}{2 A_t} K_1 \tag{3.9}
\]

By reference to the phasor diagram in Fig.3-13(b), the terminal voltage phasor is given by [BROD 1985, MOHAN 1988]:

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$$\tilde{V}_{RJ} = K_s (\tilde{I}_{sJ} - \tilde{I}_{sJ}^*)$$  \hspace{1cm} (3.10)$$

where $\tilde{I}_{sJ}^*$ is the fundamental component of the current reference. Suppose the current reference to be locked to the supply voltage, that is:

$$\tilde{I}_{sJ}^* = g_m \tilde{V}_{sJ}$$  \hspace{1cm} (3.11)$$

The following equation can be derived from Eqns.(3.8) to (3.11):--

$$\tilde{I}_{sJ} = \frac{1 + K_s g_m}{Z_s + K_s} \tilde{V}_{sJ}$$

$$= \frac{1 + K_s g_m}{K_s + j\omega L_s} \tilde{V}_{sJ}$$  \hspace{1cm} (3.12)$$

The current error equation is given by:-

$$\Delta \tilde{I}_{sJ} = \tilde{I}_{sJ} - \tilde{I}_{sJ}^*$$

$$= \frac{1 - g_m Z_s}{Z_s + K_s} \tilde{V}_{sJ}$$

$$= \frac{1 - j\omega L_s g_m}{K_s + j\omega L_s} \tilde{V}_{sJ}$$  \hspace{1cm} (3.13)$$

From (3.13) and (3.12), the amplitude of the current error and the current phase shift from the reference are obtained:-
\[ |\Delta I_{sJ}| = |\tilde{I}_{sJ} - \tilde{I}_{sJ}^*| = \sqrt{\frac{1 + (\omega L_s g_m)^2}{K_s^2 + (\omega L_i)^2}} V_{sm} \]

\[ = \frac{V_{sm}}{K_s} \quad \text{(3.14)} \]

and,

\[ \xi = \angle \tilde{V}_{sJ} - \angle \tilde{I}_{sJ} = \arctg \frac{\omega L_s}{K_s} \quad \text{(3.15)} \]

where \( V_{sm} \) is the amplitude of the phase-neutral voltage of the mains.

It can be seen from Eqns.(3.14) and (3.15) that as \( K_s \) decreases (either \( K_I \) decreases or \( A_t \) increases) the current error and current phase shift will increase; this contradicts the condition (3.7) where a small \( K_s \) is required. In the normal situation, when \( K_s \) is chosen to satisfy condition (3.7), the phase shift is negligible, typically several degrees, but the amplitude error can be significant. For example, for a 415V (r.m.s.) supply and a rectifier drawing 35A (r.m.s.) from the mains, and with other parameters \( E_{dc} = 710V, K_I = 0.2, A_t = 1 \), the error in amplitude, according to Eqn.(3.14), is 4.8A, about 10% of the rated current, whereas the error in phase is 1°, which is quite negligible. However, the amplitude error is actually compensated by altering the amplitude of the current reference through the regulation of the d.c. link voltage. To compare with the other schemes discussed before, the results of simulation are shown in Fig.3-14, where the switching frequency is 3.3KHz, which is equivalent to the average frequency of the simple hysteresis comparison scheme, as shown in Fig.3-3.
Fig. 3-14 Results of the Ramp Comparison Technique:

(a) Line current and current reference
(b) Waveforms of (a) and switching functions at the expanded time scale
(c) Current error in the space plane
(d) Spectrum of the line current
In abnormal condition, multiple crossings of the ramp by the current error may occur when the time rate of change of the current error (multiplied by a constant \( K_1 \)) becomes greater than that of the ramp, i.e. the condition (3.7) being breached. The controller is then functioning like a normal hysteresis comparator and the switching is then governed by the hysteresis band. It is also possible to incorporate a low-pass filter after the amplifier, to remove the switching ripple, before the error signal being compared with the triangular carrier. This will help the intersections between the two signals.

It should be noted that the ramp comparison requires a higher d.c. link voltage than simple hysteresis comparison to ensure the rectifier not to be over modulated. The modulation index is found from:

\[
m = \frac{K_1 \left( \frac{\tilde{I}_{s,j} - \tilde{I}_{s,j}^*}{A_t} \right)}{E_{dc}}
\]  

(3.16)

Substituting Eqn.(3.14) in Eqn.(3.16) yields:

\[
m \approx \frac{2 \left( \frac{V_{sm}}{E_{dc}} \right)}{V_{sm}}
\]  

(3.17)

which implies that \( E_{dc} \) has to be higher than \( 2 \frac{V_{sm}}{V_{sm}} \) to satisfy \( m < 1 \), that is, the minimum d.c. link voltage for the ramp comparison is 15.5% higher than that with the simple rectifier. It will be shown in the next chapter this requirement of the d.c. link voltage is the same as that for the voltage-forced schemes if the sinusoidal PWM is employed.
3.5 Predictive Control Technique

Although the ramp comparison provides advantages of a constant switching frequency and simple implementation, it has the problem of the inherent error in amplitude and phase. A predictive current control scheme can overcome these difficulties.

The principle of the predictive technique is illustrated in Fig. 3-15. The actual currents are sampled at a constant rate. A suitable voltage vector, $V_R^*(n)$, is then calculated, such that it will force the currents to track the references at the next sampling instant. The required voltage vector $V_R^*(n)$ at the $n$-th sampling instant is obtained by using a discrete form of Eqn. (3.1) and setting the current vector $i_s(n+1)$ in the $(n+1)$-th sampling instant to be equal to the current reference vector $i_s^*(n+1)$, that is:

$$V_R^*(n) = V_R(n) - L_s \frac{d}{dt} i_s^*|_{t=n}$$
\[
\begin{align*}
V_s(n) &= V_s(n) - \frac{i_s(n+1) - i_s(n)}{T_s} \\
&= V_s(n) - \frac{L_s}{T_s} i_s(n+1) + \frac{L_s}{T_s} i_s(n)
\end{align*}
\] (3.18)

where \(T_s\) is sampling period, usually equal to the switching period.

Since the \(V_s(k)\) can take only one of the eight states, pulse width modulation has to be used to realise vector \(V_s^*(n)\) as a combination (weighted in time) of the two most appropriate vectors. The detail of the space-vector modulation technique will be discussed in section 4.4.2

Implementation of the predictive control needs a calculation based on Eqn.(3.18) together with the appropriate modulation. Usually, a microprocessor based system is used. It is obvious that the actual currents lag the current references by at least one sample period and probably even longer, due to calculation delay. The response is thus likely to be slower than in any of the hysteresis schemes. In addition, the current ripple cannot be explicitly specified as with hysteresis schemes. However, because the rectifier is switched at a fixed frequency the predictive control provides well-define switching harmonics which should be easy to remove, and there is no inherent error in amplitude or phase.

Fig.3-16 shows the results of simulation using standard space vector modulation techniques [DEPENBROCK 1987, HOLTZ 1983, TOROK 1983]. It can be seen that the amplitude of the current ripple is not only not limited, but it is comparatively larger than that of the hysteresis controller being
Fig.3-16 Results of the Predictive Technique with Standard Space Vector Modulation:

(a) Line current and current reference
(b) Waveforms of (a) and switching functions at the expanded time scale
(c) Current error in the space plane
(d) Spectrum of the line current
Fig. 3-17 Results of the Predictive Technique with Improved Space Vector Modulation:

(a) Line current and current reference
(b) Waveforms of (a) and switching functions at the expanded time scale
(c) Current error in the space plane
(d) Spectrum of the line current
switched at such a low frequency (here the sampling/switching frequency is chosen to be equal to 3.3 KHz in comparison with the previous schemes). A improved modulation technique [BROECK 1988] can reduce the amplitude of the current ripple at the same switching frequency as shown in Fig.3-17. However, the amplitude of the current ripple, as well as the total harmonic in the a.c. current, will be greatly reduced as the sampling frequency is increased. Fig.3-18 shows the reduction of the total harmonic distortion in the a.c. current as the sampling/switching frequency is increased. Therefore, a relatively high switching frequency is desirable, the actual value being dictated by considerations of switching loss and speed of a digital controller.

![Fig.3-18 Total Harmonic Distortion in the A.C. Current Using the Predictive Technique](image)

3.6 Comments about the Tracking Techniques

Tracking techniques can be essentially divided into three categories: hysteresis comparison, ramp comparison and predictive control. Selection
of the current control scheme depends on the specific applications.

A simple hysteresis comparison technique is easiest to implement. Its tracking performance is independent of the d.c. link voltage, providing a good performance both in steady state and in transient state of the d.c. link regulation. Its drawback, the variable switching frequency, can be overcome by adding a carrier signal with a fixed frequency before the hysteresis comparators, in order to form the ramp comparison scheme. By properly selecting the gain of the amplifier the phase error can be negligible. The amplitude error can be compensated by altering the amplitude of current reference through the feedback regulation of d.c. link voltage.

Space vector based hysteresis controller allows more accurate control in the current ripple. However, the current ripple is essentially not significant even using the simple hysteresis comparison technique, so the more refined schemes are rarely used since they require more complex circuits and have the higher average switching frequency than that with the simple case.

In applications where a fixed switching frequency is needed, the predictive control scheme will be the best choice. The implementation by means of a microprocessor system is necessary because of the calculations and space vector modulation required. This should not be seen as a disadvantage, certainly not in the case of high performance a.c. drive system where a sophisticated computer system is usually used. Then, and, especially where transputers are used, the communication between the front-end rectifier and the inverter is facilitated, in addition to any other advantages of the
computer systems [BOSE 1987]. To reduce the current ripple, it is better to employ a high sampling/switching frequency.

It should be emphasized that the value of the input inductance $L_s$ is very important in control of reversible rectifiers. To be able to operate the reversible rectifier properly, it is desirable to choose a suitable value of inductance [see section 7.2.2.2]. Generally, the input inductors are used to buffer the mains and the switching power circuit and their value should be determined by considering the quality of the a.c. current, although it will be seen in Chapter 5 that the inductance also influence the stability of the d.c. link voltage control. In order to provide the range of suitable inductances, a typical example is given in Fig.3-19, where the common basis to quantify the quantity of the a.c. current is the total harmonic distortion (THD) and the common basis to compare the hysteresis comparison techniques with the ramp comparison and the predictive scheme is the average switching frequency discussed in section 3.3.3. It should also

![Graph](image)

**Fig.3-19** Effect of the Input Inductance on the Total Harmonic Distortion in the A.C. Current Using Various Tracking Techniques

$(V_{sm} = 339.4V, E_{dc} = 710V, I_{sm} = 20A, \text{switching frequency} = 10KHz)$
be noted that for hysteresis comparisons, the hysteresis band should be correspondingly changed as the inductance $L_s$ is changed, in order to maintain the same average switching frequency. For ramp comparison, $K_I$ is selected to ensure constant switching in each case and a proper amplitude of the reference current is chosen to obtain the same a.c. current being drawn from the mains.

3.7 Summary

To control both the d.c. link voltage and the a.c. currents, it is necessary for the current-forced system to generate the a.c. current references and use a suitable tracking technique (a.c. current controller) to activate the power devices, forcing the actual currents to follow their references. This chapter discussed the principle of current-forced scheme, emphasizing on the various tracking techniques. The characteristics of the various tracking techniques have been critically compared, enabling a designer to select a suitable technique in any application.
CHAPTER 4  VOLTAGE-FORCED CONTROL SCHEMES
— INDIRECT CONTROL OF A.C. CURRENTS

4.1 Introduction

This chapter will be concerned with the other a.c. current control method - voltage-forced scheme. Basic principles of the scheme will be presented concentrating on the control of the a.c. current. Afterwards, implementations and some practical problems will be discussed.

4.2 Principle of Indirect Control of A.C. Current

The control system employing the voltage-forced scheme is shown in Fig. 4-1, where the d.c. link voltage control loop is similar to that of the current-forced scheme and an indirect control of the a.c. currents without current sensors is incorporated as an inner loop. The objective for the current control loop is to activate the power switches of the rectifier so that the fundamental components of the terminal voltages have the proper amplitude and phase with respect to the mains. To explain the principle, it is necessary to consider the relationship between these terminal voltages and the supply voltages. For clarity, a subscript \( r \) is added to represent the fundamental value. Switching harmonics injected into the mains will not be considered here.

In normal operation of the rectifier, and with switching harmonics ignored, the fundamental components of the terminal voltage \( v_{rji} \) and a.c. current
Fig. 4-1 Control System of the Voltage-Forced Scheme

The phasor diagram for one phase of a three-phase balanced system, which is shown in Fig.4-2(a), is usually used. Essentialy, there are two aspects involved in indirect control of the current, one being the means by which the required terminal voltages are calculated, and the other being the modulation method by which the required terminal voltages are generated at the terminals of the rectifier. Both of these can be achieved by using either analogue or digital techniques.
4.3 Analogue Implementation

4.3.1 Calculation

Analogue implementation consists of two stages; namely (i) generation of the modulating signals which correspond to the fundamental values of the required terminal voltages, and (ii) generation of the drive signals (switching functions) from the modulating signals.

From the phasor diagram in Fig.4-2(a), it can be seen that the required terminal voltage for the phase A is given by:

\[
\vec{V}_{RAf} = \vec{V}_{sA} - (R_s + j\omega L_s)\vec{I}_{sAf}^*
\]
\[
= (1 - R_s g_m) \vec{V}_{sA} - \omega L_s g_m j \vec{V}_{sA}
\]

where the required current \( \vec{I}_{sAf}^* = g_m \vec{V}_{sA} \).

The in-phase component in Eqn.(4.1) is given by:

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and the quadrature component by:

$$-\omega L_g V_{s_m}$$  \hspace{1cm} (4.3)

Fig.4-3 shows the generation of the modulating signal $v_{RMA}$ for the phase A. $v_{\sigma\alpha}$, $v_{\sigma\beta}$ and $v_{\sigma\gamma}$ are signals proportional to the phase-neutral voltages in phase A, B and C, respectively. The in-phase template $v_{\sigma\alpha}$ is directly generated by $v_{\sigma\alpha}$ and the quadrature template $v_{\sigma\beta}$ is formed by subtracting $v_{\sigma\beta}$ from $v_{\sigma\gamma}$ divided by a factor $\sqrt{3}$, both template signals having an amplitude of $V_{s_m}$. $I_{s_m}^*$ is the amplitude of the reference current, which comes from the output of the regulator of the d.c. link voltage, just as in the current-forced case.

![Figure 4-3: Generation of the Modulation Signal for Indirect Control of A.C. Current](image)

For convenience, let the two template signals be:
\[ v_{s\alpha} = V_{\text{al}\gamma} \sin wt \]
\[ v_{s\beta} = V_{\text{al}\gamma} \cos wt \] (4.4)

The modulating signal for the phase A should involve in-phase and quadrature components and thereby can be constructed as:

\[
v_{RMA} = (K_1 + K_2 I_{\text{sm}}^*) V_{s\alpha} - K_3 V_{s\beta} \\
= (K_1 + K_2 I_{\text{sm}}^*) V_{\text{al}\gamma} \sin wt - K_3 V_{\text{al}\gamma} \cos wt \\
= M V_{\text{al}\gamma} \sin(\omega t - \phi) \] (4.5)

where

\[
M = \sqrt{A^2 + B^2} \\
A = K_1 + K_2 I_{\text{sm}}^* \\
B = K_3 I_{\text{sm}}^* \\
\phi = \arctan(B/A)
\]

The suitable values of \( K_1, K_2 \) and \( K_3 \) should be determined so that \( v_{RMA} \) is calculated and the required \( v_{\text{RA}}^* \) can be generated when a proper modulation is applied. Without loss of generality, consider that if the rectifier is not overmodulated the fundamental component of the terminal voltage at one phase should be \( m E_{dc}/2 \) (\( m \) is the modulation index) (MOHAN 1989), thus:

\[
v_{\text{RA}} = \frac{1}{2} \frac{M V_{\text{al}\gamma}}{A_t} E_{dc} \sin(\omega t - \phi)
\]
\[ \frac{1}{2} \frac{V_{\text{sig}}}{A_t} E_{dc} \left( (K_1 + K_2 I_{sm}^*) \sin \omega t - K_3 I_{sm}^* \cos \omega t \right) \]  \hspace{1cm} (4.6) 

where \( A_t \) is the amplitude of the triangular wave carrier.

Compare Eqn.(4.6) with (4.1) and note that \( I_{sm}^* = g_m V_{sm} \). The amplifier gains \( K_1, K_2 \) and \( K_3 \) in Fig.4-3 are thereby determined:

\[
K_1 = 2 \frac{V_{sm}}{E_{dc}} \frac{A_t}{V_{\text{sig}}} \\
K_2 = -2 \frac{R_s}{E_{dc}} \frac{A_t}{V_{\text{sig}}} \\
K_3 = 2 \frac{\omega L_s}{E_{dc}} \frac{A_t}{V_{\text{sig}}} \hspace{1cm} (4.7)
\]

These gains are constant, provided that the d.c. link voltage \( E_{dc} \) is kept constant.

4.3.2 Modulations

Using modulation techniques to activate the rectifier allows the terminal voltages to be generated. Several modulation techniques are available. The frequently used modulation techniques are carrier modulation, optimum PWM (or harmonic elimination) technique and space vector modulation. Carrier modulation is suitable for analogue implementation, whereas optimum PWM and space vector modulation are usually implemented by digital systems.
4.3.2.1 sinusoidal PWM technique

The sinusoidal PWM technique is the most popular method of carrier modulation and is reviewed extensively in the literature [e.g. BOOST 1988]. The general principle is that an isosceles triangle carrier wave is compared with a sine modulating wave, and the natural points of intersection determine the switching points of power devices (represented here by switching functions). The modulation index, defined as the ratio between the peak value of the modulating wave and the peak value of the triangle carrier wave, is an important factor which governs the successful operation of modulation. Normally, it varies from 0 to 1. It should be emphasized that in the rectifier control, the modulation index is constrained by the need for the modulating wave \( v_{\text{RMA}} \) to satisfy the relation defined by the phasor diagram in Fig.4-2(a).

Substituting (4.7) into (4.5) yields:

\[
v_{\text{RMA}} = \frac{2 A_t}{E_{dc}} \left( (V_{\text{sm}} - R I_{\text{sm}}^* \sin \omega t) - \omega L I_{\text{sm}}^* \cos \omega t \right)
\]

(4.8)

The modulation index is obtained:

\[
m = \frac{2 \sqrt{(V_{\text{sm}} - R I_{\text{sm}}^*)^2 + (\omega L I_{\text{sm}}^*)^2}}{E_{dc}}
\]

\[
\approx 2 \frac{V_{\text{sm}}}{E_{dc}}
\]

(4.9)
In regeneration, the sign of $I_{sm}^*$ reverses and modulation index will be slightly increased as the current increases. To satisfy $m \leq 1$, it is necessary to have

$$E_{dc} \geq 2V_{sm} \quad (4.10)$$

For a conventional diode bridge, the d.c.link voltage is roughly equal to $\sqrt{3}V_{sm}$. Eqn.(4.10) then indicates that the d.c. link voltage should be at least 15.5% higher than that in the diode bridge, so that whatever load condition the rectifiers are not over modulated ($m \leq 1$), especially in regeneration. An alternative view of understanding Eqn.(4.10) is that provided the d.c. link voltage is set properly the modulation index will be able to take a low enough value for any load condition. This steady state requirement, which has not been addressed in the literature, should be taken into account when the sinusoidal PWM is employed in the voltage-forced schemes. For example, for a 415V (r.m.s.) three-phase supply, if the input inductance $L_s = 4mH$, the d.c. link voltage $E_{dc}$ has to be set higher than 678V in order to satisfy $m \leq 1$. Fig.4-4 shows the results where $E_{dc} = 680V$ and the amplitude of the input current, $I_{sm}^*$, is 50A. In regeneration, the modulation index is slightly larger than that in rectification, but in both cases, the rectifier is not over modulated, resulting in a good current waveform. If the d.c. link voltage $E_{dc}$ is set to be 600V, the resultant modulation index is increased to 1.13 in an attempt to create sufficiently high terminal voltages to satisfy relation defined by Fig.4-2(a), and the rectifier is then over modulated. Fig.4-5 shows the results, with the consequent distortion in input currents.
Fig. 4-4 Results Using Sinusoidal PWM with a Higher D.C. Link Voltage

(a) Rectifying Mode  (b) Inverting Mode

Top: $V_{RMA}$ and Carrier Waveform;  Middle: $S_{A}$;  Bottom: $v_{SA}$ and $i_{SA}$
Fig. 4-5 Results Using Sinusoidal PWM with a Lower D.C. Link Voltage

(a) Rectifying Mode  (b) Inverting Mode

Top: $V_{rma}$ and Carrier Waveform;  Middle: $S_A$;  Bottom: $v_{sA}$ and $i_{sA}$
4.3.2.2 third harmonic injection technique

The so-called harmonic injection technique can be helpful in reducing the d.c. link voltage because it results in a flat-topped modulating waveform which allows the rectifier to generate a higher fundamental component of terminal voltages for the same modulation index. It is shown in the reference [HOULDSWORTH 1984] that the addition of one-sixth of third harmonic to the modulating signal has the effect of reducing the peak value of the signal waveform by a factor $\sqrt{3}/2$ without changing the amplitude of the fundamental. Thus the modulating signal expressed by Eqn.(4.5) becomes:

$$V_{RMA} = M V_{sl_t} \left( \sin(\omega t-\phi) + \frac{1}{6} \sin(3\omega t-3\phi) \right)$$ (4.11)

and has the amplitude of $\frac{\sqrt{3}}{2} M V_{sl_t}$ at $\omega t=\phi + \frac{\pi}{3}$. The modulation index is given by:

$$m = \frac{\sqrt{3}}{2} \frac{M}{A_t} = \frac{2 \sqrt{(V_{sm} - R_{u sm})^2 + (\omega L_{s sm} I_{s sm})^2}}{2 \frac{E_{dc}}{\sqrt{3}}}$$

$$\approx 2 \frac{V_{sm}}{\sqrt{3} E_{dc}}$$ (4.12)

To satisfy $m \leq 1$ requires:

$$E_{dc} \geq \sqrt{3} V_{sm}$$ (4.13)
Comparison of Eqn.(4.13) and Eqn.(4.10) shows that with the third harmonic injection the d.c. link voltage can be set 13.4% lower than with sinusoidal PWM for the same allowable modulation index. The minimum d.c. link voltage required is equal to the natural value produced in a diode bridge. In practice, the d.c. link voltage is always set sufficiently higher than the minimum value in order to manage the fluctuation in the d.c. link voltage due to the change of the load.

With the same parameters as were used in Fig.4-5, (E<sub>dc</sub> was only 600V) and with harmonic injection to reduce the modulation index to roughly 1, the result of Fig.4-6 is obtained. There is no observable distortion in the a.c. currents.

In summary, there are two conditions governing the modulation. Firstly, the terminal voltage should satisfy the relation defined by the phasor diagram shown in Fig.4-2(a), which ensures unity power factor in both rectification and regeneration. Secondly, the modulation index has to be kept less than 1 or distortion will occur; this condition will guarantee a sinusoidal waveform in a.c. currents. If either of these conditions is breached the corresponding feature will be lost. There is a minimum d.c. link voltage for which these two conditions can be satisfied. Injection of third harmonic allows reduction of the d.c. link voltage by 13.4% compared with the sinusoidal PWM, but the hardware needed for implementation is more complex.
Fig. 4-6 Results Using Harmonic Injection with a Lower D.C. Link Voltage

(a) Rectifying Mode
(b) Inverting Mode

Top: $V_{RMA}$ and Carrier Waveform; Middle: $S_A$; Bottom: $v_{sa}$ and $i_{sa}$
4.3.3 Practical Problems of Implementation

An inherent problem for analogue implementation is the accuracy. One notices in Eqn.(4.7) that the performance of the input current control depends on accurate calculations of the gains, $K_1$, $K_2$, and $K_3$ which are all related to the d.c. link voltage. If the P controller is used to regulate the d.c. link voltage, an inherent voltage error in steady state has to be compensated. Usually, the output of the triangular carrier generator is multiplied by d.c. link voltage before it is compared with the modulating signal, in order to compensate the voltage error. For a PI controller, there is no error in d.c. link voltage in steady state and the gains can be determined by using the reference d.c. link voltage in calculations. In transient state, some errors are still inevitable.

The more important factor for voltage-forced schemes is the stability of the d.c. link voltage control. To obtain a wide range of stability, it is imperative that a differential compensation be added in the control circuit, which will be explained in Chapter 5. In practice, the gain $K_2$ is changed to:

$$K_2 = -2 \frac{R_s}{E_{dc}} \frac{A_t}{V_{sig}} \left[ 1 + \frac{L_s}{R_b} S \right]$$

where $S = d/dt$, the differential operator. As can be seen here, in addition to implementing a perfect compensation, introduction of the differentiator will cause noise problem, as it is well known.
4.4 Digital Implementation

There are at least two major advantages in implementing voltage-forced scheme digitally. Firstly, the required terminal voltage can be more accurately calculated. Secondly, it is then possible to implement more sophisticated control algorithms, such as space vector modulation techniques and dynamic compensation for stability.

Before discussing digital implementation, it is necessary to extend some concepts mentioned at the beginning of this chapter. As stated before, if switching harmonics are ignored, the terminal voltages and input currents can be represented by their fundamental components. Therefore, the fundamental component vectors of the terminal voltage and input current, $V_{RF}$ and $i_{sf}$, can be defined by correspondingly replacing their fundamental components in Eqns.(2.25) and (2.23) and both of them rotate at the angular speed $\omega$ on the space plane, synchronous with the supply voltage vector $V_s$.

Fig.4-2(b) illustrates steady state relationship of the input variables on the space plane at an arbitrary instant. Note the difference between this diagram and phasor diagram in Fig.4-2(a). The former shows the relationship between the voltage and current vectors which are defined to represent three-phase quantities in a convenient way, whereas the phasor diagram shows the relationship between the sinusoidal variables (as functions of time) in one phase. The required $V^*_RF$, which "forces" the current $i_{sf}$ to be aligned with the supply voltage $V_s$ in both rectification and regeneration, can be obtained by calculation based on this diagram. A proper PWM modulation technique should be chosen to implement $V^*_RF$. The
power transferred between the supply and the d.c. link can be controlled by \( V_{Ls} \), the voltage vector across the input inductors.

### 4.4.1 Calculation

For calculation, a d-q rotating model is easily used. If the d-axis is fixed at the supply voltage vector \( V_s \), as shown in Fig.4-2(b), the required fundamental of the terminal voltage \( V^*_{rf} \) can be calculated as follow:

First, in the d-q frame, the direct-axis component of \( V^*_{rf} \) is given by:

\[
V^*_{rf} = - \frac{3}{2} \frac{V}{\sqrt{2}} - \frac{3}{2} \frac{R}{\sqrt{2}} \frac{I}{\sqrt{2}} \]  \hspace{1cm} (4.15)

and, the quadrature-axis component is:

\[
V^*_{rq} = - \frac{3}{2} \frac{1}{\sqrt{2}} \frac{L}{\sqrt{2}} \]  \hspace{1cm} (4.16)

Then, the dc quantities \( V^*_{rf} \) and \( V^*_{rq} \) are converted to the \( \alpha-\beta \) frame with the help of \( \cos \theta \) and \( \sin \theta \) signals generated from a phase detector:

\[
\begin{align*}
V^*_{ref} &= \cos \theta \ V^*_{rf} - \sin \theta \ V^*_{rq} \\
V^*_{ref} &= \sin \theta \ V^*_{rf} + \cos \theta \ V^*_{rq}
\end{align*}
\]  \hspace{1cm} (4.17)

Finally, the required \( V^*_{rf} \) is obtained:
4.4.2 Space Vector Modulation Techniques

The way of realising $V^*_{Rf}$ is to use one of the digital PWM techniques, widely used in inverter control. If the switching frequency is high enough, $V^*_{Rf}$ can be treated as a constant within the switching period and may be converted into an analogue signal which is compared with a triangle carrier waveform. The intersections determine the switching functions. The other approach is to use optimum PWM technique. In this method, the precalculated PWM waveforms are stored as bit streams of 1s and Os in the ROM. To obtain the proper drive signals (switching functions) the microprocessor selects one of the stored waveforms by writing the appropriate byte to a latch that is connected to the address pins of the ROM and the pulse widths are generated in the time domain with the help of down-counters. The undesirable harmonics can be eliminated by programing the precalculated waveforms.

Another effective modulation method, so-called space vector modulation technique [HOLTS 1983, DEPENBROCK 1987, BLOCK 1988, HABETLER 1991], is recommended here since it has the advantages of improved harmonic performance, especially at low d.c. link voltage, and improved transient performance at any operating condition, in comparison to carrier comparison
PWM techniques.

In every sampling period, which normally equals a switching period, the required terminal voltage $V_{\text{RF}}^*$ is calculated based on the method mentioned above. $V_{\text{RF}}^*$ might be located in any position on the space plane at one specified sampling period because it rotates at the angular speed of the supply. It has been mentioned that the rectifier can produce only six active terminal voltage vectors and two zero voltage vectors. To obtain the required terminal voltage $V_{\text{RF}}^*$, the two nearest active vectors are chosen plus proper zero vectors, and switching modulated between them to give the desired time average. The conduction times of the rectifier switches are modulated according to the amplitude and the angle of $V_{\text{RF}}^*$.

<table>
<thead>
<tr>
<th>Sector</th>
<th>Zero Voltages</th>
<th>Active Voltages</th>
<th>Zero Voltages</th>
</tr>
</thead>
<tbody>
<tr>
<td>I</td>
<td>$V_2 (0)$</td>
<td>$V_2 (4)$</td>
<td>$V_2 (7)$</td>
</tr>
<tr>
<td>II</td>
<td>$V_2 (7)$</td>
<td>$V_2 (6)$</td>
<td>$V_2 (2)$</td>
</tr>
<tr>
<td>III</td>
<td>$V_2 (0)$</td>
<td>$V_2 (2)$</td>
<td>$V_2 (7)$</td>
</tr>
<tr>
<td>IV</td>
<td>$V_2 (7)$</td>
<td>$V_2 (3)$</td>
<td>$V_2 (0)$</td>
</tr>
<tr>
<td>V</td>
<td>$V_2 (0)$</td>
<td>$V_2 (1)$</td>
<td>$V_2 (7)$</td>
</tr>
<tr>
<td>VI</td>
<td>$V_2 (7)$</td>
<td>$V_2 (5)$</td>
<td>$V_2 (0)$</td>
</tr>
</tbody>
</table>

Table 4.1 Switching Table for Space Vector Modulation

The angle $\gamma$ obtained from (4.18) determines the sector of the space plane where the $V_{\text{RF}}^*$ should lie:

$$N = \text{INT} \left( \frac{\gamma}{\frac{\pi}{3}} \right) + 1$$

(4.19)
where \( N \) ( = I, II, ...VI) is the sector number, as identified in Fig.3-5, and \( \text{INT} \) means integer part of the expression. The active voltage vectors for modulation are thereby determined by knowing the position of \( V^*_R \), as summarized in Table 4-1.

The modulation is achieved by using two adjacent active voltage vectors with appropriate duty cycle for the power switches. Fig.4-7 shows an example of implementation of the space vector modulation. In one switching period, the rectifier is switched from \( V^*_R(4) \) to \( V^*_R(6) \) with the duty cycle determined by the value of \( V^*_RFX \) and \( V^*_RFY \). By referring to Fig.4-7(a), the voltages \( V^*_RFX \) and \( V^*_RFY \) are calculated by:

\[
V^*_RFY = \frac{2}{\sqrt{3}} |V^*_R| \sin \gamma \\
V^*_RFX = |V^*_R| \cos \gamma - \frac{1}{2} V^*_RFY
\]

The time durations of the active vectors and the zero voltage vectors are given by:

\[
t_x = \sqrt{\frac{3}{2}} \frac{V^*_RFX}{E_{dc}} T_s \\
t_y = \sqrt{\frac{3}{2}} \frac{V^*_RFY}{E_{dc}} T_s
\]

\[
t_{z1} = t_{z2} = (T_s - t_x - t_y) / 2
\]
where $T_s$ is the switching period and $t_{z1}$ and $t_{z2}$ are the times for incorporating zero vectors $V_R(0)$ and $V_R(7)$.

Fig. 4-7 Switching Patterns of Space Vector Modulation

(a) Adjacent Active Vectors

(b) Switching Pattern of Standard Modulation

(c) Switching Pattern of Improved Modulation
In a standard modulation technique, as shown in Fig.4-7(b), time spent on the zero voltage vectors is equally distributed at the beginning and the end of the switching period $T_s$. However, an improved modulation technique can reduce the ripple content of the input current, as was demonstrated in section 3.5 where the improved space vector modulation technique was applied to the predictive current-forced scheme. This is achieved by modifying the switching pattern so that it is split into two mirror images centred around the half cycle time ($T_s/2$), as shown in Fig.4-7(c). In comparison to the standard modulation in Fig.4-7(b), the improved modulation activates the switches twice per switching cycle, which improves the controllability of the a.c. currents for the same switching frequency.

4.4.3 Discussion

4.4.3.1 Modulation index and d.c. link voltage

With the condition $t_x + t_y + t_z_1 + t_z_2 = T_s$, it can be proved that the required terminal voltage vectors obtainable reside inside the hexagon formed by the six active voltage vectors, shown in dotted line in Fig.3-5. Space vector modulation technique has the same effect as third harmonic injection, that is, the d.c. link voltage can be reduced by 13.4% relative to sinusoidal PWM technique, since the maximum fundamental of the terminal voltage can be 15.5% higher when d.c. link voltage is constant [BROECK 1988]. Fig.4-8 shows the simulation results where the $E_{dc} = 600V$. A good a.c. current waveform is still obtained, as that in Fig.4-6.
Fig. 4-8 Results of Using Standard Space Vector Modulation Technique with a Lower D.C. Link Voltage (Switching Frequency is 10KHz)

Top: $v_{sA}$ and $i_{sA}$; Bottom: Switching Function $S_A$

4.4.3.2 sampling frequency/switching frequency

With space vector modulation, the calculated terminal voltage is updated only once per switching period when the sampling period is selected to be equal to switching period. This is particularly important for a rectifier operating at low switching frequency, where error is introduced by assuming that the voltage drop across the input inductors is $\omega L_s \sqrt{3 \over 2} I_{sm}'$ (specified by Eqn.(4.16)). From the results of simulation it seems that the sampling frequency should be higher than 5KHz. Thus, when sampling is
only once per switching cycle, the switching frequency should also be well above 5KHz. It is possible to sample twice, or even more times, in each switching cycle, but the resultant implementation will then be more complex and need further investigation in practice.

4.5 Summary

In this chapter, the indirect a.c. current control methods have been discussed. In addition to avoiding the use of current monitoring devices, the voltage-forced scheme has the advantage that the switching harmonics are more predictable for elimination purposes, like the ramp comparison and the predictive scheme in the current-forced scheme (section 3.4 and 3.5), since the switching frequency is fixed.

Implementation requires the calculation of the terminal voltages, followed by a proper modulation to produce the voltages across the inductors in the input lines to be in quadrature with the supply voltage. This is equivalent to forcing the power factor to be unity. The condition for good current waveform is restricted by the modulation index. For this reason, the d.c. link voltage has to be at least 15.5% higher than that in simple diode bridge. Some improvement, to reduce the d.c. link voltage, is possible by injection of third harmonic or by using space vector modulation technique. However, a more important aspect, to be discussed in the next chapter, is that the calculation of the terminal voltage produced by the rectifier is quite complicated under transient conditions, but if the simple algorithms corresponding to steady state are used the conditions for stability become very restrictive.
CHAPTER 5: STABILITY AND TRANSIENT RESPONSE OF DC LINK CONTROL

5.1 Introduction

The two previous chapters were primarily concerned with the control of the a.c. currents, which forms an inner control loop in the whole control system. Fig.3-1 and Fig.4-1 have shown the dual loop system, in the cases of voltage and current forcing respectively. In this chapter the control of the d.c. link voltage will be investigated, with emphasis on stability and transient behaviour.

The next section is the basic principles of power flow control, leading on to discussion of the d.c. link voltage feedback control, together with injection of load information. Then, the stability of the d.c. link control will be investigated, with the transient response being analysed by means of the simulation.

5.2 Control of Power Flow

On considering the control system diagrams shown in Fig.3-1 and Fig.4-1, it is seen that the outer loops which hold the d.c. link voltage to constant are identical. Control of the power flow is carried out by controlling d.c. link voltage, perhaps also with injection of information about the load. For control of the d.c. link voltage, the system consists of a voltage sensor, a low-pass filter to eliminate the switching harmonics, and a regulator. In response to a change in the load the d.c. link voltage
varies, and the output of the regulator which defines the amplitude of the a.c. currents consequently changes value and/or sign. The input power is therefore regulated to correct the change of the d.c. link voltage, and so match the load requirement. It might seem that a more direct way of controlling the power flow is to provide the correct amplitude of the a.c. currents directly from an exact knowledge of load requirement. Better is to introduce a load injection loop into the feedback, as shown in Fig.3-1 and Fig.4-1, which allows faster response without excessive voltage variations; moreover, the value of d.c capacitance can also be reduced.

Accurate estimation of load requirement needs further investigation, but one possibility, if the reversible rectifier is combined with an induction machine drive system, is to estimate the output power to the inverter by:-

\[ P_{\text{out}} = \omega_e T_e^* + P_{\text{add}} \]

where \( \omega_e \) is the synchronous angular frequency, \( T_e^* \) is the torque demand and \( P_{\text{add}} \) is additional power losses, including power losses in the switching devices in the inverter and other additional losses. The required amplitude of the reference current can be calculated from:-

\[ I_{sm}^* = \frac{P_{\text{out}}}{\frac{3}{2} V_{sm}} \]

It is obvious that a control loop of the dc link voltage is always essential even there is a load injection loop. This is because of two facts. First, in practice, it is difficult to obtain accurate load requirement. Second,
differences in switching strategies and frequencies between rectifier and inverter make an instantaneous power match impossible. The dc link has to be used to handle the residual unbalance between the input and the load.

5.3 Conditions for Stability Analysis

The mathematical models derived in Chapter 2 describe the dynamic behaviour of a voltage-sourced rectifier. The discrete nature of the models makes them difficult to use in stability analysis. An effective method is to derive a small-signal model by considering small perturbations about the operating point in the nonlinear power balance equation; the system stability of this model is then analysed. This small-signal model is always valid in analysis of stability although it is unable to describe the transient behaviour when the fluctuations in the variables about the operating point are great.

The basic assumption made in deriving power balance equations is that the switching frequency is above the bandwidth of the dc link control loop, that is, the discrete-time nature of the rectifier can be ignored. With the current-forcing in the inner loop, the assumption that the discrete-time nature can be ignored implies that the actual a.c. currents follow their references exactly, so that the a.c. currents are perfect sinusoidal waveforms without phase shift with respect to the mains voltages. If the voltage-forced scheme is used as the inner loop, the assumption is equivalent to the pulse-width-modulated terminal voltages being replaced by their fundamental components.
5.4. Stable Region for Current-Forced Scheme

5.4.1. Rectifying Operation Mode

5.4.1.1 small-signal model

To study the current-forced control system, it is assumed that the input (a.c.) currents track their references exactly and the mains supply is balanced. In this case the instantaneous input power can be expressed in terms of the amplitude of the currents [Appendix.II], and the equation relating input power to output (d.c) power plus the rate of change of energy stored in the circuit reactances is easily written, as:-

\[
\left( V_s I_s - R_s I_s^2 - L_s I_s \frac{dI_s}{dt} \right) = C \frac{dE_{dc}}{dt} + E_{dc} i_{out}
\]

(5.1a)

where

\[
V_s = \sqrt{\frac{3}{2}} V_{sm}, \quad I_s = \sqrt{\frac{3}{2}} I_{sm}
\]

The equation is non-linear in the variables of interest, namely \(E_{dc}, I_s\), and \(i_{out}\). To proceed further small deviations about a fixed operating point are studied. The circuit parameters and the input voltage are supposed to be invariant. Then, replace \(d/dt\) by \(S\), and write:-
\[ V_s = V_{so} + \Delta V_s \]
\[ I_s = I_{so} + \Delta I_s \]

\[ E_{dc} = E_{dc0} + \Delta E_{dc} \]
\[ i_{out} = I_0 + \Delta I_o \]

Here subscript \( o \) refers to the operating point, and \( \Delta \) denotes a perturbation. The following can then be derived:

\[ AE_{dc} = G(s) \Delta I_s - G_1(s) \Delta I_o \]  \hspace{1cm} (5.3a)

where

\[ G(s) = \frac{-a_1 S + a_0}{S + \frac{1}{\tau_c}} \]
\[ G_1(s) = \frac{1}{S + \frac{1}{\tau_c}} \]

\[ a_1 = \frac{L_s I_{so}}{C E_{dc0}} \]
\[ a_0 = \frac{V_{so} - 2 R_s I_{so}}{C E_{dc0}} \]

\[ \tau_c = R_0 C \]
\[ R_0 = \frac{E_{dc0}}{I_0} \]

Eqn.(5.3a) shows the relationship between the variables of interest, i.e. dc link voltage \( \Delta E_{dc} \), input current \( \Delta I_s \) and load current \( \Delta I_o \). The block diagram of the small signal model of the closed-loop control system is shown in Fig.5-1. Note that the reference value for the variation in the dc link voltage, \( \Delta E_{dc}^* \), is zero, and the current reference \( \Delta I_s^* \) is assumed to equal to the actual current \( \Delta I_s \). The transfer function between the dc link voltage \( \Delta E_{dc} \) and the load current \( \Delta I_o \) can be obtained:
Please note that the text is not fully visible due to the page being cropped. However, the text appears to be discussing the small signal model in control systems, involving the manipulation of characteristic equations and stability analysis. The document refers to a block diagram (Fig. 5-1) of the small signal model and presents an equation for stability analysis:

\[
\frac{\Delta E_{dc}}{\Delta I_o} = -\frac{G_I}{1 + G_c G_f G} = -\frac{c_2 S^2 + c_1 S}{S^3 + b_2 S^2 + b_1 S + b_0}
\]

where

\[
G_c(s) = K_p \left(1 + \frac{1}{T_1 S}\right) \quad \text{(PI controller)}
\]

\[
G_f(s) = \frac{K_{df}}{1 + T_{df} S} \quad \text{(Filter)}
\]

\[
K = \frac{K_p K_{df}}{T_{df}}, \quad c_2 = \frac{1}{C}, \quad c_1 = \frac{1}{C T_{df}}, \quad b_0 = K \frac{a_0}{a_1}
\]

\[
b_1 = \frac{1}{T_{df} \tau_c} + K \left(\frac{a_0}{a_1} + \frac{a_1}{T_1}\right), \quad b_2 = \frac{1}{\tau_c} + \frac{1}{T_{df}} + K a_1
\]

5.4.1.2 Stability analysis

To investigate the stability further, the characteristic equation of Eqn. (5.4a) is manipulated algebraically to a form:--
\[
1 + K a_1 \frac{(S + z_1)(-S + z_2)}{(S + p_1)(S + p_2)(S + p_3)} = 0 \tag{5.5a}
\]

where

\[
z_1 = \frac{1}{T_1}, \quad z_2 = \frac{a_0}{a_1}, \quad p_1 = 0, \quad p_2 = \frac{1}{\tau_c}, \quad p_3 = \frac{1}{T_{dr}}
\]

\(z_1\) and \(p_j\) are zeros and poles of the "open-loop" transfer function, respectively \((i = 1, 2\) and \(j = 1, 2, 3\)). Typical positions of these poles and zeros and several root loci with different time constant \(T_1\) are sketched in Fig.5-2, based on the accurate calculations. The loci start from the poles

\begin{align*}
& (a) \quad \text{when } 1/T_1 \gg 1/\tau_c \\
& (b) \quad \text{small } 1/T_1 \text{ but } 1/T_1 > 1/\tau_c \\
& (c) \quad \text{small } 1/T_1 \text{ but } 1/T_1 < 1/\tau_c
\end{align*}

Fig.5-2 Sketches of Root Loci of Current-Forced Scheme (Rectification)
and move approaching to the zeros as the proportional gain $K_p$ of the PI controller increases. Note that the gain $K a_0$, pole $p_2$ and zero $z_2$ vary as the steady-state operating point shifts. $z_1$ and $p_3$ are inversely proportional to the time constant of the PI controller and the time constant of the dc voltage filter, respectively. Usually, the pole $p_2$ lies very near the origin and zero $z_2$ far away the origin. In one case, with the condition $1/T \gg 1/\tau_c$, as shown in Fig.5-2(a), as the gain $K_p$ is increased and $p_1$ and $p_2$ first move along the axis to coalesce, and then diverge as a conjugate pair of poles moving off the real axis, and eventually into the right half plane. Fig.5-2(b) and (c) also show the several different loci as the time constant $T_1$ takes different values, both providing a wider stable region than that in Fig.5-2(a). An accurate root-locus diagrams of the Fig.5-2(a), which is shown in Fig.5-3, demonstrates that effect of the input resistance $R_s$ on the root-loci is very small so that it can be ignored.

![An Accurate Root-Locus Diagram for Current-Forced scheme](image)

**Fig.5-3** An Accurate Root-Locus Diagram for Current-Forced scheme

(Rectification)

$V_{SM} = 339.4V$, $E_{dc} = 710V$, $L_s = 4mH$, $C = 1250\mu F$, $I_0 = 20A$

$K_{df} = 1$, $T_{df} = 0.002$ 

$T_1 = 0.004$
The values of some parameters, such as filter time constant, input inductance, and d.c. capacitance, are selected from general considerations. As soon as these have been fixed the proper parameters of the PI controller can be chosen to obtain stable control. The stable condition can be examined more formally by using the Routh-Hurwitz criterion, which yields expressions for selecting the parameters $K_p$ and $T_i$ of the PI controller, as follows:

\[
K_p < \frac{R_o}{K_d f X^2 A_o} \left( \frac{T_d f}{\tau_c} + 1 \right) \quad (5.6a)
\]

\[
T_i > \frac{K_p K_d f X^2 A_o \left( 1 + \frac{T_d f}{\tau_c} - K_p K_d f \frac{X^2}{R_o A_o} + \frac{T_d f}{\tau_L A_o^2} \right)}{R_o \left( 1 + \frac{T_d f}{\tau_c} - K_p K_d f \frac{X^2}{R_o A_o} \right) \left( \frac{1}{\tau_c} + \frac{K K_d f X^2}{R_o A_o \tau_L} \right)} \quad (5.7a)
\]

where

\[
A_o = \frac{E_{dc0}}{V_{s0}}, \quad \tau_L = \frac{L_s}{R_o}, \quad X^2 = \frac{L_s}{C}
\]

The load "resistance", $R_o$, is of particular significance. The stable regions defined by Eqn.(5.6a) and (5.7a) may be presented graphically against the variable $R_o$ for design purpose.

5.4.2 Regenerative Operation Mode

5.4.2.1 small-signal model
Just as in the rectification mode, the power balance equation in regeneration, can be found as:

\[
\left( V_s I_s + R_s I_s^2 + L_s I_s \frac{dI_s}{dt} \right) = -C E_{do} \frac{dE_{dc}}{dt} + E_{dc} i_{out}
\]

(5.1b)

The small-signal perturbation equation related to $\Delta E_{dc}$, $\Delta I_s$ and $\Delta I_o$ is:

\[
\Delta E_{dc} = -G(s) \Delta I_s + G_1(s) \Delta I_o
\]

(5.3b)

where

\[
G(s) = \frac{a_1 S + a_0}{S - \frac{1}{\tau_c}}, \quad G_1(s) = \frac{1}{S - \frac{1}{\tau_c}}
\]

\[
a_1 = \frac{L_s I_{s0}}{C E_{dc0}}, \quad a_0 = \frac{V_{s0} + 2 R_s I_{s0}}{C E_{dc0}}
\]

Also, the closed-loop transfer function is:

\[
\frac{\Delta E_{dc}}{\Delta I_o} = \frac{c_2 S^2 + c_1 S}{S^3 + b_2 S^2 + b_1 S + b_0}
\]

(5.4b)

where

\[
c_2 = \frac{1}{C}, \quad c_1 = \frac{1}{C T_{df}}, \quad b_0 = K \frac{a_0}{a_1}
\]

\[
b_1 = -\frac{1}{T_{df} \tau_c} + K \left( a_0 + \frac{a_1}{I_i} \right), \quad b_2 = -\frac{1}{\tau_c} + \frac{1}{T_{df}} + K a_1
\]

The "open-loop" transfer function can be found, as:
\[1 + K a \frac{(S + z_1)(S + z_2)}{(S + p_1)(S - p_2)(S + p_3)}\]  \hspace{1cm} (5.5b)

5.4.2.2 stability analysis

In contrast to the pole-zero configuration in rectification, the pole \(p_2\) now moves to the right-half plane, close to the origin, while \(z_2\) moves to the left-half plane but still far away from the origin. The rough sketch of the root-locus shown in Fig.5-4(a) demonstrates that the locus originating from \(p_1\) and \(p_2\) breaks away from the real axis in the right-half plane, and enters the left-half plane as the gain increases. Eventually, this locus will coalesce at the real axis, and then converges as two negative real poles, one approaching the zero \(z_2\), and the other tending to infinity along the negative axis. The other segment starts from \(p_3\) and finishes at \(z_1\). At first sight
it might appear that the system is unstable when the proportional gain is small, but the accurate diagram in Fig.5-4(b) shows that normally the locus shifts very rapidly to the left half plane as the gain increases, so demonstrating the large margin of stability in practice.

Likewise, the inequalities needed for selecting the parameters of the PI controller in this mode can be derived as:

\[
K_p > \frac{R_o}{K_{df} X^2 A_0} \left( \frac{T_{df}}{\tau_c} - 1 \right) \quad (5.6b)
\]

\[
T_i > \frac{K_p K_{df} X^2 A_0 \left( -1 + \frac{T_{df}}{\tau_c} - K_p K_{df} \frac{X^2}{R_o A_o} + \frac{T_{df}}{\tau_L A_o^2} \right)}{R_o \left( 1 - \frac{T_{df}}{\tau_c} + K_p K_{df} \frac{X^2}{R_o A_o} \right) \left( -1 + \frac{K_p K_{df} X^2}{R_o A_o \tau_L} \right)} \quad (5.7b)
\]

5.4.3 An Example

To illustrate the applications of Eqns.(5.6)-(5.7), an example is given, showing the design of the PI controller in a current-forced system to achieve a stable response.

After the circuit parameters have been selected [see section 7.2.2], the Eqns.(5-6) can be presented graphically in Fig.5-5. In this example, \( E_{dc} = 65V, V_{in} = 33.9V, L_s = 4mH, C = 1250\mu F, K_{df} = 1 \) and \( T_{df} = 0.002 \) [ZHANG, 1992]. The load current, \( I_o \), is chosen quite arbitrarily to be about 5A, so making \( R_o \) equal to 13Ω. The proportional gain of the PI
controller can be first selected since all the parameters in Eqn.5.7(a) have now been determined by the power system design. The point A on Fig.5-5, corresponding to $K_p = 1$, is in the stable region for rectification and regeneration; the range of gain for instability when regenerating is so small, just near the origin, that is not illustrated here. With $K_p$

![Fig.5-5 Stable Region for Proportional Gain $K_p$ (Rectification)](image)

(a) $L_s = 1\text{mH}$, (b) $L_s = 4\text{mH}$, (c) $L_s = 8\text{mH}$

determined, the graphs of the Fig.5-6(a) and (b) are plotted in order to choose the time constant of the PI controller. From these it can be seen that a choice such as represented by point B, $T_1 = 0.004$, will give stable response in both modes. In contrast, if point C, $T_1 = 0.002$, is selected the system will be stable only while regenerating. The results of simulation of these two selections are given in Fig.5-7. The average load current is reversed at time 0.24sec, changing the mode of operation from rectification to regeneration, and reversed again at 0.32sec, to revert to rectification from regeneration. The upper curves on the top diagrams show the d.c. link voltage which, as would be expected, overshoots when load is
removed and drops when load current is drawn again. The lower curve on the
top diagrams shows the amplitude of the current reference, the output of the
PI controller. The figures on the bottom diagrams show the phase voltage
and a.c. current in phase A. The instability is shown clearly in
Fig.5-7(b), corresponding to point C. Also shown in Fig.5-7(b) is the
distorted a.c. current arising from unstable behaviour of the d.c. link
control loop.

Fig.5-6 Stable Region for Time
Constant $T_1$

(a) Rectification

(b) Regeneration
Fig. 5-7 Results of Simulation

(a) Stable Response       (b) Unstable Response
Top Traces: $E_{dc}$ and $i^*_{sm}$; Bottom Traces: $v_{eA}$ and $i_{eA}$

5.5 Stable Region for Voltage-Forced Scheme

5.5.1 Small-Signal Model

The model to be derived for the voltage-forced scheme is slightly complicated because derivation of the power balance is not straightforward in the case of indirect control of the a.c. current. The d-q model in a rotating reference frame discussed in Chapter 2 will provide an easy route to derivation.
The switched nature of the terminal voltage $V_T$ is ignored, so allowing it to be replaced by its fundamental component $V_{Rf}$. With reference to section 2.3.5, equations representing the dynamic behaviour of the rectifier the indirect current control are give by:

\[
\frac{dI^{sd}}{dt} + R_s i^{sd} - \omega L_s i^{sq} = V_{sd} - V_{Rdf} \tag{5.8}
\]
\[
\frac{dI^{sq}}{dt} + R_s i^{sq} + \omega L_s i^{sd} = V_{sq} - V_{Rqf} \tag{5.9}
\]
\[
C E_{dc} \frac{dE_{dc}}{dt} = V_{Rdf} i^{sd} + V_{Rqf} i^{sq} - E_{dc} i_{out} \tag{5.10}
\]

The d-axis is aligned with the supply voltage vector, so therefore:

\[
\begin{align*}
V_{sq} &= 0 \\
V_{sd} &= V_s
\end{align*} \tag{5.11}
\]

In considering Fig.4-2(b) and Eqns.(4.15) and (4.16), the required $V^*_{Rf}$ in the rectifying mode can be calculated from the equation:

\[
\begin{align*}
V^*_{Rdf} &= V_s - R_s I^*_s \\
V^*_{Rqf} &= -\omega L_s I^*_s
\end{align*} \tag{5.12}
\]

where $I^*_s = \sqrt{\frac{3}{2}} I^*_{sm}$.
Considering \( V_{Rdf} = V_{Rdf}^* \) and \( V_{Rqf} = V_{Rqf}^* \), and substituting (5.11) and (5.12) in (5.8), (5.9) and (5.10) yield:

\[
\begin{align*}
\frac{di_{sd}}{dt} + R_s i_{sd} - \omega L_s i_{sq} &= R I_s^* \\
\frac{di_{sq}}{dt} + R_s i_{sq} + \omega L_s i_{sd} &= \omega L I_s^*
\end{align*}
\]

\( (5.13) \)

\[
C E_{dc} \frac{dE_{dc}}{dt} = (V_s - R_s I_s^*) i_{sd} - \omega L I_s^* i_{sq} - E_{dc} i_{out}
\]

\( (5.14) \)

A small-signal perturbation is then applied about the steady-state operating point:

\[
\begin{align*}
i_{sd} &= I_{sd} + \Delta i_{sd} \\
i_{sq} &= I_{sq} + \Delta i_{sq} \\
I_s^* &= I_{s0} + \Delta I_s \\
E_{dc} &= E_{dc0} + \Delta E_{dc} \\
i_{out} &= I_0 + \Delta I_0
\end{align*}
\]

Noting further that in the steady state, \( I_{sd} = I_{s0} \) and \( I_{sq} = 0 \), and replacing \( d/dt \) with \( S \), the following is obtained:

\[
\begin{bmatrix}
R_s + S L_s & -\omega L_s \\
\omega L_s & R_s + S L_s
\end{bmatrix}
\begin{bmatrix}
\Delta i_{sd} \\
\Delta i_{sq}
\end{bmatrix}
= \begin{bmatrix}
R_s \\
\omega L_s
\end{bmatrix}
\Delta I_s^*
\]

\( (5.15) \)

\[
\Delta E_{dc} = \frac{(V_s - R_s I_{s0}^*)}{(S + \frac{1}{\tau_c})} \Delta i_{sd} - \frac{\omega L I_s^*}{(S + \frac{1}{\tau_c})} \Delta i_{sq} - \frac{R_s}{(S + \frac{1}{\tau_c})} \Delta I_s^*
\]

\( (5.16) \)
The input current $\Delta i_{sd}$ and $\Delta i_{sq}$ as a function of $I_1^*$, can be deduced by solving Eqn. (5.15):

$$\Delta i_{sd} = \frac{\left( S + \frac{1}{\tau_s} + \omega^2 \tau_s \right)}{\tau_s \left( \left( S + \frac{1}{\tau_s} \right)^2 + \omega^2 \right)} \Delta I_1^* \tag{5.17}$$

$$\Delta i_{sq} = \frac{S}{\omega \left( \left( S + \frac{1}{\tau_s} \right)^2 + \omega^2 \right)} \Delta I_1^* \tag{5.18}$$

where

$$\tau_s = \frac{L_s}{R_s}$$

The relationship between the variables $\Delta E_{dc}$, $\Delta I_1^*$ and $\Delta I_o$ can be further developed by substituting Eqns. (5.17) and (5.18) into (5.16), as follows:

$$\Delta E_{dc} = G(s) \Delta I_1^* - G_\| (s) \Delta I_o \tag{5.19}$$

where

$$G(s) = \frac{d_2 S^2 + d_1 S + d_0}{\left( S + \frac{1}{\tau_c} \right) \left( \left( S + \frac{1}{\tau_s} \right)^2 + \omega^2 \right)}$$

$$G_\| (s) = \frac{1}{C \left( S + \frac{1}{\tau_c} \right)}$$
This leads to the "open-loop" transfer function for root-locus analysis following:-

\[
1 + \frac{K_p K_{df}}{T_{df}} \frac{d_2}{(S + z_1)(S + z_2)(S + z_3)} = \frac{(S + p_1)(S + p_2)(S + p_3)(S + p_4)(S + p_5)}{(S + p_1)(S + p_2)(S + p_3)(S + p_4)(S + p_5)}
\]

(5.20)

where

\[p_1 = 0, \quad p_2 = \frac{1}{\tau_c}, \quad p_3 = \frac{1}{T_{df}}, \quad p_4 = \frac{1}{\tau_s} - j\omega, \quad p_5 = \frac{1}{\tau_s} + j\omega\]

\[z_1 = \frac{1}{\tau_c}, \quad z_2 \text{ and } z_3 \text{ are the solutions of } S^2 + \frac{d_1}{d_2} S + \frac{d_0}{d_2} = 0\]

5.5.2 Stability Analysis

It noticed from Eqns.(5.17) and (5.18) that both the current \(\Delta i_{sd}\) and \(\Delta i_{sq}\) are damped oscillatory functions with a time constant \(\tau_s\). If \(\tau_s\) is very large (corresponding to low resistance on the ac side), duration of oscillations will be increased. This explains why the stability of the voltage-forced scheme relies on the presence of input resistance [GREEN 1988].
Rough sketches of root-loci with different values of the time constant $T_1$ are shown in Fig.5-8. It can be seen that even with a large time constant $T_1$, as in Fig.5-8(c), as the gain $K_p$ increases the root loci starting from a conjugate pair of poles, $p_4$ and $p_5$, soon crosses the imaginary axis and the system becomes unstable. To achieve a wider region of stability it is required that the complex pole pair, $p_4$ and $p_5$, should lie sufficiently far to the left of the imaginary axis. However, the real part of the conjugate pair of poles is associated with the quality factor $Q$ of the inductors. To move it to the left requires an increase the a.c. resistance and hence the quality factor of the inductors is reduced. This is undesirable, however, as the efficiency and the power factor of the device will be reduced. Even with a large a.c resistance ($r_s = 0.5\Omega$ for $L_s = 4\text{mH}$), the accurate root-locus diagram in Fig.5-9 shows that the stable region is still restricted.

5.5.3 Dynamic Compensation

The major reason why the voltage-forced scheme is less stable than the current-forced is that the calculations of the required terminal voltages have to be based on the steady state diagram, because the instantaneous a.c currents are not monitored. This differs from the predictive current-forced scheme discussed in section 3.5.

Taking account of the transient situation in calculations can improve stability of the voltage-forced system. In considering Eqn.(2.30) which describes the transient response of the rectifier in the d–q frame, if the discrete-time nature is neglected, the fundamental value of the terminal voltages should satisfy:-
Fig. 5-8 Sketches of Root-Loci of the Voltage-Forced Scheme
(a) when $1/T_1 > 1/\tau_c$
(b) small $1/T_1$ but $1/T_1 > 1/\tau_c$
(c) small $1/T_1$ but $1/T_1 < 1/\tau_c$

\[
\begin{align*}
\mathbf{v}_{Rm} &= -R_s i_{sd} + v_{sd} + \omega L_i \frac{di_{sd}}{dt} \\
\mathbf{v}_{Rq} &= -R_s i_{sq} + v_{sq} - \omega L_i \frac{di_{sq}}{dt}
\end{align*}
\]

Therefore, by assuming $i_{sd} = i_{sq}^*, i_{sq} = 0, v_{sd} = V_s$ and $v_{sq} = 0$, Eqn.(5.12) becomes:
**ROOT LOCI FOR VOLTAGE-FORCED CONTROL SYSTEM**

Kp: 0 $\rightarrow$ 20 step=0.1
rs = 0.01 (ohm)
rs = 0.05 (ohm)
rs = 0.5 (ohm)

Fig.5-9 An Accurate Root-Locus Diagram for Voltage-Forced scheme
(Rectification)

\[ V_{sm} = 339.4V, \quad E_{dc} = 710V, \quad L_s = 4\text{mH}, \quad C = 1250\mu\text{F}, \quad I_0 = 20A, \]
\[ K = 1, \quad T_{df} = 0.002, \quad T_I = 0.4 \]

\[ V_{Rdf} = V_s - R_s I_s^* - L_s \frac{dI_s^*}{dt} \]
\[ V_{Rqf} = -\omega L_s I_s^* \]

Correspondingly, Eqns.(5.13) and (5.14) become:

\[ L_s \frac{di}{dt} + R_s i_{sd} - \omega L_s i_{sq} = R_s I_s^* + L_s \frac{dI_s^*}{dt} \]
\[ L_s \frac{di}{dt} + R_s i_{sd} + \omega L_s i_{sq} = \omega L_s I_s^* \]

\[ C E_{dc} \frac{dE_{dc}}{dt} = (V_s - R_s I_s^* - L_s \frac{dI_s^*}{dt}) i_{sd} - \omega L_s i_{sq} - E_i i_{dc out} \]
Applying a small perturbation and using Laplace transformation as before yield:

\[
\begin{bmatrix}
R_s + S L_s & -\omega L_s \\
\omega L_s & R_s + S L_s
\end{bmatrix}
\begin{bmatrix}
\Delta i_{sd} \\
\Delta i_{sq}
\end{bmatrix}
= \begin{bmatrix}
(R_s + S L_s) \\
\omega L_s
\end{bmatrix}
\begin{bmatrix}
\Delta i^*_s
\end{bmatrix}
\]

(5.24)

\[
\Delta E_{dc} = \frac{V_s - R_s I^*_{sd0}}{C E_{dc0}} \Delta i_{sd} - \frac{\omega L_s I^*_s}{C E_{dc0}} \Delta i_{sq} - \frac{R_s + S L_s}{C E_{dc0}} \Delta i^*_s
\]

(5.25)

Solving Eqn.(5.24) gives:

\[
\begin{cases}
\Delta i_{sd} = \Delta i^*_s \\
\Delta i_{sq} = 0
\end{cases}
\]

(5.26)

and, substitution of (5.26) in (5.25) yields:

\[
\Delta E_{dc} = G(s) \Delta i^*_s - G_i(s) \Delta I^*_i
\]

(5.27)

where

\[
G(s) = \frac{-a_1 S + a_0}{S + \frac{1}{\tau_c}}, \quad G_i(s) = \frac{1}{S + \frac{1}{\tau_c}}
\]

\[
a_1 = \frac{L_s I^*_{sd0}}{C E_{dc0}}, \quad a_0 = \frac{V_{s0} - 2 R_s I^*_{sd0}}{C E_{dc0}}
\]

This is the same equation as Eqn.(5.3a). Thus, it has been proved that
after adding the item $L_s dI_s^*/dt$ into the calculations, the voltage-forced scheme has the same transfer function as the current-forced, and then has the same region of stability.

An alternative explanation for dynamic compensation is as follows:- In the current-forced scheme, both in the transient and in the steady state, the input current is forced to track the reference which is generated by multiplying together the in-phase template and a "required amplitude" signal. This ensures that the q-axis component $\Delta I_{sq}$ equals zero and the d-axis component $\Delta I_{sd}$ equals the reference $\Delta I_s^*$ in both states. For voltage-forced scheme it is the rectifier terminal voltages that force the input currents to have the required amplitude and to be aligned with the mains voltages. If the transient change $L_s dI_s^*/dt$ is considered in calculation of the terminal voltages, $\Delta I_{sq}$ will be eliminated and $\Delta I_{sd}$ will be forced to be equal to $\Delta I_s^*$ throughout the transient period, resulting in the same effect as in the current-forced case.

5.5.4 An Example

In this example, two different transient responses will be demonstrated. One is without dynamic compensation and thus has unstable response; the other is with compensation, which results in stable response.

Digital implementation of the voltage-forced scheme is well simulated by ACSL (Advanced Continuous Simulation Language). The differential term $L_s dI_s^*/dt$ is replaced by a difference equation:-
\[
\frac{I_s(n) - I_s(n-1)}{L_s} T_s
\]

where \( n \) represent \( n \)-th sampling period and \( T_s \) is a sampling period.

The circuit parameters and the load change studied is that used in Fig.5.7(a). Fig.5-10(a) shows the response of the d.c. link voltage without compensation, where the instability is clearly seen. In contrast, the response with compensation is shown in Fig.5-10(b), where stable response is achieved.

(a) (b)

Fig.5-10 Response of the D.C. Link Voltage Using Voltage-Forced Scheme
(a) Without Compensation (b) With Compensation

5.6 Transient Response of D.C. Link Voltage

5.6.1 Transient Response with PI Controller
The quality of the control system is judged by the criteria of stability, response time (or bandwidth), and steady-state error. A small-signal model is effective in analysis of stability of the control system, but not in analysis of the transient behaviour. Analysis of the transient response of the rectifier control system seems difficult because of its nonlinear and discrete nature.

For a complete transient study of the control system, a general set of equations, Eqn.(2.9) and (2.11), which are valid in describing the behaviour of the rectifier under both transient and steady-state conditions, was solved in conjunction with equations representing the control system. A number of simulations with the different parameters of the PI controller were executed in order to choose the proper combination of the parameters and/or to give an empirical 'short cut' in practice. The results presented in Table5-1 and Table5-2 refer to a system with the test load current $I_o = \pm 14A$ (average), reversing at $t_{z1}$ and $t_{z2}$ as shown in Fig.5-11. Other parameters are as follows:

- Input Voltage (Line-to-Line) : 415V (r.m.s.)
- Input Inductance $L_s$ : 4mH
- D.C. Link Voltage $E_{dc}^*$ : 710V
- D.C. Capacitance $C$ : 1250\mu F
- Crossover Frequency of D.C. Voltage Filter : 80Hz

The overshoot and droop (variations), $\sigma_1$ and $\sigma_2$, as well as the corresponding regulation time (settling time) $t_1$ and $t_2$, under the test load are also specified in Fig.5-11.
Fig. 5-11 Waveform of the Average Load Current for Testing the Transient Performance and Specification of the Corresponding Variation of the D.C. Link Voltage

It is not surprising that the variations of the d.c. link voltage are hardly changed as the integral part $T_1$ of the PI controller varies, but the value of $T_1$ affects the shape of d.c. link voltage, thus influencing the regulation time. With a large $T_1$ the overdamped waveform of the d.c. link voltage is observed, as an example shown in Fig. 5-12. Decreasing $T_1$ can result in an underdamped response and, eventually lead to instability. The critical value of $T_1$ in this particular case is 0.003. By increasing $K_p$ the d.c. voltage variations can be reduced, provided that the combination of the parameters is still within the stability region specified by Eqns. (5.6) and (5.7).

Therefore, the design procedure can be suggested as:— (i) $K_p$ is first selected to be within the stable region but large enough in order to eliminate the voltage variations (using Eqn. (5.6)); (ii) a relatively larger
<table>
<thead>
<tr>
<th>$\sigma_1 / \sigma_2$ (%)</th>
<th>$K_p \ (1/\Omega)$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.2</td>
</tr>
<tr>
<td>0.002</td>
<td>*</td>
</tr>
<tr>
<td>0.003</td>
<td>9.85/11.1</td>
</tr>
<tr>
<td>0.004</td>
<td>10.2/11.7</td>
</tr>
<tr>
<td>0.006</td>
<td>10.8/12.5</td>
</tr>
<tr>
<td>0.008</td>
<td>11.1/12.9</td>
</tr>
<tr>
<td>0.010</td>
<td>11.4/13.2</td>
</tr>
</tbody>
</table>

*: Oscillatory Table 5-1 Overshoots $\sigma_1$ and $\sigma_2$

<table>
<thead>
<tr>
<th>$t_1/t_2$ (ms)</th>
<th>$K_p \ (1/\Omega)$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.2</td>
</tr>
<tr>
<td>0.002</td>
<td>*</td>
</tr>
<tr>
<td>0.003</td>
<td>45/63</td>
</tr>
<tr>
<td>0.004</td>
<td>48/56</td>
</tr>
<tr>
<td>0.006</td>
<td>40/43</td>
</tr>
<tr>
<td>0.008</td>
<td>38/33</td>
</tr>
<tr>
<td>0.010</td>
<td>50/38</td>
</tr>
</tbody>
</table>

*: Oscillatory Table 5-2 Regulation Times $t_1$ and $t_2$

$T_1$ can be selected to ensure the combination of $K_p$ and $T_1$ to be within the stable region (using Eqn. (5.7)); (iii) the transient response of the d.c. link voltage can be easily obtained by simulation, with these pre-selected parameters and the specified load condition; (iv) if the transient response is not satisfied by only reducing $T_1$, $K_p$ should be modified and repeat (i),
Fig. 5-12 Transient Response of the D.C. Link Voltage Under the Change of the Load Current Specified in Fig. 5-1 ($I_o = \pm 14$ A)

<table>
<thead>
<tr>
<th>$K_p$</th>
<th>$T_1$ (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.002</td>
</tr>
<tr>
<td>0.2</td>
<td>0.004</td>
</tr>
<tr>
<td>3</td>
<td>0.004</td>
</tr>
<tr>
<td>1</td>
<td>0.01</td>
</tr>
</tbody>
</table>
(ii) and (iii) until a satisfactory response is obtained. In addition, two other well-known empirical 'short cut' methods, the reaction curve method and the continuous cycling method, which are inadequate in some circumstances but are often well worth trying, can be found in a reference book [BORRIE 1986].

5.6.2 Transient Response with Load Information Injection

The principal advantage of injection of load information is to improve the transient response of the d.c. link voltage, which is restrained by stability conditions, and ultimately to reduce the d.c. capacitance. This effect can also be demonstrated by means of simulation. The PI controller with $K_p = 1$ and $T_i = 0.004$ is used in every case where the capacitance is changed. So, the fluctuation in d.c. link voltage increases as the the capacitance is decreased. The load current and other parameters are the same as those in the previous section. The great reduction of the fluctuation in the d.c. link voltage is shown from the results in Fig.5-13. Alternatively, the capacitance can be greatly reduced for the same allowable voltage fluctuation if load injection is applied. Some experimental results will be shown in Chapter 7 to demonstrate further the effect of the load injection.

5.7 Summary

In order to simplify the study of stability of the control system, in both current forced and voltage forced schemes, the time-discrete nature of the waveforms has been neglected. This has allowed continuous small-signal models to be derived. Based on them, the conditions for selecting the parameters of the PI controller to achieve stability are provided.
Further studies of stability have led to the conclusion that the voltage-forced scheme is less stable than the current-forced scheme. Dynamic compensation is required to achieve a wider stable region for the voltage-forced scheme, and can lead to similar performance for both schemes.

Another important conclusion made from the analysis of stability is that the control system has a wider stable region in regenerative mode than in rectifying mode, which implies that as far as the stability is concerned only the rectifying mode needs to be considered when designing the PI controller.

Transient response of the d.c. link voltage can be easily analysed by means of simulation. A trial-and-error procedure has been suggested for selecting suitable values of the PI controller. It has also been demonstrated in this chapter that a better response is achievable by injecting load information directly into the control loop in order to overcome the problem of the sluggish response due to constraint of stability. Alternatively further reduction of the d.c. link capacitance is made possible.
Chapter 6 A Control Scheme Using Theory of Variable Structure Systems

6.1 Introduction

Variable structure control with a sliding mode was first described by Russian authors, notably Emel’yanov and Utkin [EMEL’YANOV 1964, UTKIN 1971, 1972]. In recent years the subject has attracted the attention of numerous researchers because of its excellent invariance properties. There has been a wide interest in application of sliding mode control theory in power electronics, such as in drive systems [BOSE 1985, SABANOVIC 1981, SICARD 1989, LIM 1991], dc–dc converter [VENKATARAMANAN 1985, HUANG 1989] and dc–ac converter control [CARPITA 1988].

The control systems presented in previous chapters consist of two stages, as shown in Fig.1–10. The inner loop is the a.c. current control whereas the outer loop controls the d.c. link voltage. As in most conventional two-loop control systems, the speed of the inner loop is usually faster than the outer loop. This allows us to analyse the two stages independently. The synthesis of the whole system can be broken down into two steps:—first inner loop can be synthesized—e.g. in a current-forced scheme one of the tracking techniques is chosen and implemented to ensure that the actual currents follow the reference, as discussed in Chapter 3; and then synthesis of the outer loop can be undertaken, as described in Chapter 5. However, even if the a.c. current loop can be perfectly synthesized, it can be seen from Chapter 5 that difficulty in dealing with the d.c voltage control loop will arise because of the nonlinear characteristic. The small signal model
is very effective for analysing the stability of the d.c. voltage control loop, but the analytical solution to the transient behaviour is impossible to determine. For this reason, the study of transients was based on simulations and the design of control system is still essentially empirical.

The theory of variable structure systems can be applied to power electronic systems, to yield an alternative novel control scheme, known as sliding mode control. The principal advantage of sliding mode control is that the response of the system is insensitive to its parameters and load disturbance. In sliding mode control, the 'reference model' or a predefined trajectory in phase plane (or super surface) is pre-designed and the system is forced to follow or 'slide' along the 'reference model' or the trajectory by using a suitable switching control algorithm, irrespective of system parameters. Hysteresis comparison control in current-forced schemes is a good example of sliding mode control of the a.c. current, where the 'predefined' trajectory is the current reference waveform. However, in that scheme, the 'predefined' trajectory has to be varied through the conventional regulation with the PI controller of the d.c. link voltage in order to regulate the power flow.

It is possible, however, to design a predefined trajectory which obtains not only information of a.c. currents but also that of the d.c. voltage in order to control both quantities using only one stage. The transient behaviour of such a system is determined by this trajectory, so long as a suitable switching algorithm can be applied to force the system to slide along it. The intensive investigation of theory of variable structure systems is not a purpose of this thesis, but some fundamental concept will be used and a
preliminary study of control scheme using this theory will be reported,

6.2 Review of Variable Structure System Theory

6.2.1 Variable Structure Systems

As evidenced by their names, variable structure systems differ from traditional automatic control systems in that their structures change during the transient process. This change of structure is usually intentional even though the original systems have a stationary structure, which can be described by continuous differential equations. The deliberate introduction of variable structure, in accordance with some prespecified algorithm or law of structural change, opens up many possibilities for overcoming the inherent problems of the original system, such as non-linear characteristics, variable parameters and load disturbance effects [UTKIN 1972, 1977, 1978, ZINOBER 1990].

The theory of variable structure systems can also be used to deal with discontinuous systems which are described fundamentally by discontinuous differential equations [UTKIN 1972]. Switching converters can be regarded in this way. Change of the structure is accomplished by the proper choice of sequence and time duration of OFF and ON states of the power switches; hence the differential equations describing the behaviour of the converter are changed, as can be seen from equations like Eqn.(2.11) and (2.13). Application of the theory of variable-structure systems and deliberate introduction of sliding modes make the realization of rather simple and yet quite efficient control schemes for various types of converters possible.
A variable structure system is assumed to consist of several continuous subsystems, henceforth referred to as structures; each of these structures may be unacceptable from the point of view of the quality of the control process, - by, for example, being unstable. The purpose of the controller is to select a proper switching algorithm between these structures such that useful properties of the structures are preserved, and, in some cases, new properties are obtained.

![Variable Structure Control of a Typical Second Order System](image)

6.2.2 An Example of Sliding Mode in Variable Structure Systems

To understand the basic principles of sliding mode control, it is useful to cite a typical example whose block diagram is shown in Fig.6-1 [BOSE 1985]. The plant is a simple second order system where the gain K may vary. The system has two structures, one being a negative feedback structure when an ideal switch is turned to point A, and the other a positive feedback structure when the switch is switched to point B. Each of the structures is described by its state space equation:-
\[
\begin{align*}
\frac{dx_1}{dt} &= x_2 \quad \text{(negative feedback)} \\
\frac{dx_2}{dt} &= -K x_1
\end{align*}
\]

and
\[
\begin{align*}
\frac{dx_1}{dt} &= x_2 \quad \text{(positive feedback)} \\
\frac{dx_2}{dt} &= +K x_1
\end{align*}
\]

where \( x_1 = R^* - R \) is the error signal.

The general solutions of Eqn. (6-1) and (6-2) satisfy the following relations:

\[
\frac{x_1^2}{A^2} + \frac{x_2^2}{KA^2} = 1 \quad \text{(negative feedback)} \quad (6-3)
\]

This can be plotted as a set of ellipses in the phase plane, as shown in Fig. 6-2(a);

For positive feedback:

\[
\frac{x_1^2}{4B_1 B_2} - \frac{x_2^2}{4KB_1 B_2} = 1 \quad \text{(positive feedback)} \quad (6-4)
\]

This can be plotted as a set of hyperbolas in the phase plane. Both of the structures, as shown, are unstable. However, by switching these two
structures according to a suitable law, the response of the resultant variable structure system can theoretically be constrained to a specified characteristic. Assume that the system starts arbitrarily at the point A, shown in Fig.6–2(b). The negative feedback structure is firstly selected so that the operating point (describing point) moves along the elliptic line until it reaches a predefined trajectory, termed a sliding line, \( c \), which is defined by:

\[
\sigma = c x_1 + x_2 \tag{6-5}
\]

where the coefficient \( c \) has been selected such that the sliding line \( \sigma = 0 \) is between the axis \( x_1 \) and the asymptote of hyperbolic trajectories associated with the positive feedback; thus \( 0 < c < \sqrt{K} \). When the operating point reaches at B after crossing the sliding line \( \sigma \), the system is switched to positive feedback and therefore the operating point moves back toward the sliding line \( \sigma \), along the hyperbolic line. After crossing
the line $\sigma = 0$ again, the operating point reaches the point C, resulting in
the negative feedback structure which pushes the operating point back to the
sliding line $\sigma = 0$. As a result, the motion of the operating point will
\textit{slide} on the sliding line $\sigma$ and the time domain response for movement along
the line $\sigma = 0$ can be given by:

$$x_1(t) = x_1(t_1) e^{-c(t - t_1)} \quad (6-6)$$

where $t_1$ is the time when operating point hits the line $\sigma$ from any initial
position. Eqn.(6-6) gives the mean response of the system along the
sliding line $\sigma = 0$, and it is not affected by variation of parameter K
because the line $\sigma = 0$ determines the system response. This phenomenon is
called \textit{sliding mode}.

This example shows that two unsatisfactory configurations can be switched
alternately by a proper switching algorithm to form a variable structure
system which has a deterministic response. More importantly, the resultant
variable structure system is insensitive to parameter variation and load
disturbance effects.

6.3 Control of the Reversible Rectifier Using Theory of Variable
Structure Systems

In order to design a variable structure control system a designer must
possess a strong theoretical background in the variable structure theory,
which may prove to be a major obstacle in practice. In essence, the first
stage of the design of such a system entails the choice of the predefined
trajectory - the sliding line or surface. The parameters are chosen to yield the desired dynamic response, so obtaining stability. The second stage of the design procedure involves the selection of a suitable switching algorithm which will ensures that (i) the system will be able to reach the predefined sliding line (reaching condition) and (ii) the system having reached the sliding line will be then kept on it (existing condition).

To implement sliding mode control of a reversible rectifier, it is convenient to use the space vector and rotating d-q models which were developed in Chapter2.

Define a switching line as [HABETLER 1989]:-

\[ \sigma = K \Delta E_{dc} + \Delta I_{sd} = 0 \]  

(6.7)

where

\[ \Delta E_{dc} = E_{dc} - E^*_{dc} \]  

(6.8)

and

\[ \Delta I_{sd} = i_{sd} - i^*_{sd} \]  

(6.9)

Rewrite Eqn.(3.1) as:-

\[ L_s \frac{di_s}{dt} = -V_s(k) + \frac{V_R(k)}{s} \]  

(6-10)

As discussed in previous chapters, the supply voltage vector \( V_s \) rotates at the angular frequency \( \omega \) on the space plane and the current vector \( i_s \) is governed instantaneously by selecting the terminal voltage vector \( V_R(k) \).
The current vector $i_s$ can be projected into the d–q rotating frame where the d–axis is fixed at the supply voltage vector $V_s$, as shown in Fig.6–3. The current vector $i_s$ may lead or lag the supply voltage vector $V_s$ between two switching instants. The objective of the controller is to select a proper terminal voltage vector in such a way that (i) the ac currents are controlled to be sinusoidal locked to the mains, that is, $i_{sd} = i_{*sd} = \sqrt{2/3}i_{sm}$ and $i_{sq} = 0$, and (ii) the d.c. link voltage and the a.c. currents satisfy Eqn.(6.7). If the system is sliding on the sliding line $\sigma = 0$, the transient behaviour is determined by Eqn.(6.7) and the d.c. link voltage is equal to its reference as $\Delta i_{sd}$ is controlled to be zero. $i_{*sd}$ can be obtained by estimating the load requirement discussed in section 5.2.

![Fig.6–3 Space Vector Diagram for Explaining the Principle of the Sliding Mode Control](image)

The first objective of the controller is to force the q-component $i_{sq}$ of $i_s$ to be zero so that $i_s$ will become aligned with $V_s$. This can be implemented with reference to an example in Fig.6–3, where $i_s$ lags $V_s$ at an arbitrary
angle. Three terminal voltage vectors can be selected to force \( i_{sq} \) to be zero; they are \( V_R(1) \), \( V_R(5) \) and \( V_R(4) \). \( V_R(1) \) and \( V_R(5) \) increase the amplitude of \( i_s \) but \( V_R(4) \) reduces it. The choice between them is made by considering the second objective, making \( \sigma = 0 \). When \( \sigma > 0 \), it should reduce the amplitude of the a.c. current in order to reduce \( \sigma \); thus the vector \( V_R(4) \) is selected. Otherwise, when \( \sigma < 0 \), \( V_R(1) \) or \( V_R(5) \) is chosen. The switching algorithm is summarized in Table.6-1, where the different region of \( V_s \) are considered.

<table>
<thead>
<tr>
<th>( V_s )</th>
<th>( i_{sq} &gt; 0 )</th>
<th>( i_{sq} &lt; 0 )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( \sigma &gt; 0 )</td>
<td>( \sigma &lt; 0 )</td>
</tr>
<tr>
<td>I</td>
<td>( V_R(6) )</td>
<td>( V_R(3) )</td>
</tr>
<tr>
<td>II</td>
<td>( V_R(2) )</td>
<td>( V_R(1) )</td>
</tr>
<tr>
<td>III</td>
<td>( V_R(3) )</td>
<td>( V_R(5) )</td>
</tr>
<tr>
<td>IV</td>
<td>( V_R(1) )</td>
<td>( V_R(4) )</td>
</tr>
<tr>
<td>V</td>
<td>( V_R(5) )</td>
<td>( V_R(6) )</td>
</tr>
<tr>
<td>VI</td>
<td>( V_R(4) )</td>
<td>( V_R(2) )</td>
</tr>
</tbody>
</table>

Table 6-1  Switching Table for Sliding Mode Control

The results of simulation are given in Fig.6-4, for which circuit parameters are the same as those in a conventional control system in Appendix III. In comparison with the conventional control system where the d.c. link voltage is controlled by a PI controller plus the injection of the load information as shown in Fig.A-3-6, sliding mode control provides a better transient performance and its transient behaviour is determined by the designed parameter \( K \) in Eqn.(6.7).
It is believed that difficulty in designing suitable system for controlling the D.C. link voltage in order to satisfy the transient requirement might be overcome by using theory of variable structure system. By means of simulations, the preliminary results demonstrate the principle and operation of the reversible rectifier using the sliding mode control scheme. It should be pointed out that there are many theoretical and practical problems.
unsolved yet but the basic principle of sliding mode control is still very attractive, and research on this novel scheme is a prospective topic in the future.
CHAPTER 7. DESIGN CONSIDERATIONS AND EXPERIMENTAL WORK

7.1 Introduction

The objective of the practical work was to investigate and build a small scale prototype reversible rectifier and its control systems, in order that a complete understanding of the theoretical and practical performance could be achieved. It was originally planned that all the control schemes, including the voltage-forced and sliding mode schemes, would be implemented. However, thus far only the current-forced schemes, have been investigated practically. A cheap analogue control system, employing a simple hysteresis comparison and ramp comparison schemes, and a more expensive transputer based digital control system implementing the predictive control scheme, were constructed.

7.2 Descriptions of Practical Work and Design Considerations

7.2.1 Power Devices and Power Circuit Design

To achieve a good quality of waveform, it is desirable to operate a reversible rectifier at a high switching frequency. The choice of fast switching devices lay between power bipolar transistors, MOSFETs and IGBTs.

It was initially intended to use IGBTs to construct a 5.5KVA rectifier, to be operated in conjunction with an inverter fed induction machine drive system then available in the laboratory. Due to financial limitations, a 1KVA prototype, switching at up to 20KHz, was actually constructed, incorporating
power MOSFETs of type IRFP240. This practical work concentrated on demonstrating the principle and operation of the reversible rectifier, rather than on the development of good power-switching circuits. Aspects such as losses in power devices are well described in the applications literature [e.g. GRANT 1987, IKEDA 1988, MESTHA 1989, HEUMANN 1989].

7.2.2 Circuit Parameters

It is first necessary to select suitable circuit parameters in order to operate a reversible rectifier in its proper mode. The parameters include the d.c. link voltage, the input inductance, and the d.c. link capacitance.

7.2.2.1 d.c. link voltage

The previous chapters showed that the d.c. link voltage must necessarily be higher than that in a simple diode rectifier. A higher d.c. link voltage can be advantageous, as far as control of the machine is concerned, because the voltage transfer ratio, that is, the ratio of the a.c. voltage of the machine to the supply voltage, can be higher than 1. Selection of the d.c. link voltage should take account of the follows:–

- It should be high enough to remain always above the minimum value required by the specific control scheme, whatever the load changes. Typically this requires a voltage 10–20% higher than the natural value of the rectified voltage.
- The voltage stress and switching losses of the switching devices.
For testing the prototype reversible rectifier, the d.c. link voltage was set to be 65V or 72V, with a corresponding line-line input voltage of 41.5V (r.m.s.).

7.2.2.2. input inductance and d.c. link capacitance

The choice of input inductance is based on the following considerations—

- To reduce the amplitude of the switching components in the input current and to facilitate smooth control a reasonably large inductance is required;
- As the inductance is increased the cost rises, and the dynamic range of the controller must be widened to obtain a satisfactory response.

A suitable value of capacitance should be selected by considering stability and transient response of the d.c. link voltage control: the capacitance should be substantial enough to prevent sudden load changes from altering the d.c. voltage too quickly, and so exceeding the dynamic range of the controller of the d.c. link voltage. The discussions in the previous chapter suggested that injection of load information could improve transient response and hence widen the dynamic range of the controller. The value of the capacitance can be reduced if the information about load is injected.

A more fundamental problem relevant to the reversible rectifier concerns the minimization/optimization of the reactive components. As switching devices continue to improve, the reactive components used as energy storage and
filtering will increasingly dominate the cost and the power density. There were few reports of reactive component minimization [ZIOGAS 1984, 1985]. More detailed discussions were given by T.G. Habetler and D.M. Divan [HABELTER 1989], with the major conclusions as follows:— (i) Filter cost is lower with the voltage-sourced configuration (present configuration) than that with the current-sourced configuration (not be discussed in this thesis); (ii) Once the configuration is specified, filter minimization becomes dependent only on the switching pattern. The objective to minimize the reactive filter requirements was to minimize the energy stored in the capacitor and the inductors by satisfying some constraints. These constraints were that (i) the input and output voltages are defined, and (ii) the total harmonic distortions of the input and output current are specified.

It should be noted that the minimum value of capacitance by such a method was much smaller than that it should be, because they assumed that the d.c. link capacitor only handle the switching harmonics and the regulation of the d.c. link voltage was not considered. From the analysis in Chapter 5 it has been seen that there is a restraint on the value of capacitance as far as the regulation of the d.c. link voltage is concerned. It was found that the value of capacitance which is required for satisfying the performance of regulation is much larger than that which is required for removing the switching harmonics. Then, use of the total energy stored in both the capacitor and the inductors as the optimum criterion seems to be questionable. Reactive component minimization is still opened to be investigated. However, one method to choose the suitable reactive component is suggested as follows:—
(i) Since the capacitance chosen for satisfying the regulation performance of the d.c. link voltage is much larger than that for removing the switching harmonics and there is a low-pass filter in the feedback path, it is reasonable to assume that the switching harmonic content, due to the switching of the rectifier and the inverter, is very small and it has no effect on the a.c. current;

(ii) Choose a small initial value of inductance and calculate the total harmonic distortion in the input current with the specific control scheme and the specific switching frequency;

(iii) If the total harmonic distortion is not satisfactory, increase the inductance and repeat (ii) and this step until the suitable inductance is obtained;

(iv) Choose a small initial value of capacitance and simulate the performance of the d.c. link voltage loop with a specific controller and the specific load;

(v) If it is difficult to design the controller of the d.c. link voltage to satisfy the required performance by using the method described in Chapter 5, increase the capacitance and repeat (iv) and this step until the suitable capacitance is obtained.

An example of selecting the suitable value of the inductance and capacitance, as well as the parameters of the PI controller, for a high power level rectifier is given in Appendix III and the performance of such a system is
shown by simulation. In the laboratory prototype of the reversible rectifier, the 4mH inductance and a 1250μF electrolytic capacitor was arbitrarily chosen.

7.2.3 Drive Circuit Design

The purpose of this work was to obtain the fundamental knowledge about the switching performance of the power devices and their gate drive characteristics. The drive circuit designed for MOSFETs/IGBTs, shown in Appendix IV, provided a simple, low cost, high performance solution to the gate drive requirements. A transformer-isolated driver overcomes the disadvantages of an optical coupler-isolated driver - namely the poor noise immunity, the high impedance output and the need for additional floating power sources which add the cost and complexity. In addition, transformer coupling of low level signals to power switches offers several other advantages such as impedance matching, DC isolation and either step-up or step-down capability.

7.2.4 D.C. Link Current and a Simulated Inverter Load

The ultimate load of the reversible rectifier is normally an inverter, switching at a high frequency to supply a variable-frequency, variable-voltage source to an a.c. machine. Conceptually, the d.c. link current waveform is obtained by multiplying the sinusoidal current waveform of the stator and its corresponding switching function. In general, the current consists of both positive and negative pulses, depending on the power factor of the machine [EVANS 1986].

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To test the reversible rectifier, a simulated inverter load, consisting of resistors, a bank of lead-acid batteries, and MOSFET switches, was constructed, as shown in Fig. 7-1, to model the d.c. link current drawn by the inverter load. The voltage of the battery bank is larger than the d.c. link voltage and the two resistances are selected to provide a bi-polarity current pulse drawn from the link when the two MOSFETs are driven by a pulse generator. The power flow can be controlled by changing the duty cycle of the pulse applied to the two MOSFETs. The only difference between the simulated inverter load and the real inverter load is the shape of the pulse current, but this does not influence control of the power flow.

7.2.5 Selection of A.C. Current Control Schemes

The theoretical analysis in Chapter 5 shows that the current-forced schemes can provide better stability than the voltage-forced schemes. To achieve the same stable region as with the current-forcing, voltage-forcing needs a more complicated control system, which additionally increases the cost of the
whole control system. In comparison with the voltage-forced scheme, the only disadvantage of current-forcing, is the necessity of monitoring a.c. currents. Fortunately, a high quality current sensor is not expensive nowadays. Therefore, current-forced schemes are preferable to voltage-forced one, and so have been implemented.

7.3 Analogue Control System

A simple analogue control system employs the simple hysteresis comparison and/or the ramp comparison technique to control the a.c. current. The d.c. link voltage or power flow is governed by a PI controller, together with a load information injection loop. In this section, implementation of the analogue control system will be presented in detail.

7.3.1 Control System Diagram

The block diagram of the control system with a current-forced control scheme has been shown in Fig.3-1. It consists of an a.c. current controller, a reference signal generator, a d.c. link voltage regulator, a low pass filter and the current/voltage measurement circuits.

7.3.2 A.C. Current Controller

Fig.7-2 shows the a.c. current controller in one phase, which consists of two stages. The op-amp $A_1$ compares the a.c. current feedback signal with its reference, followed by a hysteresis Schmitt trigger $A_2$. With these two stages the current error can be observed and the hysteresis band can be
altered by changing the RP value. In addition, a triangle wave at fixed frequency can easily be applied to the comparator, through \( R_r \), to implement the ramp comparison control.

![Hysteresis Comparator Diagram](image)

**Fig. 7-2** A Hysteresis Comparator

### 7.3.3 Generation of Current Reference

A current reference generator provides the a.c current control with the required sinusoidal waveform. It is implemented by an analogue 4-quadrant multiplier which multiples a sinusoidal template, derived from the phase voltage of the mains, and the output of the PI controller. The device chosen is actually a transconductance amplifier, the LMI3600. This operational amplifier is a very versatile device, which can easily be made to act as a voltage-controlled amplifier [MARSTON 1989]. It has differential voltage input terminals (like a conventional op-amp) but the gain can be controlled by an external bias current fed into the amplifier terminal. Fig.7-3 shows an economical yet effective analogue 4-quadrant multiplier using the LMI3600, set up to generate the current reference. The template
sinusoidal is derived from the phase-neutral mains voltage, followed by a low-pass filter. The control signal from the output of the PI controller is tied to pin 5, which controls the gain of the amplifier. The output signal polarity at pin 8 depends on the polarities of both the template and the control signal, while its amplitude can be varied by changing the control signal applied to pin 5. Thus a sinusoidal reference is generated whose waveform follows the template, and whose amplitude is controlled by the output of the PI controller.

7.3.4 Current and Voltage Measurement

The a.c. current measurement is carried out by using a multi-range current transducer, LEM type LA25-NP, in each phase. The module provides electronic measurement of d.c., a.c., and pulsed currents with galvanic isolation with a bandwidth from DC to 150KHz.
The d.c. link voltage is measured by means of the circuit shown in Fig. 7-4. The high voltage is attenuated by resistors, followed by a differential amplifier with a low-pass first-order active filter which eliminates the switching ripple from the d.c. link.

![Circuit Diagram](image)

**Fig. 7-4** Measurement and Control of the D.C. Link Voltage

7.3.5 Controller/Load Information Injection

A simple PI controller using an operation amplifier is also shown in Fig. 7-4. The output of the PI controller is applied to an adder which is capable of injecting the rectifier load information directly to the a.c. current control loop. For protection, two zener diodes are used to limit the output voltage, which thus limits the amplitude of the reference current.
7.3.6 Experimental Results

Performances of the prototype reversible rectifier in steady state and in transient state are demonstrated in this section by showing the a.c. current waveform together with its phase voltage and the d.c. link voltage waveform.

Fig.7-5 shows the a.c. current waveform and the corresponding phase voltage in one input line of a conventional three-phase diode-bridge rectifier. It can be seen that the current at the input to the diode bridge deviates significantly from a sinusoidal waveform. In contrast, the current drawn by the prototype reversible rectifier employing the simple hysteresis comparison scheme is nearly sinusoidal and the displacement power factor is unity, as shown in Fig.7-6.
Fig. 7-7 and Fig. 7-8 show the results with the ramp comparison technique, switching at 10KHz. Current distortion can be observed in Fig. 7-7 since $E_{dc}/V_{sm}$ is less than 2, resulting in $m > 1$ (see Eqn. (3.17)). An improved current waveform is obtained by increasing $E_{dc}/V_{sm}$ to 2.4, and is shown in Fig. 7-8. The template locked to the phase-to-neutral voltage of the mains is also shown in each diagram for comparison.

![Fig. 7-7 Input Current $i_{sA}$ Using Ramp Comparison Scheme with $E_{dc}/V_{sm} = 1.9$ (Input Current: 5A/div)](image1)

![Fig. 7-8 Input Current $i_{sA}$ Using Ramp Comparison Scheme with $E_{dc}/V_{sm} = 2.4$ (Input Voltage: 10V/div)](image2)

Fig. 7-9 and 7-10 show the input current waveform and the associated reference current waveform, using the simple hysteresis comparison technique and the ramp comparison technique, respectively. Comparison of these waveforms shows that the same amount of current is drawn from the mains under the same load, but the amplitude of the current reference in the ramp comparison scheme is less than the actual current and the phase shift is too small to be observable.
To test the transient response, the load discussed in section 7.2.4 was used. It was driven by a pulse generator in order to provide repeated reversals of the average load current, as specified in Fig.5-11. The results presented here refer to a system with the parameters, given as follows:

- d.c. link voltage: 65V
- a.c. line-to-line voltage: 42V (rms)
- Input Inductance $L_s$: 4mH
- D.C. Capacitance $C$: 1250μF
- Average Load Current $I_0$: 5A
- Proportional Gain $K_p$: 0.24
- Time Constant $T_1$: 0.003

The PI controller was first operated to control the d.c. link with the simple hysteresis comparison technique in a.c. current control. As shown in
Fig. 7-11, the steady state error of the d.c. link voltage was zero, as expected and the overshoot on the d.c. link voltage as well as the phase reversal of the input current is clearly shown. In other respects the observed behaviour is essentially the same as that predicted by simulation.

The overshoot can be reduced by injecting load information to the control loop. The behaviour under these conditions has also been observed and simulated. For the cases of good injection, shown in Fig. 7-12, the overshoots were \( \sigma_1 = 1.4\% \) and \( \sigma_2 = 0\% \) and the regulation times \( t_1 = 10\text{ms} \) and \( t_2 = 0 \). For comparison, the results with no load injection are shown in Fig. 7-11, where \( \sigma_1 = 6.6\% \) and \( \sigma_2 = 6.6\% \), and \( t_1 = 30\text{ms} \) and \( t_2 = 60\text{ms} \).
Experimental Results

Simulation Results

Fig. 7-12 Transient Response with Good Injection about the Load

Fig. 7-13 Transient Response with Under-Injection about the Load
Experimental Results

Simulation Results

Fig. 7-14 Transient Response with Over-Injection about the Load

behaviour under the imperfect load injection was also studied and shown in Fig. 7-13 and Fig. 7-14, respectively.

7.4 Transputer Based Control System

This section is concerned with a digital implementation of the control of the a.c. current using the current-forced scheme. Control of the d.c. link voltage has not been implemented in this digital system. The use of parallel processing techniques in control of the reversible rectifier by a INMOS transputer will be discussed and the experimental results will be shown.
7.4.1 Transputer Overview

A transputer is a single VLSI device with processor, its own local memory and communications links. Fig.7-15 shows a transputer architecture. An unique feature is the point-to-point serial communication links which provides full duplex communication with other transputers.

A transputer can be used either alone, in a single processor system, or in networks to build high performance concurrent systems. In this application, a single transputer (T800) is used to control the a.c. currents. Further expansion to an integrated a.c. drive system by using other transputers was envisaged, though this has not yet been proved. A single transputer is capable of supporting concurrency by means of a "hardware scheduler",

![Transputer Architecture Diagram](image)

enabling any number of tasks (processes) to be executed "concurrently" by automatically sharing the processor time among tasks. Indeed, for a single transputer this gives no increase in speed but it enables programs intended for use on a network to be developed and tested on one transputer.
7.4.2 Hardware

7.4.2.1 transputers and Transputer Development System

There are two transputers in the system — the target transputer and the master transputer. The target transputer board consists of an INMOS T800 20MHz transputer, 2 Mbytes DRAM, and boot/configuration routines stored in EPROM. It actually carries out control of the rectifier. The master transputer board (SMT101 'Sprint' Board) is a PC plug in board with an INMOS T425, providing the Transputer Development System [INMOS, 1989], with which application programs can be edited, compiled and run. This provides an environment for developing programs in Occam, a language especially suitable for parallel processing. The programs are configured to run on the target system, and are downloaded to there after having been developed on the master system.

7.4.2.2 I/O peripherals and interfacing [GOLDAK 1991]

The input and output peripherals, and the interface to the target transputer consist of:-

- an address decoder to access the I/O peripherals,
- a phase-locked loop and a counter, to monitor the phase angle of the mains,
- four fast analogue-to-digital converters to measure the a.c. currents, the d.c. link voltage and the load current.
During the concurrent execution of several tasks, each task proceeds asynchronously with the others, that is, each task proceeds at its own speed. Communication between tasks is via the links known as *channels*. The channels may be hardware links when the tasks are running in different transputers, or internal "software" links when the tasks are executed in a single transputer. The channels are one-way and self-synchronizing, so that communication only takes place when both the sending and receiving processes are ready. If one task becomes ready before the other, then it will automatically wait for the other, without any explicit command from the programmer. The only responsibility left with the programmer is that of avoiding *deadlock* by ensuring that the second task becomes ready sometime.

For example, in Fig.7-16, task A is handling input from an analogue-to-digital converter while task B computes a control output level. Task A reads the input from the converter, scales it and signals task B, via the link named `inf.sender`, that the input information is ready. Task B waits for the signal from task A, processes the input data to generate the control output level, then signals task A, via the link `inf.echo`, that it has completed the processing and waits again for the signal that another batch of input data is ready. The two tasks may be executed in parallel, that is, task A may be handling a second batch of input signals at the same time as task B is processing the control level based on the first batch of input data. The signals sent between the tasks via the links allow the tasks to synchronize their activities so that task B does not start computing the control law before task A has finished processing its data input. If tasks
A and B are executed by two transputers in the network the links *inf.sender* and *inf.echo* would be the hardware links, as shown in Fig.7-15, otherwise the links would be the internal "software" link.

Fig.7-16 Communication between Two Tasks by the Link

7.4.4 Occam Structure Implementing Control of the A.C. Current

The implementation of the a.c. current control by the current-forced scheme includes:-

- measurement of the a.c. currents (in two of three phases)
- measurement of the phase of supply voltage and generation sinusoidal references for three-phase currents
- tracking control

Several tasks are used to carry out the implementation and the structure is shown in Fig.7-17.

Task 1 Interrupts

This task is responsible for receiving start/stop instructions from the master transputer and send an interrupt signal to all other tasks in order to
terminate the execution of the tasks. Once a task has been executed an interrupt signal has to be sent to it when the "stop running" instruction is received from the master transputer.

**Task 2 Buffer**

The use of buffers to decrease the coupling between active processes is a common feature of concurrent programming languages. This buffer (task2) decouples tasks 3 and 4, allowing them to be executed asynchronously. The implication is that tasks 3 and 4, which actually carry out the control of the a.c. current, can each be executed at their own speed, but this is only true if the buffer is empty. Otherwise, the sender (task4) must wait until the receiver (task3) reads the previous value; that is, the rate of progress of the sender and receiver is linked.
Task 3  I/O control, time-out and output

This task carries out the Input/Output control and sends the switching signals to drive circuit, activating the power devices. For generating PWM signal, the task is to time-out the PWM pulse-widths.

Task 4  Input data and current control

This task reads the values of the a.c. currents and the amplitude of the reference current. Then, the a.c. control is processed. The proper switching functions are determined and then sent to task 3 through task 2.

The flowchart of tasks 3 and 4 implementing the predictive a.c. current control scheme (using standard modulation technique) is shown in Fig.7-18.

Tasks 3 and 4 are executed in parallel. Task 3 has the higher priority to ensure a correct timing for generating PWM pulses. After defining the variables and setting the sampling time [processes (1), (2)], task 3 is invoked either by the interrupt signal sent from the task 1, which will terminate the execution of task 3 [processes (4) and (5)], or by the sampling time-out signal, which will carry on the execution [processes (6),(7)...(15)]. The PRIority ALTeration construct of Occam ensures that the task be either terminated or executed, but the termination has a higher priority. When neither the interrupt signal [process(4)] nor time-out signal [process (6)] invokes it, task 3 is turned to an inactive state, allowing the the processor to deal with other active processes which have been on the list waiting to be executed. The transputer operates in such a
Fig. 7-18 Occam Structure Implementing the Predictive Control
Fig. 7-19 Occam Structure Implementing the Simple Hysteresis Control
way that inactive processes do not consume any processor time. With the sampling period being completed, task 3 becomes active again and the process (7) reads the switching patterns (switching vectors and times in one switching period) through communication with task 4 [process (22)] via the buffer task 2, immediately followed by sending the first zero vector $V_{z1}$ and setting the time $t_{z1}$ [process(8)]. Simultaneously, analogue-to-digital converters and a counter for detecting the phase angle of the mains are triggered and a signal which informs task 4 is sent directly through the channel named *time.signal*. This signal will start the execution of task 4, in order to calculate the switching patterns for the next sampling/switching period. Meanwhile, task 3 becomes inactive [process(9)], so permitting the processor to deal with calculations in task 4, and other processes, and remains so for time $t_{z1}$. Processes (10), (12) and (14) send the active switching vectors $V_{x}$, $V_{y}$ and the second zero vector $V_{z2}$ to the drive circuit, completing a switching cycle of the modulation. Afterwards, the task returns to process (7), reading in the next switching patterns and repeating the whole process.

The execution of task 4 is also illustrated in Fig.7-18. The ALTernation construct determines whether execution or termination is being invoked. The process(18) is triggered by *time.signal* from task 3 [process(8)], which ensures that the a.c currents and the phase angle are ready to be read in. After reading the data, the reference current is generated, followed by calculation of the switching patterns for the next switching/sampling period based on Eqn.(4.20) and (4.21) [processes(19)~(21)]. Task 4 will be made inactive after the calculated switching patterns are sent to the buffer task 2 [process(22)], ultimately being read by process (7) in task 3.
Fig. 7-19 shows the flowchart implementing the simple hysteresis a.c. current control. Task 4 determines the switching functions based on the hysteresis comparison [process(21)~(22)] and task 3 sends out the switching functions at every sampling time [process(26)].

7.4.5 Experimental Results

Fig. 7-20 shows the experimental results obtained with employing the predictive control scheme [see section 3.5]. The rectifier was switched at a fixed frequency of 10KHz. In comparison with the results in Fig.7-6 and Fig.7-8, a better current waveform was observed in spite of the distorted supply voltage, because the pure sinusoidal template was generated by looking up a pre-calculated sine table. Thus the distortion due to the imperfect supply voltage waveform in the analogue implementation was avoided.

Fig.7-21 shows the a.c. line current waveform together with the corresponding phase voltage, obtained by using a simple hysteresis comparison. It should be noted that the switching in this case is dependent not only on the hysteresis band but also on the frequency of sampling, time delay of the processing and the resolution of the analogue to digital converters.

7.5 Summary

This chapter presents the implementation of the reversible rectifier and its control systems. The work reported here has confirmed the feasibility of reversible rectifiers, and indicated that good current waveforms can be drawn in both rectifying and inverting modes. The observed behaviour of the
prototype reversible rectifier as well as its control system was essentially the same as that predicted by simulation, so supporting the theoretical studies in the previous chapters.

Fig. 7-20 Input Current Using the Predictive Scheme

(Input Current: 5A/div)

Fig. 7-21 Input Current Using the Simple Hysteresis Scheme

(Input Voltage: 10V/div)
8.1 Introduction

In this concluding chapter, a review of the most important points of this dissertation is given. Recommendations for future work on reversible rectifiers are drawn.

8.2 Review of the Dissertation

The work reported has demonstrated that considerable improvement in the input current waveform and the power factor, plus the ability to regenerate high quality power, can result from replacing a conventional three-phase bridge rectifier by a reversible rectifier. Three major problems of a conventional bridge, namely, (i) distorted a.c. current waveform, (ii) poor power factor, and (iii) uni-directional power flow, can be solved simultaneously.

In contrast to the matrix converter, which offers similar benefits, the combination of reversible rectifier and conventional inverter shows good commercial potential in the near future. This is because implementation of such a system is cheaper, in part because the power circuit configuration as well as much of the control scheme is similar to that of the inverter, with which most engineers are familiar.
The decision to employ reversible rectifiers rather than dissipative regeneration and filters for waveshaping as discussed in Chapter 1 depends on the additional equipment cost versus the savings on energy recovered, and the desirability of sinusoidal currents as well as unity power factor operation.

Special problems relevant to the control of the reversible rectifier have been discussed in this dissertation, and it is believed that guidelines for designing a suitable control system in practical applications have been given.

The emphasis in the dissertation has been on the current-forced schemes, and the means of controlling the a.c. current and the power flow. It has been shown that direct control of the a.c. currents by monitoring them and forcing them to follow a template can provide better stability and transient performance than the alternative, apparently simple, voltage-forced scheme (indirect control of the currents), and so allow simple implementation. In theory, however, by properly calculating the terminal voltage (using the differential term \( L \frac{dI}{dt} \)), the performance of the voltage-forced scheme may be improved to become comparable with current-forcing, but, in practice, the control system becomes more complicated. The decision whether to employ voltage-forced rather than current-forced depends on the degree of need for a wide range of stability, and on the balance between the additional cost of the control system and savings on the current sensors. In general, for low and medium power rating applications, current-forced schemes are preferable to the voltage-forced schemes.
The discussion in Chapter 3 suggested that the simple hysteresis comparison and the ramp comparison are the preferred current-tracking techniques if analogue control is chosen, whereas the predictive control scheme using space vector modulation technique is the best choice for a digital system. It is believed by some researchers that the variable switching frequency of hysteresis comparison schemes may cause some problems, such as audible noise as shown in the frequency spectrum, and make electromagnetic interference more difficult to control. The ramp comparison and the predictive scheme can provide a constant switching frequency; the former can be implemented at a low cost but has some tracking errors, whereas the latter has a better steady state performance but requires a digital system, which increases the cost of the system.

The power flow control is usually carried out by monitoring the d.c. link voltage, together with the injection of the load information if it is available. The stability analysis in Chapter 5 has resulted in a method for designing a suitable PI controller, an aspect which has not been addressed before. Some important conclusions can be drawn as follows. Firstly, the stable region for regeneration is wider than that for rectification, that is, if the control system is stable in the rectifying mode under the specific condition it is also stable in the regenerative mode. Therefore, for the purpose of designing the PI controller to achieve stable response, it is only necessary to consider the rectifying mode. Secondly, the proportional gain $K_p$ of the PI controller can be the first parameter to be determined, since it is independent of the integral part $T_i$. Then, $T_i$ can be selected. The equations for selecting $K_p$ and $T_i$ are given in Eqn.(5.6) and (5.7). Thirdly, the transient response of the control
system can then easily be examined by means of simulations under the specific load conditions. Injection of load information can reduce the overshoot of the d.c. link voltage due to the change of the load, particularly effective when the rectifier is operated from regeneration to rectification.

A sliding mode control scheme discussed in Chapter 6 provides a novel scheme with which the transient behaviour of the reversible rectifier may be determined analytically. Preliminary research has shown the characteristics of such a novel control scheme.

For experimental purposes, a 1kW reversible rectifier using power MOSFETs was constructed and tested. In order to investigate different control schemes practically, both analogue and digital control systems were built. The experimental results confirmed the feasibility of reversible rectifiers, and indicated that good current waveforms can be drawn in both rectifying and regenerative mode. The implementation of digital control, incorporating a transputer system, allows more complex control algorithms to be used and the possibility is also opened of closer integration of the control of the rectifier with that of the machine in the future.

8.3 Discussion of Future Work

8.3.1 Control Scheme Using Theory of Variable Structure System

In Chapter 6, a novel control system, termed sliding mode control, was investigated, based on the basic principle of the theory of variable
system. Future work on sliding mode control might include the following:

(i) investigation of existence of the sliding mode under the switching algorithm described in Chapter 6, (ii) investigation of other predefined trajectories (or super surfaces) along which the system slides and corresponding switching algorithms which ensure the existence of sliding modes, and (iii) practical implementation.

8.3.2 Reactive Component Minimization/Optimization

In the previous chapter (section 7.2.2) a method of selecting suitable values for the reactive components has been suggested. But optimization of these reactive components is still open to investigation. A problem concerns the power loss in the input inductors, an aspect which has not been discussed in this dissertation. Both theoretical and practical investigations about this topic should be made in the future.

8.3.3 Electromagnetic Interference (EMI)

As remarked in Chapter 1, rapid changes in voltages and currents within a switching converter are a source of electromagnetic interference (EMI) with other equipment as well as possibly preventing its own proper operation. There are various standards that specify the maximum limit on the EMI [ANGSTENBERGER 1992]. This is an area which clearly requires attention if practical reversible rectifiers are to be built. The EMI problem produced by the power conversion with reversible rectifier/inverter arrangement will have to be investigated in the future.
The most effective way of eliminating EMI is to prevent it from being generated at source. Some methods have been suggested [MOHAN 1989], including:—

(i) the use of snubbers in the power circuit, which reduce both the $dv/dt$ and the $di/dt$ of the circuit, or the use of the resonant link,

(ii) proper mechanical layout, wiring, and shielding, and (iii) use of EMI filters.

An EMI filter would be placed in the input line, and it then becomes natural to consider the filter and the selection of the input inductance together. It has been seen that reduction of the input inductance will increase $di/dt$ as well as the total harmonic distortion in the a.c. current. It would be interesting to investigate the use of small values of input inductance (less than 1mH), together with a proper input filter to remove the additional current ripple and to also eliminate the conducted EMI.

8.3.4 Applications and Practical Considerations

One aspect requiring further study is the integration of the control of the rectifier with that of the machine, more interestingly, in conjunction with a transputer network.

Although the reversible rectifier has been viewed as a component of an integrated drive system, the possibility of allowing it to provide current-shaping to the other electronic equipment connected nearby seems very attractive. Moreover, applications of the reversible rectifier are not limited to a.c. drive systems. There have been a few reports of applications of reversible rectifiers in other areas, such as VAR
compensators [AKAGI 1990], power supplies for magnets of particle accelerators [CISCATO 1991], and HVDC transmission [Ängquist 1991].

It was also thought that the influence of an asymmetrical supply on the reversible rectifier should be investigated. At the time of writing this was being undertaken by a colleague at the University of Surrey [BAKRAN 1992]. Good progress is being made, and it may be that no further questions of significance will remain.
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APPENDIX I  SWITCHING FREQUENCY OF HYSTERESIS COMPARISON
FOR A SINGLE-PHASE REVERSIBLE RECTIFIER

With reference to Eqns.(2.1) and (2.2), the slopes of the current $i_s$ are determined as:

$$\frac{di^+_s}{dt} = \left[ v_s(t) + \frac{E_{dc}}{2} \right] / L_s \quad t_n < t < t_n + DT_s \quad (A-1-1)$$

$$\frac{di^-_s}{dt} = \left[ v_s(t) - \frac{E_{dc}}{2} \right] / L_s \quad t_n + DT_s < t < T_s \quad (A-1-2)$$

where $i^+_s$ and $i^-_s$ represent $i_s$ in the increasing and decreasing period, respectively, and $D$ is the duty cycle of one arbitrary switching period.

From the Fig.A-1, the followings are obtained:

$$\frac{\Delta i}{DT_s} = \frac{d(i^+_s - i^-_s)}{dt} \quad |t = t_n| = \left. \frac{di^+_s}{dt} \right|_{t = t_n} - \left. \frac{di^-_s}{dt} \right|_{t = t_n}$$

$$= \frac{v_s(t) + \frac{1}{2} E_{dc}}{L_s} \quad \left. \frac{di^+_s}{dt} \right|_{t = t_n}$$

$$\left. \frac{\Delta i}{DT_s} = \frac{d(i^-_s - i^+_s)}{dt} \quad |t = t_n + DT_s| = \left. \frac{di^-_s}{dt} \right|_{t = t_n + DT_s} - \left. \frac{di^+_s}{dt} \right|_{t = t_n + DT_s}$$

$$= \frac{v_s(t + DT_s) - \frac{1}{2} E_{dc}}{L_s} \quad \left. \frac{di^-_s}{dt} \right|_{t = t_n + DT_s}$$

Note that the switching frequency is much higher than the frequency of the mains, thus:

A- 1
Fig. A-1 Determination of the Switching Frequency of Hysteresis

Comparison for a Single-Phase Reversible Rectifier

\[ V_n(t) = V_n(t + DT) \]

\[ \frac{di_{n}^{*}}{dt} \bigg|_{t=t_n} = \frac{di_{n}^{*}}{dt} \bigg|_{t=t_n + DT_n} \]

(A-1-5)

Substituting Eqn.(A-1-1) to Eqn.(A-1-3), and Eqn.(A-1-2) to Eqn.(A-1-4), and considering Eqn.(A-1-5) yields:

\[ DT_n = \frac{\Delta i_h L_s}{\left[ v_n(t_n) + \frac{E_{dc}}{2} \right] - L_s \frac{di_n^{*}}{dt} \bigg|_{t=t_n}} \]

(A-1-6)

\[ (1-DT_n) = \frac{-\Delta i_h L_s}{\left[ v_n(t_n) - \frac{E_{dc}}{2} \right] - L_s \frac{di_n^{*}}{dt} \bigg|_{t=t_n}} \]

(A-1-7)

The instantaneous switching frequency can be obtained:

\[ \text{A-2} \]
\[ f_s = \frac{1}{T_s} = \frac{\left(\frac{E_{dc}}{2}\right)^2 - \left(\frac{v_s(t) - L_s \frac{di_s}{dt}}{L_s \Delta i_h E_{dc}}\right)^2}{L_s \Delta i_h E_{dc}} \]

where \( i_s^* = g_m v(t) \)

In general, \( |v_s(t)| \gg g_m L_s |dv_s(t)/dt| \) since \( g_m L_s \ll 1 \). Eqn.(A-1-8)

becomes:

\[ f_s = \frac{\left(\frac{E_{dc}}{2}\right)^2 - v_s^2(t)}{L_s \Delta i_h E_{dc}} \]

(A-1-9)

Let \( v_s(t) = V_{sm} \sin \omega t \), thus:

\[ f_s = \frac{E_{dc}^2 - V_{sm}^2}{4L_s \Delta i_h E_{dc}} - \frac{V_{sm}^2}{L_s \Delta i_h E_{dc}} \sin^2 \omega t \]

\[ = \frac{E_{dc}^2 - 2V_{sm}^2}{4L_s \Delta i_h E_{dc}} + \frac{V_{sm}^2}{L_s \Delta i_h E_{dc}} \cos 2\omega t \]

(A-1-10)

The maximum switching frequency is:

\[ f_{max} = \frac{E_{dc}}{4L_s \Delta i_h} \]

(A-1-11)

at \( \omega t = 0, \pi, 2\pi, \ldots \); and, the average switching frequency is:

\[ f_{avg} = \frac{E_{dc}^2 - 2V_{sm}^2}{4L_s \Delta i_h E_{dc}} \]

(A-1-12)

A- 3
APPENDIX II POWER EQUATIONS

Suppose there is no phase shift between the input currents and the mains voltages and consider only symmetrical condition, thus:

Input Voltages: \[ v_{sA} = V_{sm} \sin(\omega t) \]
\[ v_{sB} = V_{sm} \sin(\omega t - 120^\circ) \quad (A-2-1) \]
\[ v_{sC} = V_{sm} \sin(\omega t + 120^\circ) \]

Input Currents: \[ i_{sA} = I_{sm} \sin(\omega t) \]
\[ i_{sB} = I_{sm} \sin(\omega t - 120^\circ) \quad (A-2-2) \]
\[ i_{sC} = I_{sm} \sin(\omega t + 120^\circ) \]

The instantaneous input power is:

\[ P_{in} = \sum_{sJ} v_{sJ} i_{sJ} - R_s \sum_{sJ} i_{sJ}^2 - L_s \sum_{sJ} i_{sJ} \frac{di_{sJ}}{dt} \quad (A-2-3) \]

Note:

\[ \sin^2(\omega t) + \sin^2(\omega t - 120^\circ) + \sin^2(\omega t + 120^\circ) = \frac{3}{2} \]

and,

\[ \sin(\omega t)\cos(\omega t) + \sin(\omega t - 120^\circ)\cos(\omega t - 120^\circ) + \sin(\omega t + 120^\circ)\cos(\omega t + 120^\circ) = 0 \]

Therefore:

\[ \sum_{sJ} v_{sJ} i_{sJ} = \frac{3}{2} \frac{V_{sm} I_{sm}}{} \quad (A-2-4) \]
\[ \sum_{J=A,B,C} i_{sJ}^2 = \frac{3}{2} I_{sm}^2 \quad (A-2-5) \]

\[ \sum_{J=A,B,C} \frac{di_{sJ}}{dt} = \frac{3}{2} I_{sm} \frac{dI_{sm}}{dt} \quad (A-2-6) \]

Substituting Eqns. (A-2-4), (A-2-5) and (A-2-6) into Eqn. (A-2-3) yields:

\[ P_{in} = \frac{3}{2} \left( V_{sm} I_{sm} - R_s I_{sm}^2 - L_s I_{sm} \frac{dI_{sm}}{dt} \right) \quad (A-2-7) \]
APPENDIX III  AN EXAMPLE OF SELECTING PARAMETERS OF THE CIRCUIT AND THE PI CONTROLLER

Consider a 20KVA reversible rectifier connected to the 415v mains. Suppose the output current to be 25A and specify the total harmonic distortion in the input current to be less than 5%. A simple hysteresis comparison technique is selected in control of the a.c. current, with average switching frequency 10KHz.

(1) Determine the d.c. link voltage

The minimum value of the d.c. link voltage for the simple hysteresis comparison technique is equal to the magnitude of the line-to-line voltage of the mains, that is, 587v. If the d.c. link voltage is chosen to be 650v, 63v margin will be obtained, which allows the 9.7% voltage droop in the d.c. link voltage.

(2) Determine the input inductance

The relationship between the average switching frequency and \( \Delta i L \) is shown in Fig.A-3-1. It can be seen that \( \Delta i L \) should be approximately equal to 4 in order to obtain 10KHz switching frequency. Using the method presented in section 7.2.2.2, 1.5mH inductance and 2.7A hysteresis boundary are determined, with reference to Fig.A-3-2, which gives 3.7% total harmonic distortion in the a.c. current at the rated operating point.
(3) Determine the d.c. link capacitance and the parameters of the PI controller.

The value of capacitance is selected to be 400μF, using the method in section 7.2.2.2. For selecting the proper parameters of the PI controller, Eqns.(5.6) and (5.7) are then illustrated in Fig.A-3-3 and Fig.A-3-4, respectively. Suppose that the output current $i_{out}$ is regularly reversed, as shown in Fig.5-11, where $I_o = 25$ A, making $R_o$ equal to 26Ω. The point A
Fig.A-3-4 Stable Region for Time Constant $T_1$

on Fig.A-3-3 and the point B on Fig.A-3-4, corresponding to $K_p = 1.5$ and $T_1 = 0.004$, are the stable region and with a good margin of allowable change in load current.

The results of simulation using these parameters are shown in Fig.A-3-5 for the case of using PI controller only, which gives $\sigma_1 = 12.2\%$ and $\sigma_2 = 13.4\%$, and in Fig.A-3-6 for the case of including the injection of information about the load, which gives $\sigma_1 = 8.3\%$ and $\sigma_2 = 1.8\%$. It can be seen that the d.c. link voltage is dropped below the minimum value required, as the rectifier operates from the regenerative mode to rectifying mode, if only the PI controller is used. The distortion in the a.c. current can be observed. To eliminate the large variation of the d.c. voltage, it is desirable either to increase the capacitance together with redesigning the PI controller or to inject the information about the load, as shown in Fig.A-3-6.
Fig.A-3-5 Transient Response with
PI Controller Only
(Top Trace: $E_{dc}$
Bottom Trace: $v_{sA}$ and $i_{sA}$)

Fig.A-3-6 Transient Response with
Injection about the Load
APPENDIX IV  CIRCUIT DIAGRAMS