Exploring System-on-Panel Integration for Next-Generation Display Applications

Xiaojun Guo

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Nano-Electronics Centre Advanced Technology Institute University of Surrey Guildford, Surrey, GU2 7XH, United Kingdom.

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For my parents and Qian
Abstract

Following the advent of the digital multi-media era and the popularity of the internet, high-resolution flat-panel displays are becoming the central feature of many consumer products. This dissertation is to explore the challenges and opportunities of system-on-panel (SoP) integration for next-generation high-performance multifunctional flat-panel display products. SoP integration, which aims to mount a display screen and its analogue and digital display driver circuits as well as other high-level function integrated circuits (ICs) on the same glass substrate, will help realize the implementation of high-density, multifunctional, compact display products, and also lead to a substantial savings in costs by shortening the display manufacturing and inspection processes while maintaining a level of high reliability.

This dissertation makes contributions on three aspects. Firstly, the dissertation explores the device structure and related design implications for the continuous down-scaling of polycrystalline silicon (poly-Si) thin-film transistors, which is the most promising candidate for building ICs in SoP integration. The thick source/drain nanometre-scale ultra-thin channel poly-Si transistors are demonstrated with desirable performance and ultra-scaling capability in this work. The further analysis by numerical device simulation gives the implications for optimal design of poly-Si TFTs down to sub-100-nm regime. The second contribution is to design and analyze the pixel circuits for the self-emissive type display technologies, i.e. organic light emission diode (OLED) and carbon nanotube (CNT) based field emission displays (FEDs). The merits and related design issues of the switch-current pixel circuits are fully studied. And to integrate the light element devices into SPICE circuit simulations, a simple and effective macro-modelling approach is proposed. Finally, this dissertation also investigates the electro-thermal effects in SoP integration. The analysis results show the much more severe electro-thermal effects in SoP integration compared to that of conventional bulk CMOS and SOI technologies. Possible heating removing and management methods are given for the progress of reliable SoP integration.
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(iii) Hybrid technology and system integration

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Chapter 1

Introduction

1.1 Motivation of this Work

1.1.1 Display Technologies and Integration Limits

![Diagram comparing OLED and CNT-FED to LCD](image)

*Figure 1.1: Illustration of the inherent merits of OLED and CNT-FED compared to LCD, which make OLED and CNT-FED display technologies may take the place of LCD in future markets.*

Following the advent of the digital multi-media era and the popularity of the internet, high-resolution flat-panel displays are becoming the central feature of many consumer products, from camcorders, mobile phones, to notebook PCs. The
flat-panel industry has been dominated by liquid crystal displays (LCDs). LCD technology is advancing so rapidly that it seems difficult for other technologies to compete in the marketplace, despite all of the enthusiasm and innovation that is emerging from research laboratories in both universities and industry for decades. However, as shown in Fig. 1.1, with the inherent merits compared to LCDs, self-emissive display technologies like organic light emitting diodes (OLEDs) [1], and carbon nanotube (CNT) based field emission displays (FEDs) [2] are promising to take the LCD's place in the market. This will be possible if proponents work together to identify and remove the barriers to improved performance and commercialization.

At the same time, the tremendous advances of display technologies make the system integration more and more important to further improve the performance of display products with design constraints in weight, cost and power. The conventional approach is to mount the display screen and discrete electronic components like packaged integrated circuits (ICs), resistors, capacitors, inductors and various other passive elements, onto a printed circuit board (PCB). Various kinds of loss exist in the module because the system has to transfer huge amounts of data through the off-chip interconnect wires at high frequency, which in turn limits the signal bandwidth that the system can achieve. A discrete IC solution also causes high cost due to the complicated assembly processes. Therefore, a new integration solution is pursued to overcome the limits in cost and performance for PCB based display products.
1.1.2 System-on-Panel Integration

In order to obtain an even higher level of display product performance and to further lower costs, an encouraging integration design called "System-on-Panel (SoP)", is proposed by Sharp [3], which aims to mount a display screen and its analogue and digital display driver circuits as well as other peripheral function ICs including power supply, memory, CPU, video, audio, touch sensitivity and communication interface on the same glass substrate panel, as shown in Fig. 1.2. Compared to the standard PCB approaches, SoP integration eliminates the traditional "attachment" and "packaging" steps, and reduces the power consumed in the data communication. SoP designs will help realize the implementation of high-density, multifunctional, compact display products, and also lead to substantial savings in costs by shortening the display manufacturing and inspection processes, while maintaining a high level of reliability.

With low temperature processing (500°C or lower), SoP establishes a viable manufacturing technology, which could not only result in lower cost electronics for certain applications, but fabricate devices over large areas on cheap substrates such as glass, or even plastic film to provide a distributed, yet integrated, electronics capability for large area applications [4]. As this technology matures, we can look forward to ultra-compact system-on-glass, system-on-plastic products in the future, like super high-definition Hi-Vision Projectors, multimedia-ready ultra-compact...
personal information tools, pocket-size audio-visual equipment, E-book, ultra-slim
digital cameras, artificial-skin, etc..

1.2 Requirements and Challenges for SoP Integration

![Figure 1.3: Front- and back-end technologies and design methodologies for achieving high-performance SoP products.](image)

To achieve real SoP products with high-level performance, all front- and back-end technologies and design methodologies, as summarized in Fig. 1.3, are required to be developed. Since SoP integration is analogous to the conversion from hybrid circuit technology to IC technology, most of the silicon IC industry's existing expertise in analogue/digital, mixed-signal circuits and systems design can be adopted in the SoP applications. This scenario, however, requires the development of device technology at a level analogous to that of the IC industry, and new display solutions in addition to LCD to meet the system integration requirements and application demands, and to fulfill the growing demands for display products with high image quality, lower cost, and also robustness. When high performance ICs being integrated into the glass or plastic substrate, the resultant effects on the system performance and reliability are required to be seriously re-considered, since
both the physical and electrical properties of such substrates are quite different from that of silicon wafers. In the following subsections, these issues are briefly discussed.

1.2.1 Thin-Film Transistors

Thin-film transistors (TFTs), which have a structure similar to that of traditional silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect transistors (MOSFETs), but use amorphous silicon (a-Si) [5], low-temperature polycrystalline silicon (poly-Si) [6], or organic/inorganic nanostructured semiconductor [7, 8] as the channel material, as shown in Fig. 1.4, show tremendous promise. Among all these alternatives, poly-Si enjoys a considerable advantage of benefiting from the mature silicon technology base, and has the capability to implement high performance complementary metal-oxide-semiconductor (CMOS) circuitry [9]. The substrate transfer techniques [10, 11] may enable one to build poly-Si devices and circuits on plastic substrates for flexible panel integration. However, poly-Si has many forms. Grain size can vary from the smallest extreme, i.e. a-Si in the zero
limit, to being infinitely large, i.e. crystalline silicon (c-Si). Not only can grain size vary, but the quality of the Si grain can vary as well. Temperature limitations that exist due to the thermal-sensitive nature of the substrate (i.e. glass) result in difficulties to improve the silicon film quality and thus prevent the device performance to a level as high as that of SOI MOSFETs. Fig. 1.5 illustrates the carrier mobility that can be achieved with different forms of silicon, i.e. a-Si, poly-Si, pseudo crystalline silicon (c-Si), and c-Si. The need for high mobility devices to achieve high-speed circuits and high-level integration makes the quality of poly-Si films of overriding importance.

![Figure 1.5: Schematic showing the electron mobility that can be achieved for different forms of silicon channel material.](image-url)
On the analogy of Si ULSIs, the minimisation of the TFTs is also quite vital for improving the device speed and drivability, and achieving high-performance, lower-power large-scale integrated circuits (LSIs) in SoP integration. Fig.1.6 illustrates both higher carrier mobility and smaller devices are required for achieving higher level SoP integration. While the conventional CMOS technology is approaching the physical scaling limits, there is still a huge space remaining for down-scaling of TFT devices. The improvement of material quality as well as the minimization of the devices will enable to build large and cheap high-performance ICs for applications in this rapidly growing field of macroelectronics [4].

1.2.2 Display Technologies

As mentioned in Section 1.1.1, OLEDs and CNT-FEDs can be the display solutions that may replace LCDs in the future to fulfill the growing demand for display products with high-performance. As these display technologies further advance towards even higher image quality, higher efficiency, and low power consumption,
the active-matrix architecture, which integrates light elements with transistor memory/driving circuits in each display pixel, will become the technology of choice. However, unlike LCDs, the light elements in both display technologies are current-driven devices. Consequently, the one-transistor pixel structure for active-matrix LCDs, as shown in Fig. 1.7, cannot be used in OLEDs and CNT-FEDs to provide the constant current and subsequently constant illumination in the pixel. In fact, a minimum of one switching TFT to program and store the data signal and one drive TFT to provide the current is required for these pixels. Hence, more design considerations of the pixel circuits for these two technologies are required.

![Diagram](image)

**Figure 1.7:** The one-transistor pixel circuit structure for LCDs. $C_{LC}$-capacitance of liquid crystal cell, $C_s$-storage capacitance.

### 1.2.3 Performance and Reliability Issues in SoP Integration

Unlike silicon, either glass or plastic substrates are electrically and thermally insulating. This may result in additional effects on performance and reliability for SoP integration that does not occur in conventional CMOS ICs.

The electrical insulation of the substrate can benefit SoP integration for complete elimination of substrate parasitic capacitance and signal crosstalk. However, the resultant floating body effect increases the output conductance of the TFTs and, therefore, in analogue circuit applications, reduces the maximum attainable gain, as well as the common mode rejection ratio. While, in digital
circuits, the floating body effect increases the power dissipation and slightly degrades the switching characteristics [12]. The floating body also results in the hysteresis effects, which may cause the circuits to function improperly [13].

In conventional CMOS and SOI technology based IC chips, a majority of the heat generated in the devices and circuits conducts through the silicon substrate, which is packaged and in contact with a heat-sink. However, for SoP integration on a glass or plastic substrate, with extremely-low thermal conductivity, the generated heat cannot be efficiently dissipated. The localised temperature rise then leads to a degradation of the device's characteristics, and may severely impact the circuit(s) and system performance and reliability. The electro-thermal issues need to be carefully investigated and managed for reliable SoP integration.

1.3 Scope of this Work

This dissertation is aiming at making contributions on three aspects to the progress of SoP integration for next generation display applications. The first objective is to explore the device structure and related design implications for the continuous scaling down of TFTs. The nanometre-scale ultra-thin channel poly-Si transistors are demonstrated with desirable performance and ultra-scaling capability in this work. Further analysis by numerical device simulations gives implications on optimal design considerations of poly-Si TFTs down to the sub-100-nm regime. The second objective of the dissertation is to design and analyze the pixel circuits for the self-emissive type display technologies, i.e. OLED and CNT-FED. The merits and related design issues of the switch-current pixel circuits are fully studied. And to integrate the light element devices into SPICE circuit simulations, a simple and effective macro-modelling approach is proposed. The final objective is to investigate the electro-thermal effects in SoP integration. The analysis shows the much more severe electro-thermal effects in SoP integration compared to that of
conventional bulk CMOS and SOI technologies. Possible heat removing and management methods are given for the progress of reliable SoP integration.

1.4 Organisation of this Dissertation

This dissertation is organized in seven chapters and three appendixes, as follows:

Chapter 2 gives a literature review of the technological evolution for achieving SoP integration, which covers four aspects including poly-Si TFT technologies, OLED and CNT-FED technologies, active-matrix addressing methods and the system integration.

Chapter 3 describes the simulation methods to be used in the study. This includes electrical and thermal simulations of semiconductor devices using a commercial Technology Computer Aided Simulation (TCAD) tool - Atlas, circuit simulation using the industry-standard circuit simulator - HSPICE and also a three-dimensional (3-D) finite-element method simulation with COMSOL Multiphysics for analysis of self-heating in interconnects and chip-level electro-thermal effects in SoP integration.

Chapter 4 presents the device structure and fabrication of nanometer-scale ultra-thin channel poly-Si transistors, and also investigates the electrical characteristics and carrier transport mechanisms for such devices. Detailed analysis via TCAD device simulations provides guidelines for designing extremely-scaled poly-Si TFTs.

Chapter 5 analyses the operation behaviour and related non-idealities of the switched-current (S-I) pixel circuits, and thus provide guidelines for optimal design of S-I pixel circuits for high performance active-matrix OLED displays and CNT-FEDs. The analysis is based on the current-copier circuit configuration, and can be extended to other S-I pixel circuits. A macro-modelling approach for modelling the non-standard emission devices and a simple circuit model to emulate the operation of a pixel in the display matrix are also proposed.
Chapter 6 highlights the very pronounced electro-thermal effects in SoP integration compared to that of CMOS bulk and SOI technologies. The analysis shows that the electro-thermal effects, if not properly addressed, may severely restrict design metrics including performance, reliability and cost. Possible heat removing methods in SoP integration are introduced.

Chapter 7 provides an overall conclusion of this thesis. The results are summarised and several suggestions for future research directions are offered.
Chapter 2

Technological Issues and Evolution for SoP Integration – A Literature Review

2.1 Introduction

SoP integration not only helps compress the display system into a smaller “electronic” footprint, which then allows greater freedom in aesthetic and ergonomic design and make the assembly more robust and reliable, but also enables a whole new generation of ‘intelligent’ displays, which can handle and manipulate the information by themselves. However, to integrate the functional ICs to perform signal processing, computing and information storage on non-silicon temperature-sensitive substrates (glass or plastics), it is required to improve the TFT performance to be comparable to that of c-Si MOS transistors, to develop the process of fine design rules down to deep-submicron or even nano-scale regime, and also develop reliable design methodologies and integration technologies for high-performance circuits and systems. As poly-Si TFT technology improves and the carrier mobility increases, integrating more system functionality directly onto the glass substrate during the cell-fabrication process will be feasible. Some new display solutions in addition to LCDs are also required for further enhancement to fulfil the growing demands for display products with higher brightness, higher resolution, better colour reproducibility, full moving picture capability, lower cost, and also robustness to severe environment and temperature conditions. OLED displays and CNT-FEDs are emerging as two promising candidates. With further advance of display technologies toward even higher
image quality (e.g. higher resolutions, more colours, higher brightness etc.), and the active-matrix architecture, which integrates emission elements with transistor memory/driving circuits in each display pixel, has become the technology of choice. In SoP integration, due to the insulating substrate with poor thermal conductivity, the generated heat at devices and circuits can not be efficiently dissipated. The localized temperature rise may lead to a degradation of the device's characteristics, and the circuit and system performance. Such thermal issues are required to be investigated for reliable and high performance SoP integration.

In this chapter, the device physics and technological advances of poly-Si TFTs are reviewed in Section 2.2. In Section 2.3 the self-emissive display technologies, including OLED and CNT-FEDs, are described. The active-matrix addressing methods for both display technologies are presented in Section 2.4, followed by the introduction of possible thermal effects in SoP integration in Section 2.5. Finally, the literature is summarised.

2.2 Physics and Technology of Thin-Film Transistors

As described in Chapter 1, a poly-Si TFT is a type of SOI MOSFET but using the poly-Si thin film as the channel material, which can be processed at temperatures below the melting point of the substrate. It has all the advantages of a SOI device: fabrication simplicity, strong latch-up immunity and possible high packing density. However, in poly-Si TFTs, the presence of grain-boundaries (GBs) in the poly-Si film severely degrades the device performance, namely, the mobility is lowered, the threshold voltage and leakage current are increased, and the stability is deteriorated [14]. In the past, significant effort has been devoted to the poly-Si crystallization technology to enlarge the grain size for high-quality poly-Si films [15-17], while scaling-down of the device gate length is also pursued as a more straightforward route to reduce the GBs in the channel region, and improve the device speed and drivability for achieving higher-performance, low-power ICs based on poly-Si materials [18, 19]. In this section, physical models of grain-
boundaries in poly-Si films are firstly introduced. Then the poly-Si crystallisation
techniques and device scaling for improving the device performance are presented
in detail.

2.2.1 Grain-Boundary Models

Poly-Si is composed of silicon crystallite grains with a GB between two grains. At
GBs, grains of different crystallographic orientation meet, creating lattice mismatch.
The resulting mismatch causes disruptions in atomic arrangements and several
crystallographic defects, such as vacancies, bended, strained and broken bonds,
and dislocations [20]. The nature of the GB material can be considered to be
between that of a completely ordered single crystal and that of highly disordered
amorphous material, with its energy gap being somewhat larger than the energy
gap of the single-crystal material within the crystallites, and varying from one to
the other due to different structures. As a result, a heterojunction is formed at the
interface between a crystallite and a GB, with the GB material behaving as an
intrinsic wide-band-gap semiconductor [21]. Therefore, the effect of the GBs can be
modelled by rectangular potential barriers with width of \(W_g\) and height of \(\Phi_g\), as
shown in Fig. 2.1(b). \(W_g\) is approximately equal to the width of the GB. The GB is
also as an effective scattering centre for carrier transport, and the scattering
potential can be represented by the rectangular potential barrier [22].

The defect levels at GBs behave as traps for free carriers [23]. If it is n-type,
the GBs will predominantly trap electrons, and holes if p-type. The charging of the
traps at the GB implies a removal of free charges from the grain, leaving space-
charge regions (SCRs) near the GBs, thereby, creating additional potential-energy
barriers in the depleted regions on both sides of the GBs. Fig. 2.1 (a) and (b) depict
this situation for a n-type material. The additional space-charge potential is
\(q\phi\) below the GB rectangular potential barrier. The charge neutrality condition
establishes the potential width \(W\), as shown in Fig. 2.1.
Figure 2.1: (a) A cross-section schematic of an n-type poly-Si from top-view, showing charges at the grain boundaries (GBs), and the space-charge regions (SCRs) that surround them. (b) shows the conduction band diagram along the line AB depicted in (a).

Based on the above models, in order to move from one grain to another, the carriers have to either tunnel through a GB barrier or be sufficiently energetic to be thermally emitted over the barrier. Carrier transport in poly-Si film includes thermionic field emission through the space-charge potential barrier resulting from trapping effects (TFE1) and through the GB rectangular potential barrier (TFE2),
and also thermionic emission over these barriers (TE). In general, all of the above conduction mechanisms occur in parallel. However, at a given temperature or within a small range of temperatures, carrier transport is dominated by one or two of these processes. At very low temperatures only a few carriers have sufficient energy to surmount the parabolic barriers in the depletion regions, and current transport is dominated by TFE1. As the temperature is increased, the contribution of the carriers with sufficient energy to surmount the depletion-region barriers and tunnel through the much thinner GB barriers becomes more significant, and TFE2 dominates the transport process at intermediate temperatures. As the temperature is further increased, more carriers attain energies higher than the maximum height of the GB barriers, and TE dominates the transport process at high temperatures. Transport of carriers from one grain to the other require not only enough energy to overcome or tunnel through the potential barrier, but also an appropriate momentum in the second grain [24]. In other words, the quantum mechanical effect does not allow the incident carrier to exist in the second grain if no suitable state is available. This selection rule causes the reduction of carrier transmission. Considering the case of electron transport from one conduction band valley (valley \( a \)) to one of the valleys in the second grain (valley \( b \)). The transition from one wave vector \( k_a \) to the other different wave vector \( k_b \) usually occurs with either absorption or emission of a phonon. The phonon-assisted transition of carriers across a GB depends on the GB angles and the crystallographic orientations of two neighbouring grains.

### 2.2.2 Crystallization of Poly-Si

Poly-Si films can be either deposited directly in the polycrystalline phase, or transformed from another phase (i.e. amorphous Si) to polycrystalline by the supplement of energy (typically in the form of heat). To improve the device mobility, a variety of crystallization methods have been conceived in the past to improve the silicon film quality without exceeding the temperature constraints.
Directly deposited columnar poly-Si by low pressure chemical-vapour deposition (LPCVD) from silane gas was the material of initial interest in this area [25], but the small grain size and high density of defects of the films limit the application of the approach.

A remarkable improvement in poly-Si TFT performances was achieved by the low-temperature, solid phase crystallization (SPC) technology [26]. The pre-deposited a-Si films are converted into poly-Si by prolonged (10-100 hours) thermal annealing at temperatures between 530-600 °C. Due to the long processing time and high density of localised states not only at the grain boundaries but also within the grains in SPC poly-Si material, such technology is rather unsuitable for high performance TFTs.

To that end, laser-crystallisation technology seems more appropriate. The most commonly used laser crystallisation technique of a-Si on glass has been with rare-gas halogen excimer lasers [27]. Excimer lasers emit in the UV region (output wavelengths 193 nm, 248 nm and 308 nm for ArF, KrF and XeCl gas mixtures, respectively) with a short pulse duration (from 10 ns to 30 ns). The combination in Si of strong optical absorption of the UV light and small heat diffusion length during the laser pulse implies that high temperatures can be developed in the Si-surface region, causing melting, without appreciable heating (< 400 °C) of the substrate. This makes the excimer laser crystallisation (ELC) process compatible with glass or even plastic substrates. The poly-Si obtained also has a good crystallinity with very few in-grain defects, due to the melt-regrowth process. However, the film quality consistency and the narrow processing window to realize super lateral growth (SLG) for large grains have prevented the wide adoption of this technology. Recently, a family of laser-based crystallization technologies that are loosely classified as advanced lateral-growth crystallization schemes have rejuvenated the field of crystallization and provided directions for the formation of very high quality poly-Si films with sufficiently wide process window [15, 16, 28]. Some of the techniques can produce poly-Si films with nearly single-crystalline structure. TFTs with pseudo c-Si channels show the uniform and
excellent electrical characteristics that are closer to the conventional SOI MOSFETs [15, 29]. By taking advantage of the continuous grain (CG) silicon technology, which realizes pseudo c-Si TFTs in mass production, Sharp has succeeded in developing the first system panel, where a CPU, graphic controller, memories, and an audio circuit are monolithically formed on a glass substrate forming an full functional LCD [30], as shown in Fig. 2.2. The CPU based on the CG silicon technology was also transferred to a plastic substrate by stress-peel-off (SPO) process, and thus a flexible system panel can be achieved [31].

Figure 2.2: Photograph of glass substrate on which system panel is formed. [31]
2.2.3 Device Scaling

Table 2.1 Advantages of scaling down on device and circuit performances [32]

<table>
<thead>
<tr>
<th>Circuit or device parameters</th>
<th>Symbol</th>
<th>Scaling factor</th>
<th>Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply voltage</td>
<td>$V_{dd}$</td>
<td>$1/\kappa$</td>
<td></td>
</tr>
<tr>
<td>Drain Current</td>
<td>$I_o$</td>
<td>$1/\kappa$</td>
<td>$I_o(\kappa) = \frac{I_o}{\kappa} = \frac{V}{L/k} \left( \frac{V_{gs} - V_{th}}{k} \right) = \frac{I_o}{\kappa}$</td>
</tr>
<tr>
<td>Capacitance</td>
<td>$C_L$</td>
<td>$1/\kappa$</td>
<td></td>
</tr>
<tr>
<td>Conductance</td>
<td>$g_m$</td>
<td>$1/\kappa$</td>
<td></td>
</tr>
<tr>
<td>Sheet resistance</td>
<td>$\rho_s$</td>
<td>$\kappa$</td>
<td>$\rho_s(\kappa) = \rho_s(1/\kappa) = \kappa \rho_s$</td>
</tr>
<tr>
<td>Voltage drop across the signal lines</td>
<td>$\delta V$</td>
<td>$\kappa$</td>
<td>$\delta V(\kappa) = I(\kappa) \rho_s(\kappa) V(\kappa) = \kappa \delta V$</td>
</tr>
<tr>
<td>Line delay</td>
<td>$\tau_L$</td>
<td>$1$</td>
<td>$\tau_L(\kappa) = \rho_s(\kappa) C_L(\kappa) = \tau_L$</td>
</tr>
<tr>
<td>Power</td>
<td>$P_w$</td>
<td>$1/\kappa^2$</td>
<td></td>
</tr>
<tr>
<td>Power and delay products</td>
<td>$P_w \cdot \tau_L$</td>
<td>$1/\kappa^2$</td>
<td>$P_w(\kappa) \tau_L(\kappa) = P_w \tau_L / \kappa^2$</td>
</tr>
</tbody>
</table>

A scaling of the transistors means a proportional minimization of device dimensions, patterned geometries, and the power supply voltage. This is the most straightforward route for poly-Si TFTs to reduce the GBs in the channel region, and improve the device speed and drivability for achieving low-power, high-performance and high integration ICs. The advantages of the scaled-down structure on device and circuit performance are very large as shown in Table 2.1, where performance is illustrated as a scaling factor $\kappa$. It is noticed that the scaling concept yields high circuit performance, that is, a power-delay product of $P_w \cdot \tau_L = 1/\kappa^2$ [32].

Recently, combining the factors of the Schottky-barrier (SB) source/drain, metal gate, and thin effective gate oxide thickness (EOT) to fabricate deep-submicrometer TFTs, TFTs with low threshold voltage, low subthreshold swing, high transconductance, low S/D resistance, high on/off current ratio, and good control of
threshold voltage down to 0.1-μm gate length have been demonstrated [19]. However, the industry TFT technology is still far behind this. If assuming the TFT technology can achieve similar trends to that of CMOS technology, it is expected that the 0.1 μm technology node can be reached by 2018, as shown in Fig. 2.3.

The low processing temperature requirement for TFTs also impacts the gate insulator (GI) film. The quality of the GI film affects critical device aspects such as the switching speed (i.e. subthreshold slope), the threshold voltage and the leakage current. These parameters have significant impact on the aspects of circuits fabricated with TFTs and need to be controlled within tight specifications. Especially, as the devices being scaled down, it is required to achieve high-quality, uniform and very thin GI layers over large area. New GI material process technologies are required to be developed to improve bulk and interface characteristics. This will not be the scope of this dissertation, and details about electrical properties and processing of high quality GI material can be seen in [33].

Figure 2.3: The predicted scaling trend of poly-Si TFT technology compared with the scaling trend of Intel CMOS technology.
2.3 Organic Light-Emitting Diode

Since the first observations of light emission in small molecule based organic light-emitting diodes (OLEDs) [34], there has been increasing interest in their applications to flat panel displays due to the advantageous characteristics of OLEDs for displays include high efficiency, wide viewing angle, fast response, potentially low cost and flexibility. Over the past decade, the OLED display technology has made rapid progress, and various types of OLED displays have been demonstrated or commercialized. Further advance of OLED display technologies toward even higher image quality (e.g., higher resolutions, more colours, higher brightness etc.), higher efficiency, and low power consumption, in general, impose requirements in various aspects of the technology, including OLED materials with higher efficiencies and longer lifetimes, advanced OLED device structures that would give better optical and electrical performances (e.g., higher efficiencies, more saturated colours, higher contrast, lower voltage, high integration capability for active-matrix displays etc.), providing better display performances (e.g., better uniformity, more grayscales, etc.) [35].

2.3.1 Materials and Basic Device Structures

The basic structure of an OLED consists of a thin film of organic electroluminescent (OEL) material sandwiched between two electrodes, as depicted in Fig. 2.4 (a). The anode is transparent and is usually made of indium tin oxide (ITO), while the cathode is reflective and is made of metal. When a voltage is applied between the electrodes, charges are injected into the organic material, holes from the anode and electrons from the cathode. Then, the charges move inside the material, generally by hopping processes and recombine to generate light, as shown in Fig. 2.4 (b).
Cathode (i.e. metal)

Organic Stack

Anode (i.e. ITO)

Substrate (i.e. glass, plastic or foil ... )

Figure 2.4: (a) A basic structure of an OLED; (b) Illustration of the operation mechanisms of an OLED.

For efficient hole injection from the anode, a low barrier is required with respect of the highest occupied molecular orbital (HOMO) level of the organic material (typically 5–6 eV). ITO is usually used for the anode because of its high work function as well as its good transparency in the visible range. Hole injection is further enhanced by oxygen plasma treatment of the ITO. On the cathode side, a low barrier for electrons is needed in respect of the lowest unoccupied molecular orbital (LUMO) level of the organic material (typically 2–3 eV). Low work function metals such as Ca and Mg are required but they are very sensitive to moisture, and more stable cathodes have been introduced, such as Mg/Ag alloys or Al in
combined with alkali metal compounds [36]. A thin LiF layer (~1 nm) capped with a thicker Al layer is widely used as the cathode, and many other insulating layers such as CsF, MgO, Al₂O₃ and NaCl have been studied in order to enhance electron injection [36].

The choice of organic materials and the stack structure also determines the device’s performance features: emitted colour, operating lifetime and power efficiency. Two types of organic materials are used: small molecules (SM-OLED) and polymers (PLED). The electroluminescence performance is generally very similar for the two classes of material and the main difference is the deposition process of the thin organic film. While SM materials are generally deposited by evaporation under vacuum (referred to as a ‘dry process’), PLED materials are processed from solutions (a ‘wet process’). Devices based on SM materials allow more layer engineering and more sophisticated architecture compared with PLED devices. The historical evolution of the organic material layer structure is shown in Fig. 2.5. More and more layers have been used with specialized functions such as the hole injecting layer, hole transporting layer, hole blocking layer, emitting layer, and electron transporting layer. It has been shown that the electroluminescence efficiency of OLEDs can be increased by carrier or exciton confinement within a multilayer device [37]. In comparison, the PLED technology uses a simpler structure, which consists of two or three polymer layers only. More recently, a very promising approach for low power display technology has been demonstrated by combining electrically doped transport layers and a phosphorescent-doped emitting layer in a diode structure called a p-i-n junction [38].
2.3.2 Advanced Device Structures

To improve the performance of active-matrix OLED displays (AMOLEDs), top-emitting, inverted and high contrast OLEDs were developed in the literature. These device structures enhance display performances, such as aperture ratio of pixels, integrated capability with high performance pixel circuits, emission efficiency, and contrast.

A. Top-Emission OLEDs

Conventional OLEDs (Fig. 2.4(a)), adopting reflective top metal cathodes, transparent bottom anodes and transparent substrates, are bottom-emitting devices which emit light from their bottom surface (substrate). In AMOLED displays, however, the pixel circuits of opaque transistors below the OLEDs block emission from a significant portion of the pixel area, reducing the aperture ratio of pixels [Fig. 2.6(a)]. OLED displays with lower aperture ratios would require higher OLED current densities to achieve desired display brightness, which are
detrimental to the efficiency and lifetime of OLED operation. Top-emitting OLEDs, i.e., OLEDs that emit light from the top surface of devices remove such constraints, and therefore render feasible the fabrication of OLED displays on opaque substrates and also permit use of more complicated pixel circuits in AMOLEDs for higher display quality yet without sacrificing aperture ratios of pixels. As shown in Fig. 2.6 (b), Top-emitting OLEDs, in general, are composed of a reflective bottom anode, organic layers, and a (semi-)transparent top cathode for light out-coupling. The major challenges for making efficient top-emitting OLEDs are to develop transparent top cathodes with effective electron injection and to develop the reflective bottom anode with efficient hole injection, which were thoroughly reviewed in [35].

Figure 2.6: Schematic diagrams showing the cross sections of AMOLED displays with: (a) top-emitting and (b) bottom-emitting configurations. (Adopted from [35])
B. Inverted Structure OLEDs

Figure 2.7: Cross section of the AMOLED using an n-type transistor to drive the inverted OLED. (Adopted from [35])

Whatever the detailed AMOLED pixel circuit, there is at least one transistor (i.e., the driving transistor) in series with the pixel OLED, working as a voltage-controlled current source (VCCS) to supply a constant current independent of OLED operation. The remaining part of the pixel circuit controls the gate voltage of the driving transistor. With the conventional OLED structure, it is only possible to form the VCCS configuration with the p-type transistor. Indeed there is a strong desire to form the VCCS configuration with the n-type transistor, since usually the n-type transistors have performances significantly superior to those of p-type transistors. For instance, in a-Si TFTs often used in large-scale AMLCDs and AMOLEDs, only n-type transistors are available, while in poly-Si TFTs, n-type TFTs usually have higher carrier mobility and thus lower operation voltage. To form the VCCS configuration with the n-type transistor, one must "invert" the OLEDs, i.e. making OLEDs that have a cathode at bottom and an anode on top, as shown in Fig. 2.7. The major challenges in inverted OLEDs, like in developing top-emitting OLEDs, are to prepare a bottom cathode providing effective electron injection and to prepare a top anode providing effective hole injection.

Very recently, Chen et al. demonstrated efficient inverted top-emitting OLEDs using an ultrathin Alq₃–LiF–Al trilayer as the electron-injection structure for the
bottom cathode [39]. Such an electron-injection structure does not involve handling reactive metals during fabrication and permits use of highly reflective materials such as Al and Ag as the bottom cathode. In 2005, Murakami et al. reported inverted top-emitting OLEDs employing an e-beam-evaporated V_2O_5 layer as a buffer-hole-injection layer for the sputtered IZO (indium zinc oxide) top anode [40]. Such inverted top-emitting OLEDs exhibited identical current-voltage characteristics, comparable operational stability and efficiency in comparison with the conventional bottom-emitting device. In the same year, a 3.25-in full-color AMOLED display incorporating inverted top-emitting OLEDs and the poly-Si backplane was also demonstrated [41]. The inverted top-emitting OLED adopted the p-i-n structure with Cr as the reflective bottom electrode and semitransparent metal-dielectric capping as the top anode.

C. High Contrast OLEDs

Generally, OLEDs are composed of a reflective back electrode, organic layers, and a (semi-)transparent exit electrode for light out-coupling. With the reflective back electrode, OLEDs exhibit rather strong reflection. Such reflection would seriously degrade the contrast of an OLED display under a strong lighting environment.

Through inserting extra layer(s) of optical purposes (absorption, interference or both) into the active region of devices, several device structures have been developed for bottom-emitting OLEDs to reduce reflection for improving contrast. Recently, Yang et al. reported a high-contrast top-emitting OLED [42]. The device utilizes only optical characteristics of electrodes and antireflection (AR) coatings deposited outside the active region of the device, thus reducing impacts on electrical characteristics and device complexity.

Yang’s low-reflection top-emitting device achieved a cd/A efficiency over 60% of that of the bottom-emitting device. The high-contrast top-emitting OLEDs are readily compatible with the processing of active-matrix backplanes and had been implemented into a 3.8-in QVGA (i.e. 240×320) AMOLED with top-gate low-
temperature poly-Si TFTs.

Additionally, incorporation of microcavity structures in any type of OLEDs could be used to enhance colour purity, brightness, and efficiency of OLED displays. Thus, microcavity OLEDs are also becoming attractive for high-performance AMOLEDs. The critical technical issues and the status of development associated with the device technologies are reviewed in [35].

### 2.4 Carbon Nanotube based Field-Emission Displays

Field-emission displays (FEDs) are characterized by superior display performances such as fast response time, wide viewing angles, wide operation temperatures, cathode ray tube (CRT) like colours, ultra-slim features, low cost, and low-power consumption. Compared to OLED, FEDs have much higher brightness, longer lifetime and also the capability of operating in harsh environments. In the FED, most of the performance parameters are determined by the electron emitting material and cathode structure. Various materials such as silicon, molybdenum and carbon related material, etc. were studied for the electron emitters [43]. Carbon nanotubes (CNTs) have inherent advantages as a field emitter material due to their excellent field emission characteristics, strong chemical stability, high mechanical strength and capability of being deposited over large area [44].

In this section, the physical and field emission properties of CNTs are reviewed firstly, and then related field emission device structures and fabrication processes of the FE triode devices for display integration are presented.
2.4.1 Physical Properties of Carbon Nanotubes

In the ideal case, CNTs are a unique form of carbon filament/fibre consisting of either one cylindrical graphene sheet (single-wall nanotube, SWNT) or of several nested cylinders with an interlayer spacing of 0.34–0.36 nm that is close to the typical spacing of turbostratic graphite (multiwall nanotube, MWNT). The diameter of the SWNTs is usually in the range of 0.4–5 nm while the diameter of the MWNTs is 20–100 nm. There are many possibilities to form a cylinder with a graphene sheet [45], as shown in Fig.2.8. In general, the whole family of nanotubes is classified as zigzag, armchair, and chiral tubes of different diameters. This diversity of possible configurations is indeed found in practice, and no particular type is preferentially formed. In most cases, the layers of MWNTs are chiral and of different helicities. Pristine SWNTs are usually closed at both ends by fullerene-like halfspheres that contain both pentagons and hexagons. As shown in Fig. 2.9, a SWNT has a well-defined spherical tip, whereas the shape of a MWNT cap is more polyhedral than spherical. An open MWNT, as the name implies, doesn't have a cap at the ends of the graphene layers and the internal cavity of the tube is exposed.
Figure 2.8: Schematic representation of the construction of a nanotube by rolling-up an infinite strip of graphite sheet. In (A) the chiral vector $C = na \hat{a} + ma \hat{b}$ connects two lattice points $O$ and $A$ on the graphene sheet. An infinite strip is cut from the sheet through these two points, perpendicular to the chiral vector. The strip is then rolled-up into a seamless cylinder. $T = t m \hat{a} + h a \hat{b}$ is the primitive translation vector of the tube. The nanotube is uniquely specified by the pair of integer numbers $n, m$ or by its radius $R = C \pi / 2 \pi$ and chiral angle $\theta$ which is the angle between $C$ and the nearest zigzag of C-C bonds. All different tubes have angles $\theta$ between zero and 30°. Special tube types are the achiral tubes (tubes with mirror symmetry): armchair tubes $(n, n)$ ($\theta = 30°$) (B(a)) and zigzag tubes $(n, 0)$ ($\theta = 0$) (B(b)). All other tubes are called chiral (B(c)). (Adopted from [45])

Figure 2.9: TEM pictures of the ends of a SWNT, a closed MWNT and an open MWNT (Adopted from [44])
2.4.2 Field Emission Properties of Carbon Nanotubes

Electron field emission is a quantum process, where under a sufficiently high external electric field, electrons near the Fermi level can tunnel through the energy barrier and escape to the vacuum level (Fig. 2.10). Compared to thermionic emission, this is a preferred mechanism for certain applications because no heating is required and the emission current is almost solely controlled by the external field [43].

![Potential-energy diagram illustrating the effect of an external electric field on the energy barrier for electrons at a metal surface. (Adopted from [46])](image)

Since the first report about electron emission from CNTs [47], many works have been conducted on preparing CNT emitters and measuring their emission properties [44, 48]. Although the emission properties reported for CNTs vary, depending on the CNT content and size distribution in the specific samples measured, CNTs in general exhibit excellent emission properties, regardless of their structures, orientation, synthesis techniques, or purification [46]. The emission threshold fields of these CNTs are all significantly lower than the reported values for other field emitters such as the Spindt tips and diamond. The nanotubes generate high current densities. SWNTs generally have a smaller diameter and higher degree of structural perfection than MWNTs and hence a
capability for achieving higher current densities and longer life time \[49\]. The current-voltage characteristics of an individual clean SWNT showed no sign of current limiting for an emission current of 2 μA \[50\]. Upon operating at such high current densities, the emission remains robust with no apparent structural degradation or surface damage occurring to the nanotube emitters.

The extraordinary electron field emission characteristics of CNTs can be attributed to its three properties \[48\]: Firstly, with graphene walls parallel to the filament axis, CNTs (single wall metallic-type or multiwall) exhibit high electrical conductivity at room temperature. Secondly, nanotubes are high in aspect ratio and whisker-like in shape. Utsumi \[51\] evaluated commonly used field emission tip shapes and concluded that the best field emission tip should be whisker-like. Thirdly, CNTs can be very stable emitters, even at high temperatures and as they are covalently bonded they do not suffer from electro-migration. Distinctively different from metal emitters, the resistance of a CNT decreases with temperature which limits Joule heat generation, and in fact its temperature varies sub-linearly with current.

For macroscopic ensembles of CNTs, the emission characteristics are related to the unique structure and chemical bonding of the individual CNTs as well the density and orientation of the CNTs; the interaction of the CNTs with the supporting surface. The close packed arrays of CNTs shows a decreased quality of the emission as the close packing of the tubes screen the applied field effectively, reducing the field enhancement of the high aspect ratio tubes. One of the most challenging issues with macroscopic CNT cathodes is the emission uniformity.

2.4.3 Device Structure and Fabrication Process

FEDs can be operated in either diode or triode mode devices. The diode structure is very simple, and has been employed in many CNT FED prototypes. However, since sufficient current density must be guaranteed at the cathode and the corresponding on-off modulation voltage has to be as low as possible to reduce the
power dissipation and enable the easy addressing with low voltage driver ICs, the diode structure has limited potential for display applications. The triode structure, with a gate electrode much closer to the cathode to extract electrons, has high emission current densities at low voltages, and therefore is preferred for the FEDs which leads to lower driving voltage, high light efficiency, smooth gray scale imaging and the fast response for moving pictures [52].

![Diagram of CNT field emission triode devices](image)

**Figure 2.11:** Different structures of CNT field emission triode devices. (Adopted from [52])

There are four types of structures as shown in Fig. 2.11: gate bridge structure, normal-gate structure, planar-gate structure and under-gate structure. Although the under-gate and planar structures were used in FEDs due to the relative simple process and also exhibited some good characteristics, the larger modulation voltage swing, the worse capability of controlling the electron beams convergence on the anode plate and the worse integrability make them less competitive [53].
The structure of a normal-gate CNT field emission triode being integrated with the transistor circuits for active-matrix displays is illustrated in Fig. 2.12. When fabricating the devices, in order to keep the excellent characteristics of field emission, it is desirable that the process of attaching or growing CNTs onto the cathode electrode is taken as a last step to keep the CNTs intact. A typical self-aligned fabrication process is illustrated in Fig. 2.7 [54]. The vertically aligned CNTs were grown on patterned catalyst layers using plasma enhanced chemical vapour deposition (PECVD). PECVD is a high yield and controllable method of producing vertically aligned CNTs with relative low temperature for display applications. To be compatible with the substrate temperature restrictions and the underlayer silicon IC process, CNTs must be synthesized at relatively low substrate temperatures. A technique that was developed for this purpose in our group is to use a combination of a titanium barrier layer and low hydrocarbon concentrations, with plasma-assisted heating [55]. The use of titanium as a thermal barrier will allow the possibility of maintaining the substrate temperature close to room temperature, while allowing the growth of high quality CNTs. Numerical simulation results demonstrate the realistic possibility of using standard 5V CMOS circuitry to drive the normal-gate triode FEDs, which has high contrast, as long as
a lithography resolution of 2µm over a large area becomes mainstream [56]. This structure seems to be the most promising for an application of CNTs to FED emitters in terms of operation voltages as well as FED device performance.

**Figure 2.13:** Self-aligned fabrication process for CNT field emission triode devices. The process began with the deposition of a sandwich structure on the substrate comprising doped poly-Si (gate) on SiO$_2$ (insulator) on a base metal electrode. An array of 150×150 holes of 1 µm diameter at a pitch of 4 µm was then patterned using optical lithography (a). A reactive ion etch (RIE) step using SF$_6$ gas was then used to isotropically etch the poly-Si gate (b). Wet chemical etching in buffered hydrofluoric acid was used to isotropically etch the silicon dioxide insulator, in order to form an array of microcavities (c). Both the gate and insulator were deliberately over etched to produce an undercut. A 20nm TiN layer was then deposited by sputtering, which was followed by the evaporation of 3 nm of nickel (the catalyst for CNT growth) (d). The role of the TiN layer is to prevent nickel diffusion into the back metal electrode during the CNT growth. The unwanted TiN and nickel over the gate were then removed by dissolving the photoresist in acetone (lift-off process, e). (Adopted from [54])
2.5 Active-Matrix Pixel Circuits

The simplest way to address a matrix array of OLEDs or FEDs is by passive matrix (PM) addressing. Although it provides for low-cost displays due to its simple fabrication and integration, the problem with this method is that in order to achieve a given luminance averaged over a frame period $T_f$, a higher driven current within a shorter horizontal scanning time is required. The required higher current level increases with increasing scan rows, and can adversely affect the long term reliability of the display. Moreover, the high currents and high scanning voltages cause much power to be dissipated in the row and column lines of the displays. As this power is not used to produce light, the display efficiency falls rapidly. The lack of luminance uniformity and signal crosstalk are another two severe problems in PM addressed displays. Therefore, the PM addressing scheme is not suitable for the high information-content OLEDs and FEDs with significantly large number of scan rows.

Active matrix (AM) addressing can solve these problems in PM through integrating transistors or circuits into each pixel. The pixel circuitry performs two functions as both a controlled current source and a memory to enable the pixel to continue providing current after the addressing period. Unlike the optical state of a liquid-crystal pixel that can be actively addressed and voltage driven using a single “address” transistor [57], the current-controlled emission of an OLED or an electron field emitter pixel requires at least two transistors to maintain a continuous excitation [58].

In the literature, several pixel circuit configurations have been reported for driving OLEDs [58-61], and also FEDs [62-64], based on the voltage-mode or current-mode approach. The four basic configurations are shown in Fig. 2.14. In the two-TFT configuration [Fig. 2.14 (a)] a voltage is imposed to the gate of a driving transistor during selection and this voltage is stored on a capacitance. Although this configuration has a built-in memory and therefore does not require high peak luminance, this configuration suffers from TFT threshold voltage and
mobility dispersion as well, leading to severe brightness non-uniformity. To suppress the effect of the TFT threshold voltage dispersion, the four-TFT voltage-mode pixel circuit [Fig. 2.14 (b)] is proposed, which uses an auto zero cycle to reference the data against the TFT threshold voltage. However, the main problem of this circuit is that this auto zero cycle is slow when a large number of gray levels are requested, and it can not eliminate the mobility dispersion induced brightness non-uniformity.

The four-TFT switched-current (SI) pixel circuit in Fig. 2.14 (c) is the other approach, whereby the video signal is converted to a current signal, then sampled into the current source transistor during selection, and during other time of a frame period the current source transistor reproduces and holds the current signal to drive the OLED or electron field emitters. So OLEDs and CNT emitters driven with this circuit can provide the best emission current uniformity, but it has a serious charging/discharging problem at low gray levels when the input data current is very low. The long-time and signal-dependent charging/discharging can be improved to meet the video bandwidth requirements by using current-scaling [65-67], current-feedback [68], or hybrid driving approaches [69].
Figure 2.14: Different configurations for pixel addressing circuits. (a) Voltage-mode two transistor configuration. (b) Voltage-mode four transistor configuration. (c) Current-mode four transistor configuration.
2.6 Thermal Effects in SoP Integration

In SoP integration, due to the insulating substrate with poor thermal conductivity, the generated heat at devices and interconnects during system operation can not be efficiently dissipated. The resulting high operation temperature may lead to severe degradation of the device and interconnect reliability, and circuit and system performance. Such serious self-heating problems set one of the biggest challenges for progress of SoP integration. This section reviews the temperature dependence of the silicon material properties and device electrical characteristics, and also how the device and interconnect reliability is affected by temperature rise. The power dissipation and speed as a function of temperature is also briefly discussed.

2.6.1 Temperature Effects on Silicon Material and Devices

Temperature has a strong influence on the properties of semiconductor materials, and thus device performance [70]. In Table 2.3, the influence of temperature on important parameters for silicon material and devices is summarized. Intrinsic carrier density, and generation lifetimes vary exponentially with growing temperature. A weaker increase with temperature can be observed for carrier diffusion length. The recombination lifetime decreases with the increase of temperature.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Temperature Dependence</th>
</tr>
</thead>
<tbody>
<tr>
<td>Intrinsic carrier density, $n_i$</td>
<td>$T^{(3/2)} \exp(-E_a/(2kT))$</td>
</tr>
<tr>
<td>Generation lifetime, $\tau_g$</td>
<td>$n_i \cdot \exp(\Delta E/kT)$</td>
</tr>
<tr>
<td>Recombination lifetime, $\tau_r$</td>
<td>$\sim T^{\frac{1}{2}}$</td>
</tr>
<tr>
<td>Carrier mobility, $\mu_{sp}$</td>
<td>$A \cdot T^{\alpha_0} + B(p) \cdot T^{-2}$</td>
</tr>
<tr>
<td>Diffusion length, $L_{n}, L_{p}$</td>
<td>$\sim T^{\alpha_d - 1}$</td>
</tr>
<tr>
<td>Built-in potential, $V_B$</td>
<td>$kT/q \cdot \ln(N_A N_p/n_i^2)$</td>
</tr>
<tr>
<td>Fermi potential, $E_F - E_i$</td>
<td>$kT \ln(n_i/n_i^0)$</td>
</tr>
</tbody>
</table>

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Figure 2.15: The I-V characteristics of the n-channel and p-channel TFTs with channel length of 4 μm and channel width of 40 μm at different temperature. (a) The output characteristics ($V_{gs}$=8V); (b) The transfer characteristics ($V_{gs}$=8V).
Figure 2.16: The linear temperature dependence of the threshold voltage ($V_{th}$) and velocity saturation parameter ($\alpha_{sat}$).

Figure 2.17: The effective electron mobility ($\mu_{eff}$) as a function of temperature in a low trap density poly-Si TFT.
The temperature dependence of these parameters results in drastic change of the electrical characteristics of silicon devices at high temperature. Fig. 2.15 shows the current-voltage (I-V) characteristics for n-channel and p-channel poly-Si TFTs of 4um channel length at different temperatures, simulated by the RPI Poly-Si TFT model [71]. The temperature rise affects the device characteristics through threshold voltage ($V_T$), the saturation velocity ($v_{sat}$) and effective carrier mobility ($\mu_{eff}$), which depend on the temperature sensitive material parameters in Table 2.3. Fig. 2.16 depicts the linear temperature dependence of $V_T$ and $\alpha_{sat}$, which is similar to that of CMOS bulk and SOI transistors.

For poly-Si TFTs, phonon scattering, surface scattering, crystal-defect and grain-boundary scattering are the major scattering mechanisms governing the characteristics of carrier mobility. Surface scattering and crystal-defect scattering are nearly independent of temperature, while the equivalent mobility values caused by phonon scattering ($\mu_{ph}$) and grain-boundary scattering ($\mu_{gpb}$) have strong but different temperature dependences as [72]:

$$\mu_{ph} \propto T^\alpha \tag{2-1}$$

$$\mu_{gpb} \propto \exp\left(-\frac{E_b}{kT}\right) \tag{2-2}$$

where $\alpha$ is temperature constant (less than zero), $E_b$ signifies the grain-boundary energy barrier, $k$ is Boltzmann’s constant and $T$ is the absolute temperature.

At low temperature, because grain-boundary scattering dominates, the effective mobility increases with rising temperature due to the reduced barrier height at the grain boundaries. When the temperature is high enough, the mobility starts decreasing as the temperature grows, because the barrier height is sufficiently lowered and phonon scattering starts to prevail. These competing temperature dependence result in a non-monotonic variation of the mobility versus temperature as shown in Fig. 2.17.
2.6.2 Temperature Effects on Device and Interconnect Long-Term Reliability

The practical limiting factors for device applications at high temperature are given by failure rates and lifetimes. On the device level, mainly degradation and breakdown of oxides and electromigration (EM) are the main causes for failures.

A. Time-Dependent Dielectric Breakdown (TDDB)

The fundamental physical mechanisms of gate oxide breakdown are divided into two groups: intrinsic and extrinsic oxide breakdown mechanisms. The intrinsic oxide breakdown refers to defect-free oxide. The failure mechanism can be defined at the critical density of accumulated charge traps in the gate oxide through which a conductive path is formed from one interface to the other. The extrinsic breakdown refers to defects in the oxide whose failure mechanisms are the result of plasma damage, mechanical stress inside of oxide film, contamination, hot carrier damage, or oxide damage by ion implantation.

The $E$ and $1/E$ models are widely used in intrinsic gate oxide reliability predictions for oxide thickness greater than 5 nm [73, 74]. Both models have a known physical basis. The $E$-model is expressed as:

$$t_{bd} = A \cdot \exp(-\gamma E) \cdot \exp\left(\frac{E_a}{kT_j}\right)$$

(2-3)

where $t_{bd}$ is the time to breakdown, $A$ is a constant for a given technology, $\gamma$ is the field acceleration parameter, $E$ is the oxide field, $E_a$ is the thermal activation energy, $k$ is Boltzmann's constant, and $T_j$ is the junction temperature (K).

On the other hand, the researchers have argued that the breakdown process is a current driven process, thus $t_{bd}$ should be dependent on $1/E$. The $1/E$ model predicts:
\[ t_{bd} = t_0 \cdot \exp\left(\frac{G}{E}\right) \cdot \exp\left(\frac{E_a}{kT_j}\right) \]  

(2-4)

where \( t_0 \) and \( G \) are constants, and other symbols have the same meanings as above. Both models indicate that increasing the operational temperature will exponentially decrease the time for break down.

B. Electromigration (EM)

Interconnect EM is the movement of metal atoms in the direction of electron flow due to momentum transfer from electrons to the metal ions under thermal and voltage stresses. EM is usually modeled by the empirical Black's formula [75], that relates the Mean-Time-To-Failure (MTTF) to the stressing conditions and is given as:

\[ \text{MTTF} = A \cdot J^m \cdot \exp\left(\frac{E_a}{kT_j}\right) \]  

(2-5)

where \( A \) is a process constant dependent on the material and geometry of the metal strip, \( m \) is a current exponential factor, \( T_j \) is the local temperature (K), \( k \) is Boltzmann's constant, \( E_a \) is the activation energy and \( J \) is the current density. The activation energy for Al-Cu metal is in the range of 0.76-0.86 eV and the activation energy for Cu interconnections can vary widely from 0.7-0.9 eV to 1.0 eV.

Equation (2-5) shows the MTTF will also exponentially decrease as the operation temperature is increased.
2.7 Summary

Advances in process and device technology make possible the realization of significant systems, as devices can be made smaller and faster and the on-panel level of integration denser. The rapid progress of the self-emissive display technologies including OLEDs and CNT-FEDs fulfills the growing demands for display products with high performance and low cost. All the technological evolutions make it feasible to achieve multifunctional and compact SoP display products of desirable performance and acceptable price in the near future. However, the remaining issues, as stated in the chapter, are: (1) continuously down-scaling the TFT devices for higher speed, higher drivability, and denser integration; (2) design and analysis of active-matrix pixel circuits suitable for self-emissive displays; (3) investigate and manage the thermal effects in SoP. The work in this dissertation will focus on these three aspects.
Chapter 3

Implementation Methods

3.1 Introduction

This thesis is aiming to explore the technological issues in three aspects for SoP integration:

- Device structure and design implication for extreme down-scaling
- Design and analysis of pixel driving circuits for self-emissive displays
- Analysis and manage thermal effects in SoP integration.

The academic research in universities specializes in providing novel ideas and theoretical solutions for aimed problems. However, actual fabrication of advanced devices, complicated circuits and systems to demonstrate the design ideas requires the use of large state-of-the-art laboratory facilities, which is too expensive and time-consuming to setup and operate in university environments. In order to fully investigate the arisen technical issues and verify the proposed design ideas, different-level simulation methods in associate with some key fabrication processes are utilized in this thesis as a low cost and time-effective route.

This chapter, firstly, introduces the Technology Computer Aided Simulation (TCAD) tool – Atlas Silvaco in Section 3.2, which is used in the work to study the performance of extremely-scaled poly-Si TFTs and also electro-thermal effects in TFTs. The industry-standard circuit simulator – HSPICE for simulation and analysis of active-matrix pixel circuits is introduced in Section 3.3. To study the thermal
effects in SoP integration, three-dimensional (3-D) finite-element method (FEM) simulation with COMSOL Multiphysics is described in Section 3.4. A summary regarding this chapter is finally provided.

3.2 Numerical Device Simulation with Atlas Silvaco

The utilisation of Technology Computer Aided Simulation (TCAD) tools in semiconductor has become widespread in industry and academia over the past decade to estimate device performance, optimize device parameters or to perform tolerance analyses. Most importantly, TCAD can be regard as a "virtual fabrication laboratory", where one can truly grasp fundamental concepts of designing and fabricating electronics device, such as field-effect transistors (FETs) only by simulation. The use of TCAD is essential in reducing the number of experiments by providing guidelines, so that only the most promising are experimented.

ATLAS Silvaco Device Simulation Framework enables device technology engineers to simulate electrical, optical and thermal behaviour of semiconductor devices. ATLAS provides a physics-based, modular, and extensible platform to analyze DC, AC, and time domain responses for all semiconductor-based technologies in two and three dimensions [76].
3.2.1 Electrical Simulation of Extremely-Scaled TFTs

In this dissertation, firstly, the two-dimensional (2-D) simulation is adopted to study the digital performance of the extremely-scaled TFTs. For each simulation, ATLAS solves the following five basic semiconductor device equations numerically:

(i). Poisson equation

\[ \varepsilon \nabla^2 \psi = -q \left( p - n + N_D^+ - N_A^- \right) - \rho_s \]  

(ii). Electron and hole continuity equations

\[ \frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot J_n - U_n \]  

\[ \frac{\partial p}{\partial t} = \frac{1}{q} \nabla \cdot J_p - U_p \]  

(iii). Electron and hole current equations

\[ \overline{J}_n = -q \mu_n n \nabla \phi_n \]  

\[ \overline{J}_p = -q \mu_p p \nabla \phi_p \]  

where \( \varepsilon \) is the dielectric permittivity, \( \psi \) is the electrostatic potential, \( n \) and \( p \) are the electrons and holes concentrations, \( N_D^+ \) and \( N_A^- \) are the ionized donor and acceptor impurity concentrations, \( \rho_s \) is the surface charge density which may be present due to the fixed charge in the insulator or charge interface states, \( \overline{J}_n \) and \( \overline{J}_p \) are the vectors accounting for the electron and hole current density, \( U_n \) and \( U_p \) are the electrons and holes net recombination rates, \( \mu_n \) and \( \mu_p \) are the electrons and holes mobilities, and \( \phi_n \) and \( \phi_p \) are the electrons and holes quasi-Fermi potentials.

The numerical algorithms used in ATLAS to solve these basic semiconductor equations are based on the finite element method, which discretises the equations.
on a 2D simulation grid. This discretisation process yields a set of non-linear algebraic equations, where the unknowns represent the potential, $n$ and $p$ at each grid point. The coupled non-linear algebraic equations are solved by a non-linear Newton iteration method. The equations (3-1) to (3-3) are solved over the entire grid until a self consistent potential ($\psi$) and free carrier concentrations ($n$, $p$) are obtained. Once the potential ($\psi$) and free carrier concentrations ($n$, $p$) have been successfully calculated at a given bias, it is then possible to determine the quasi-Fermi levels ($\bar{\phi}$) and terminal currents ($J_n^\prime, J_p^\prime$) as given in equation (3-4) and (3-5).

The results obtained from the device simulations depend critically on the physical models and parameters used. Basically all the physical models and materials' parameters can be modified through the statements in the input files. Some of the physical models are described as follows [76]:

(i) **Impact Ionization Model:** This model generally characterize the acceleration in velocity and generation of more free carriers once sufficient energy is acquired in high electric field. Since in this case, the TFT simulation is mainly for low voltage digital application, this model is not loaded.

(ii) **Gate Current Model:** In a device that features a Metal-Insulator-Semiconductor (MIS) formation, high electric field across the thin insulator may results in possibility of tunnelling of electrons (gate current) from the semiconductor (or metal) Fermi level into the insulator conduction band. This may degrade the device operating characteristics with time. This reliability issue can be accounted in simulation using the Gate Current Model. Since gate current is not main area of research in this thesis, this model thus is not included.
Carrier Generation and Recombination Model: This model describes the attempt of semiconductor material to return to steady-state equilibrium after being perturbed by external causes such as phonon transition in the presence of traps, trap-assisted tunnelling of electrons in high electric field, electrons or holes generation or recombination at interfaces etc. The default models for Shockley-Read-Hall and Auger were used throughout the simulations.

Carrier Mobility Model: This model characterises the speed of the electrons and holes induced by electric field in the semiconductor devices by taking into account of various scattering events. The choice of the mobility models is important especially for an extremely-scaled device simulation as it would significantly affect the current drive and transconductance characteristics with gate voltage. In this thesis, the drift-diffusion (DD) transport model has been used to simulate the electrical behaviour of extremely-scaled TFTs. The DD model is known as the simplest and the most efficient approach to calculate the carrier transport in the channel, however it tends to neglect the effects regarding the non-stationary carrier transport, such as velocity overshoot, which will substantially influence the ON-current ($I_{ON}$) of the transistor. Instead of using the time-consuming Monte Carlo (MC) simulation for accurate $I_{ON}$ prediction, one efficient method to tackle this problem in DD model is to modify the high field mobility parameters $\mu_{sat}$ and $\beta$ as given in equation (3-6), following the Granzner approach [77]. This method has been proved to be able to improve the prediction of $I_{ON}$ in agreement with that from MC simulations. The Lombardi CVT model is used to for all relevant effects (longitude as well as transverse field effects) required for simulating the carrier mobility.
\[ \mu = \frac{\mu_0}{\left[ 1 + \left( \frac{E_0 \mu_0}{v_{sat}} \right)^\beta \right]^{\frac{1}{\beta}}} \]  

(3-6)

where \( E_0, \mu_0, v_{sat} \) and \( \beta \) represents the longitudinal electric field, low field mobility and material-dependent \( \beta \) parameter, specifying how abruptly the velocity goes into saturation.

### 3.2.2 Electro-Thermal Simulation of TFTs

Atlas can also account for lattice heat flow and general thermal environments in the device simulation. It implements Wachutka’s thermodynamically rigorous model of lattice heating \[78\], which accounts for Joule heating, heating, and cooling due to carrier generation and recombination. The dependence of material and transport parameters on the lattice temperature, and supports the specification of general thermal environments using a combination of realistic heat-sink structures, thermal impedances, and specified ambient temperatures can also be specified in the simulation. The tool supplies numerical techniques that provide efficient and robust solution of the complicated systems of equations that result when lattice heating is accounted for.

During the simulation process, the partial differential heat flow equation (3-7) is added to the primary semiconductor equations including Poisson’s equations, carrier continuity equation and transport equations, which are numerically and self-consistently solved by ATLAS, on the 2-D or 3-D domains, by fully-coupled and block iteration methods.

\[ \rho \cdot C_p \cdot \frac{\partial T_l(x,y)}{\partial t} = \nabla (\kappa \cdot \nabla T_l(x,y)) + H \]  

(3-7)

where \( \rho \) is the mass density, \( C_p \) is the specific heat of the material, \( \kappa \) is the thermal conductivity, \( T_l \) is lattice temperature, and \( H \) is the generated heat.
Since, in this case, the devices are studied for analogue applications, energy-balance (EB) transport model, instead of DD model, is used to account for velocity overshoot in device simulation, as shown in equations (3-8) to (3-13). For electrons the EB transport model consists of:

\[
\text{div} \bar{S}_n = \frac{1}{q} \nabla \cdot \bar{E} + W_n - \frac{3k}{2} \frac{\partial}{\partial t} (\lambda_n^* \cdot n \cdot T_n)
\] (3-8)

\[
\bar{J}_n = q \cdot D_n \cdot \nabla n - q \cdot \mu_n \cdot n \cdot \nabla \psi + q \cdot \mu_n \cdot D_n^\varphi \cdot T_n
\] (3-9)

\[
\bar{S}_n = -K_n \cdot \nabla T_n - \left( \frac{k \cdot \delta_n}{q} \right) \bar{J}_n \cdot T_n
\] (3-10)

And for holes:

\[
\text{div} \bar{S}_p = \frac{1}{q} \nabla \cdot \bar{E} - W_p - \frac{3k}{2} \frac{\partial}{\partial t} (\lambda_p^* \cdot p \cdot T_p)
\] (3-11)

\[
\bar{J}_p = q \cdot D_p \cdot \nabla p - q \cdot \mu_p \cdot p \cdot \nabla \psi + q \cdot \mu_p \cdot D_p^\varphi \cdot T_p
\] (3-12)

\[
\bar{S}_p = -K_p \cdot \nabla T_p - \left( \frac{k \cdot \delta_p}{q} \right) \bar{J}_p \cdot T_p
\] (3-13)

where \(\bar{S}_n\) and \(\bar{S}_p\) are the energy flux densities associated with electrons and holes, 
and \(\mu_n\) and \(\mu_p\) are the electron and hole mobilities. The remaining terms, \(D_n\) and \(D_p\), are the thermal diffusivities for electrons and holes. \(W_n\) and \(W_p\) are the energy density loss rates for electrons and holes. \(K_n\) and \(K_p\) are the thermal conductivities of electrons and holes. \(T_n\) and \(T_p\) are the electron and hole temperatures. \(k\) is the Boltzmann constant. \(\delta_n\) and \(\delta_p\), \(\lambda_n^*\) and \(\lambda_p^*\) are material related model parameters.

Temperature-dependent impact ionization model is also included in this case. The self-consistent electro-thermal simulation automatically uses the built-in temperature dependence of all the material physical and thermal parameters, and the physical models that are specified.
3.3 Circuit Simulation with HSPICE

SPICE, as its name implies Simulation Program for Integrated Circuits Emphasis, is a general purpose circuit simulator developed at the University of California, Berkeley in 1973. It is used for nonlinear dc, nonlinear transient, and linear ac analyses. Circuits may contain resistors, capacitors, inductors, mutual inductors, independent voltage and current sources, four types of dependent sources, lossless and lossy transmission lines (two separate implementations), switches, uniform distributed RC lines, and the many models of semiconductor devices such as: diodes, BJTs, JFETs, MESFETs, and MOSFETs.

HSPICE is a commercially available extended version of the SPICE circuit simulator from Synopsys, the industry-standard circuit simulator. It offers a high-accuracy circuit simulation environment that combines the most accurate and validated integrated circuit (IC) device models with advanced simulation and analysis algorithms. It supports comprehensive interconnect and signal-integrity analysis solutions, extensive cell-characterization capabilities, and extensive optimization and corner-case analysis capabilities [71].

Hspice lets us perform detailed transistor level simulations. Hspice simulations imitate actual performance of the circuit when fabricated. However, the accuracy of the transistor level simulations depends on how well each device in the circuit is modelled. The device model used in this dissertation to characterise the electrical characteristics of poly-Si TFTs in pixel circuit design is the widely accepted RPI Poly-Si TFT model developed by Rensselaer Polytechnic Institute [79]. The following analysis was used in the study.

- Non-linear DC analysis: calculates the DC transfer curve.
- Non-linear transient analysis: calculates the voltage and current as a function of time when a large signal is applied.
All analyses are done at a default temperature of 300K.

3.4 Three-Dimensional Thermal Simulation with COMSOL Multiphysics

In this dissertation, the self-heating in interconnects and chip-level thermal performance for SoP integration were studied by 3-D finite-element method (FEM) simulation using COMSOL Multiphysics.

COMSOL Multiphysics is a powerful interactive environment for modelling and solving all kinds of scientific and engineering problems based on partial differential equations (PDEs) [80]. With this tool, we can easily extend conventional models for one type of physics into multi-physics models that solve coupled physics phenomena—and do so simultaneously. Thanks to the built-in physics modes it is possible to build models by defining the relevant physical quantities—such as material properties, loads, constraints, sources, and fluxes—rather than by defining the underlying equations. COMSOL Multiphysics then internally compiles a set of PDEs representing the entire model.

When solving the PDEs, COMSOL Multiphysics uses the proven finite element method (FEM). The software runs the finite element analysis together with adaptive meshing and error control using a variety of numerical solvers. A more detailed description of this mathematical and numerical foundation appears in [80].

In the work, the simulation couples the built-in conductive media DC model and the heat transfer model in COMSOL Multiphysics, and solves the electric current and the heat transfer equations simultaneously.
3.5 Summary

It is essential to replace the costly and time-consuming fabrication and characterisation experiments with simulations to deliver shorter development cycles and higher yields in university research. The aim of this chapter is to explain the simulation methods implemented in this dissertation to analyse both electrical and thermal issues at device, circuit and system level in SoP integration. To study the electrical characteristics of extremely-scaled TFTs for digital VLSI applications, 2-D simulation is done by Atlas, vended by Silvaco, with carefully specified physical models. The simulation and analysis of active-matrix pixel circuits is performed with HSPICE, the industry-standard circuit simulator, adopting the widely accepted RPI TFT model. To study the electro-thermal effects on TFT’s analogue performance, the 2-D device simulation by Atlas considers the self-heating effects, and also replaces the DD transport model with the EB model. And finally, to understand the self-heating effects on interconnects and the chip-level thermal effects, 3-D FEM simulations with COMSOL Multiphysics are performed.
Chapter 4

Device Structure and Design
Implications for Extreme-Scaling

4.1 Introduction

Although significant effort has been devoted to the poly-Si crystallization technology to enlarge the grain size [15-17], scaling-down of the channel length may be a more straightforward route to improve the device speed and drivability for achieving higher-performance and low-power ICs based on poly-Si materials [18, 19, 32]. As devices being aggressively scaled, challenges include sustaining the device electrostatic integrity (El) to suppress the parasitic two-dimensional effects including short-channel effects (SCE) and drain-induced barrier lowering (DIBL), controlling leakage currents (Ioff), and maximizing on-off current ratio (Ion/Ioff) [81]. One promising option for continued scaling of the devices while overcoming these challenges without significant departure from standard device structures and process is to use an ultra-thin active channel [82]. With the ultra-thin channel structure, the possibility of using an undoped body may provide immunity to threshold voltage (Vth) variations due to statistical dopant fluctuations, as well as enhanced carrier mobility for higher transistor drive currents. However, ultra-thin poly-Si films pose difficulties in terms of device fabrication and understanding the electronic transport mechanisms. When the poly-Si layer becomes ultra-thin, even the merest thickness variation may result in highly random potential fluctuations due to a strong vertical quantum-confine-ment effect (QCE) [83]. Charge traps at
grain-boundaries (GBs) and the oxide/poly-Si interface will deplete the poly-Si layer of free carriers, resulting in an extremely high resistivity [84]. The high series resistance of the ultra-thin source and drain regions could also limit transistor drive currents.

In this chapter, the device scaling challenges and related device physics are introduced firstly in Section 4.2. In Section 4.3, the fabrication and device structure of nanometre-scale ultra-thin channel poly-Si transistors are presented, and the electrical properties and carrier transport mechanisms in the devices are also discussed. Through numerical device simulations, Section 4.4 gives the design implications for extremely-scaled poly-Si TFTs. Finally, this chapter is summarised.

### 4.2 Device Physics and Scaling Challenges

This section gives the definition of EI, and shows the ultra-thin channel structure is preferred to sustain the EI in short-channel TFTs. The off-state leakage current mechanisms in short-channel poly-Si TFTs and quantum confinement effects in the ultra-thin channel films are also discussed, which is important for the work in Section 4.3 of studying the electrical properties of the ultra-thin channel poly-Si transistors.

#### 4.2.1 Electronics Integrity

The EI of a device reflects its resistance to parasitic two-dimensional (2-D) effects including SCE and DIBL, as illustrated in Fig. 4.1. SCE is defined as the difference in threshold voltage between long-channel and short-channel transistors measured using small Vgs. DIBL is defined as the difference in Vth measured for short-channel transistors using a small and a nominal value for Vgs.
Figure 4.1: The definition of the electrostatic integrity (EI) of a device reflects its resistance to parasitic two-dimensional (2-D) effects including short-channel effects (SCE) and drain-induced barrier lowering (DIBL).

A good EI means a one-dimensional (1-D) potential distribution in a device (as in the long-channel case), whereas poor EI means a 2-D potential distribution that results in the 2-D parasitic effects. A simple relationship between SCE and DIBL on one hand and EI on the other has been established, as follows:

\[
SCE \propto \Phi_{D} \cdot EI \\
DIBL \propto V_{DS} \cdot EI
\]  

(4-1)  
(4-2)

where, \(\Phi_{D}\) is the drain-to-channel junction built-in voltage, \(V_{DS}\) is the drain-to-source bias, and if assuming the device is fully-depleted, EI in a thin channel TFT is given by:

\[
EI = \left(1 + \frac{t_{s}^{2}}{L^{2}} \right) \cdot \frac{T_{nv} \cdot T_{tn}}{L^{2}}
\]

(4-3)

In this expression, \(t_{s}\) denotes the channel thickness, \(L\) denotes the electrical channel...
length (junction-to-junction distance), $T_{ox}$ denotes the effective electrical oxide thickness in inversion. From (4-1), it can be observed that to give a better suppression of the 2-D parasitic effects, thinning the silicon film and gate insulator is required. Since there is a technology limit of depositing very thin gate insulators of high quality for the low temperature TFT process [33], using an ultra-thin channel structure is preferred for extremely-scaled TFTs.

4.2.2 Leakage Current Mechanisms

In poly-Si TFTs, it is demonstrated that anomalous leakage currents arise by electron-hole pair generation via GB traps at drain junction through thermionic emission or thermionic field emission [85]. For the n-channel devices, as illustrated in Fig. 4.2, the generated electrons are readily collected at the drain electrode while holes flow through the channel in the opposite direction by the drain field. When the holes reach the source region they experience a repulsive built-in potential. The holes accumulate and reduce the barrier. The source contact injects the electrons and recombination of electrons and holes takes place, forming the current [86]. Therefore, the leakage current is correlated to 1) the carrier generation rate at the drain junction, which is dependent on GB trap density and electric field at the drain junction; 2) the channel resistance; and 3) the number of carriers which surmount the barrier near the source, which depends on the source barrier. As shown in Fig. 4.3, as the channel length is reduced, the drain potential begins to have a strong effect on the band bending over a significant portion of the device, and the source barrier reduces with an increase in the drain voltage due to the DIBL effects, which may in turn increase the $I_{off}$. With DIBL effects, the weak-inversion subthreshold leakage current also becomes significant. Therefore, in short-channel devices, in different $V_{os}$ regimes, different leakage mechanisms will dominate, as illustrated in Fig. 4.4.
Figure 4.2: The basic structure of an n-channel poly-Si TFT and the band diagram illustrating the junction leakage current mechanisms.

Figure 4.3: Simulated conduction band energy of devices with different channel length for $V_{G}=0$, showing significant DIBL in short-channel devices.
In the case of optimized Si transistors for VLSI design, the $I_{\text{off}}$ in the regime between 'b' and 'c', is more physically important, since in VLSI applications, $V_{GS}$ will usually be biased in this regime to turning off the devices. In the analysis in Section 5, $I_{\text{off}}$ will be defined as the $I_{DS}$ value at the bottom point of the $I_{DS}$-$V_{GS}$ curve ('b' in Fig. 4.4), which is corresponding to the lowest $I_{\text{off}}$ value that the devices can reach after optimization.
Figure 4.4: Illustrations of the off-state leakage mechanisms in different $V_{GS}$ regimes. In short-channel devices, both the junction leakage and the subthreshold leakage current depend on the source-to-channel barrier.
4.2.3 Quantum Confinement Effects in Ultra-thin Channel

In the ultra-thin film channels, there will be a strong QCE in the direction of film thickness [83]. Thus electron motion perpendicular to the layer is quantized, and the change of the ground level conduction band energy due to QCE is given by [83]:

$$\Delta E_{co} = \frac{h^2}{8m^* t_{si}^2}$$

(4-4)

where $m^*$ is the effective mass of the electron, $h$ is the Planck constant, and $t_{si}$ represents the channel thickness.

![Graph](image)

**Figure 4.5**: Dependence on channel thickness of widened band-gap width due to quantum confinement effects in the direction of film thickness.

From equation (4-4), it can be seen that the band-gap is widened due to the QCE. If assuming an electron effective mass of 0.19 $m_e$ and hole effective mass of 0.49 $m_e$, we can expect a 2-nm-thick film to have a 0.69-eV wider bandgap than the bulk material, as shown in Fig. 4.5.
4.3 Nanometer-Scale Ultra-Thin Channel Transistors

4.3.1 Device Structure and Fabrication

The device structure of fabricated ultra-thin channel poly-Si TFTs is shown in Fig. 4.6 (a). The devices were fabricated in Hitachi Central Research Laboratory. Electron-beam lithography was used to fabricate sources and drains of 100-nm-thick phosphorous-doped amorphous silicon on a buried-oxide layer. A thin layer of undoped amorphous silicon (2.0 nm, 2.5 nm and 3.0 nm, respectively) and 10 nm-thick silica were deposited by chemical vapour deposition (CVD). The silica layer is to protect the very thin channel film from etching, oxidation, or other damage. The amorphous film was then crystallized by thermal annealing. The average grain size of the ultra-thin poly-Si channel films is at 10-nm-scale. After patterning the resist by electron beam lithography, the silica was wet-etched. In the oxygen-plasma-ashing process for resist elimination, the exposed thin film of poly-Si was oxidized so that only that part of the thin film which had been covered by silica remained to be the channel. The channel width varies from 70 nm to 0.5 μm with a channel length of 0.5 μm. A 25-nm-thick gate insulator (SiO2: 15 nm + SiN: 5 nm + SiO2: 5nm) and a 100-nm-thick layer of phosphorous-doped poly-Si for the gate electrode were then deposited onto the whole structure. Finally, the gate electrodes and the metal contacts were fabricated. Micrographs of the final structure are given in Fig. 4.6 (b). This structure is almost identical as that of a single-electron-memory the Hitachi group reported previously [87], where natural variation of the channel film thickness is used to form a nanometer-scale current path and storage node. In these devices, however, a flat channel film is deposited by CVD with precise control over the film thickness down to sub-nanometre scale, so that the device simply functions as a MOSFET. The formed thick source/drain (S/D) ultra-thin-channel device structure combines the features of deep S/D contact regions for low parasitic resistance and improved Ef.
Figure 4.6: (a) Schematic description of the device structure. (b) Cross-sectional scanning electron microscopy and transmission electron microscopy micrographs of the fabricated devices.
4.3.2 Basic Electrical Characteristics

The room-temperature output characteristics ($I_{DS}$-$V_{DS}$) for the 0.5 μm length and 0.4 μm width ultra-thin channel poly-Si TFTs of different thickness channels ($t_{Si} = 2.0 \text{ nm}, 2.5 \text{ nm}, \text{ and } 3.0 \text{ nm}$) are shown in Fig. 4.7, which indicate the typical MOSFET behaviour. From the $I_{DS}$-$V_{DS}$ characteristics, it can be seen that the kink effect in such devices is effectively suppressed due to the use of ultra-thin channels. The transfer-characteristics ($I_{DS}$-$V_{GS}$) of the fabricated ultra-thin channel poly-Si TFTs with different thickness channels at different drain bias are shown in Fig. 4.8. The data are obtained through converting the measurements for 500 parallel transistors to a per-transistor result. Extremely small leakage currents and its channel thickness dependence for the devices can be seen in Fig. 4.8. The details of the device
electrical properties and their channel thickness and width dependence are discussed below.

Figure 4.8: Room-temperature $I_{DS}$-$V_{GS}$ characteristics for the devices of different thick channels with channel length 0.5 μm and the channel width 0.4 μm at a drain bias of (a) 1.1 V; and (b) 3.0 V.

4.3.3 Channel Thickness Dependence of $I_{OFF}$ and $I_{ON}/I_{OFF}$

According to Section 4.2.2, the reduction of $I_{OFF}$ may be achieved through reducing the carrier generation rate at the drain junction, increasing the conduction resistance in the channel, or reducing the carrier recombination rate at the source end. The ultra-thin channels eliminate the subsurface leakage and contribute to the high channel resistance, which can be one of the mechanisms for the marked reduction of $I_{OFF}$ in the ultra-thin channel devices. Two other mechanisms to be considered for the ultra-thin channel devices are the reduced carrier recombination rate at the source due to the suppressed DIBL effects and the decreased carrier generation rate at the drain junction due to the widened band-gap.
The ultra-thin channels enhance the electrostatic control of the channel from the gate, and thus effectively suppress DIBL effects. Fig. 4.9 shows the $I_{\text{off}}$ versus normalized drain bias ($V_{ds}/L$) for the ultra-thin channel devices and a thick channel poly-Si TFT. It can be seen that the ultra-thin channel devices present much slower $I_{\text{off}}$ increase rate with the drain bias, and thus much lower $I_{\text{off}}$ value at high drain bias, which are attributed to the suppressed DIBL in the ultra-thin channel devices. Fig. 4.10 shows the simulated DIBL versus $L/t_{\text{ox}}$ for aggressively scaled devices. The DIBL is sufficiently sustained when $L/t_{\text{ox}}$ is larger than 10. This criterion holds for the simulated devices, which have a relatively thick gate-oxide (10 nm). The value may be further reduced by using thinner high-$\kappa$ dielectrics. Therefore, it is possible to design high performance sub-50nm TFTs using the nanometer-scale thin poly-Si films.

Compared to the normal thick channels, the ultra-thin poly-Si channels with nano-size grains contain much higher density trap states, and a higher electric field also presents at the drain junction, as illustrated in Fig. 4.11. However, a lower leakage generation rate at the drain junction may still be expected in the ultra-thin channel devices due to the widened band-gap by the QCE along the direction of film thickness, as discussed in Section IV, since the electron excitation and tunnelling probability from the trap states to conduction band is exponentially dependent on band-gap width.

The reduction of $I_{\text{off}}$ with decreasing the channel thickness is shown in Fig. 4.12. Values are relative to the current at room temperature for a device with an 8-nm-thick channel, since the QCE is almost completely absent in this case. Since this dependence is much stronger than that of the on current when the gate voltage is high enough, there is a higher on-off current ratio ($I_{\text{on}}/I_{\text{off}}$) in thinner channel devices, as shown in the inset in Fig. 4.12. Decreasing the channel film thickness shifts both $I_{\text{on}}$ and $I_{\text{off}}$ and improves the $I_{\text{on}}/I_{\text{off}}$, and thus can meet the special requirements for low-power memory applications [88].
Figure 4.9: The measured leakage current $I_{\text{off}}$ versus normalised drain voltage for devices of different channel thickness.

Figure 4.10: The simulation results of DIBL versus the ratio of the channel length to the channel thickness ($L/t_\text{Si}$). The simulated DIBL across a large number of devices with different channel length and channel thickness. The E1 is sufficiently sustained when $L/t_\text{Si}$ is larger than 10.
Figure 4.11: The simulated electrical field along the channel in the devices of different channel thickness, showing a higher electrical field presenting at the drain junction in the ultra-thin channel devices.

Figure 4.12: Dependence of leakage-current ($I_{OFF}$) reduction on channel thickness. Inset: Dependence of ON/OFF ratio ($I_{ON}/I_{OFF}$) on channel thickness.
4.3.4 Channel Thickness Dependence of Carrier Mobility

![Graph showing the relationship between effective carrier mobility ($\mu_{\text{eff}}$) and channel thickness ($t_{\text{Si}}$). The relationship is $\mu \sim t_{\text{Si}}^6$.]

Figure 4.13: The effective carrier mobility of devices ($\mu_{\text{eff}}$) with different channel thickness. $\mu_{\text{eff}}$ degrades more dramatically with the decrease of $t_{\text{Si}}$ than that in ultra-thin crystalline SOI transistors, which has a $t_{\text{Si}}^6$ dependence.

In poly-Si films, GBs degrade the carrier mobility, through trapping free carriers and creating potential barriers to scatter carriers. With the decrease of $t_{\text{Si}}$, both the GB potential barrier and potential fluctuations increases; and the average grain size also becomes smaller due to a faster quenching rate during annealing. Thus more GBs are introduced into the channel, contributing more traps and scattering centers. Therefore, as shown in Fig. 4.13, the carrier mobility degrades much more dramatically with the decrease of $t_{\text{Si}}$ than that in ultra-thin c-Si SOI transistors, which has a $t_{\text{Si}}^6$ dependence [83]. The relatively lower carrier mobility can be improved by passivating the trapping states at GBs, and enlarging the grain size by advanced crystallisation techniques.
4.3.5 Channel Width Dependence of Electrical Properties

Figure 4.14: $I_{DS}$-$V_{GS}$ characteristics at a drain bias of 0.1 V for different channel width devices, showing the channel width dependence: (a) 2.5 nm thick channel; (b) 3.0 nm thick channel. The displayed current values were normalized for different channel widths, which vary as: 70 nm, 0.1 μm, 0.15 μm, 0.2 μm, 0.3 μm, 0.4 μm and 0.5 μm in the direction indicated by the arrow.

The room-temperature $I_{DS}$-$V_{GS}$ curves for the devices of 2.5 nm and 3.0 nm thick channels with different channel width at a drain bias of 0.1 V are shown in Fig. 4.14, which indicates the different channel width dependence of the electrical properties for the two types of devices. Fig. 4.15 shows the extracted $V_{th}$ values of all the devices. We found large $V_{th}$ shifts and also significant increase of $V_{th}$ dispersion in devices of 2.0 nm and 2.5 nm channel thickness, when the channel width is smaller than 300 nm. While for the devices with 3.0 nm thick channel, the measured $V_{th}$ values have little dependence on the channel width. A clear increase of $V_{th}$ was also observed for c-Si MOSFETs of channel widths narrower than 10 nm, due to the QCE in the channel width direction [89]. However, here, the channel width is much larger than the scale that the QCE may occur. The significantly increased $V_{th}$
and its dispersion for narrower channel devices of 2.0 nm and 2.5 nm thick channels are attributed to other effects.

**Figure 4.15:** Dependence of $V_{th}$ on the channel width for different channel thickness devices. $V_{th}$ was defined as the value of $V_{ds}$ at an $I_{ds}$ of 1 nA/µm with the drain bias of 0.1 V. We have measured 10 devices for every dimension.

**Figure 4.16:** Schematics of potential fluctuations of the lowest sub-band level ($E_{c0}$) induced by quantum-confinement effect (QCE) along the channel thickness direction (Z-direction).
Figure 4.17: Potential profiles (upper figures) and schematic top views (lower figures) in ultra-thin poly-Si channels illustrating the percolation model.

Figure 4.18: For the narrow channel, the resulted percolation conduction path is limited and a path composed of relative low potential sites like that in a wider channel may be stopped at the boundary of the channel ("dead end"). Finally, the electrons have to transport through a path of higher potential sites, thus higher $V_{th}$ was measured for the narrow channel devices.
The average grain size of the ultra-thin poly-Si channel films is at 10-nm-scale. Transport of carriers from one grain to the other requires sufficient energy to overcome or tunnel through the GB potential barrier [22], and will depend on the barrier potential, and also the energy conditions of two neighbouring grains. These parameters are all related to the local physical properties of the film (film thickness, crystalline orientation, grain size, etc.), and drastically vary over the whole film [20], resulting in large spatial potential variations due to the QCE along the channel thickness direction, as shown in Fig. 4.16. This conduction problem could, in principle, be described by the percolation theory that was successfully applied to inhomogeneous conductors [90]. However, an accurate statistical knowledge of the distribution of grain size, crystalline orientation, GB angle and local grain thickness must be known to implement this model, which is almost impossible to obtain for the ultra-thin poly-Si samples. Therefore, we can only estimate the role of percolation qualitatively in the following analysis, but it is enough for understanding the carrier conduction mechanisms in the devices. As illustrated in Fig. 4.17 (a), with the increase of gate voltage, the potentials of grains with lowest energy levels (E►), first, move below the Fermi level (E ►), and localized pockets of electrons will form in these grains; however, no electron transport path is formed in the channel. With the increase of gate voltage, the GB barriers are also decreased by gate induced GB barrier lowering effects [91].

As more and more grains with E► < E ◄ are generated during the increase of gate potential, there is possibly a percolation cluster of such grains that bridge the source and drain, as shown in Fig. 4.17 (b). Driven by the electric force, electrons will select the GBs with lower potential barrier, and transport into neighbouring grains in the percolation cluster, which has the right energy states for the incoming electrons. For the narrow channel, the resulting conduction path is limited and a path composed of relative low potential barriers in a wider channel may be stopped at the boundary of the channel, as illustrated in Fig. 4.18. Finally, the electrons have to transport through a path of higher potential sites. Thus, higher Vth values were measured for the narrow channel devices. Since the conducting
path potential in the narrow area is more sensitive to the local film properties than that in a wider area, the wide channel devices have much more uniform electrical characteristics, and thus a significant increase of \( V_{th} \) dispersion was found in the narrow devices.

The channel thickness dependence of \( V_{th} \) shift with decreasing the channel width is attributed to the influence of ts on the local electrical properties of the poly-Si film. According to equation (4-1), the increase of ts results in the decrease of \( \Delta E_0 \), and also a reduced spatial potential fluctuation. Since the GB material has a relative large effective electron mass [21], the decreased ground level potential at GBs may be larger than that at the grains, which results in the decrease of the GB barrier height. The above mechanisms make the thicker film have relatively lower local site potential and more uniform electrical properties over the whole film. Thus, for the thicker channel devices, the probability of finding a conduction path in the narrow channel covering lower potential sites is almost similar as that in the wide channel devices. As a result, for the 3.0-nm thick channel devices, \( V_{th} \) values show little dependence on the channel width. The different rate of \( V_{th} \) shift from the wide device to the narrow device is also determined by the uniformity of the film properties.
Figure 4.19: The dependence of subthreshold voltage swing and the normalized drain on-current ($I_{on}$) on channel width for: (a) the 2.5 nm and (b) 3.0 nm thick channel devices. $I_{on}$ is extracted as the current at the gate voltage of 3 V in the $I_d-V_{ds}$ curves shown in Fig. 4.8 (b).
With the continuous increase of gate potential, the GB barriers are further lowered, and more grains' conduction band minima, $E_c$ will be push below $E_F$. As a result, more than one conductive path may appear in the channel contributing to the current transport as shown in Fig. 4.17 (c). In thinner channel devices, the number and the required electron transport energy of the possible conductive paths will directly depend on the channel width, since in a wider channel the possibility of finding more conductive paths of lower potential sites is higher, while in the narrow channel the number of conductive paths are limited by the channel boundaries. Therefore, there is also a large degradation of the normalized drain on-current ($I_{on}$) when the channel width is below 0.3 μm, as shown in Fig. 4.19 (a). The large subthreshold voltage swing in narrow channel devices is also because a higher gate bias is needed to enable a path composed of higher potential sites in narrow channel devices to carry more current. For the 3.0 nm thick channel devices, due to the relative low potential sites and uniform electrical properties over the film, the devices show little dependence of the subthreshold voltage swing on channel width, as shown in Fig. 4.19 (b). However, the narrow channel devices obviously have a larger normalized on-current than wide channel devices as shown in Fig. 4.19 (b), which may be attributed to two reasons: firstly, in wider devices, electrons may transport through lower potential sites, but the effective transport length is longer and will be more dominant in the thick channel devices; secondly, the ratio of the effective carrier transport width to the actual device channel width in the narrow devices is larger than that in the wide devices. These special properties of ultra-thin channel devices imply that additional considerations are necessary for the device modelling and circuit design.
4.4 Design Implications for Extremely-Scaled Devices

![Diagram of Excimer Laser Irradiation and Source/Drain Structures](image)

Figure 4.20: (a) The structures for realizing thickness spatial modulation; (b) The micrograph shows the obtained channel film structure with source/drain unilateral grain growth; and (c) The channel model for the simulation.

With the down-scaling of channel length and the increase of grain size, the channel length of the poly-Si TFTs is becoming comparable to or even smaller than the grain size. As a result, the fluctuations of the locations and physical properties of GBs in the channel are likely to induce significant statistical fluctuations in device performance. Recently, several methods with simple processes allow the possibility to form uniform poly-Si layers with a spatially controlled grain structure, by creating abrupt temperature gradients to initiate the lateral grain
growth (LGG) [92-94]. Among these methods, the simple method of thickness spatial modulation (TSM) [94], which requires no additional processing steps, can also naturally produce ultra-thin-body, thick-S/D structure, which is suitable for designing extremely-scaled TFTs. The TSM method induces the LGG through creating lateral temperature gradient between thick S/D and thin channel regions. As illustrated in Fig. 4.20 (a), two possible implementations of the concept are raised S/D (RSD) and buried S/D (BSD) structures. In both structures, a thick layer of a-Si film was defined as the S/D islands on or inside the buried oxide layer, covered by a thin layer of a-Si film to form the channel. When a proper laser energy density irradiates the whole region, the channel region is completely melted while the thick S/D regions are only partially melted, leaving behind islands of solid material. As a result, grain growth will come up from the unmelted S/D islands, and then stretch toward the completely melted thin channel until small grains, which homogeneously grow in the channel region, impede the extending grains. For a certain channel length, a device with a single GB in the channel can be fabricated (Fig. 4.20 (b)). Since the grain growth is less sensitive to laser energy density variation within the broadened process window, the device exhibits more uniform properties. Although, as the film thickness is reduced, the lateral grain size of the thin film crystallized at the optimal laser energy density may become smaller due to a faster quenching rate, it is still possible to use a thinner film to produce the single-GB structure for shorter channel devices.

In this section, through numerical device simulations, the manufacturability of the devices by the TSM method is investigated for sub-100 nm TFT design by projecting the device performance with process induced variations of GB properties, and other device parameters. The study is expected to be able to give some implications for extremely-scaled TFT design.
4.4.1 Simulation Setup

![Graph](image1)

Figure 4.21: Fitting of the simulation results via the proposed channel model to the experiment data of a 2 μm channel poly-Si TFT.

![Diagram](image2)

Figure 4.22: The buried source/drain device structure for the study.

To evaluate the device performance, device simulations were performed using Atlas, vended by SILVACO [76]. As illustrated in Fig.4.20 (c), the channel is seen as being composed of two low-trap-density regions due to the presence of sub-GB's, separated by a narrow high-trap-density region as the single-GB. The donor-like and acceptor-like densities of states for carrier traps are given by the double
exponential expressions [95]:

\[ g_d(E) = g_{\text{DA}} \exp\left(\frac{E_d-E}{E_{\text{TD}d}}\right) + g_{\text{DDA}} \exp\left(\frac{E_d-E}{E_{\text{DDA}}}\right) \] (4-5)

\[ g_a(E) = g_{\text{TA}} \exp\left(\frac{E_a-E}{E_{\text{TD}a}}\right) + g_{\text{DA}} \exp\left(\frac{E_a-E}{E_{\text{DA}}}\right) \] (4-6)

where \(g_{\text{DDA/DA}}\) is the density of the donor/acceptor-like states at \(E=E_d/E_{\text{c}}\). \(E_{\text{DDA/DA}}\) is the deep-gap slope of the donor/acceptor-like states. \(g_{\text{DDA/TA}}\) is the density of the donor/acceptor-like states at \(E=E_d/E_{\text{c}}\). \(E_{\text{TD/DA}}\) is the band-tail slope of the donor/acceptor-like states.

### Table 4.1 Geometrical parameters used in the simulation

<table>
<thead>
<tr>
<th>Geometrical Parameters</th>
<th>Values</th>
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</thead>
<tbody>
<tr>
<td>Metallurgical channel length, (L_{\text{met}})</td>
<td>100 nm</td>
</tr>
<tr>
<td>Gate length, (L_g)</td>
<td>80 nm</td>
</tr>
<tr>
<td>Channel thickness, (t_{\text{si}})</td>
<td>6 nm, 8 nm, 10 nm, 12 nm</td>
</tr>
<tr>
<td>Gate insulator thickness, (t_{\text{ex}})</td>
<td>10 nm</td>
</tr>
</tbody>
</table>

### Table 4.2 GB model parameters used in the simulation

<table>
<thead>
<tr>
<th>Model Parameters</th>
<th>GB region GB trap density</th>
<th>Low trap region GB trap density</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(g_{\text{DD}} (\text{cm}^{-3}\text{eV}^{-1}))</td>
<td>(g_{\text{DD}} (\text{cm}^{-3}\text{eV}^{-1}))</td>
</tr>
<tr>
<td>(g_{\text{DD}} (\text{cm}^{-3}\text{eV}^{-1}))</td>
<td>0.7e20</td>
<td>0.7e19</td>
</tr>
<tr>
<td>(g_{\text{DD}} (\text{cm}^{-3}\text{eV}^{-1}))</td>
<td>1.5e18</td>
<td>1.5e17</td>
</tr>
<tr>
<td>(g_{\text{DD}} (\text{cm}^{-3}\text{eV}^{-1}))</td>
<td>0.4e21</td>
<td>0.4e20</td>
</tr>
<tr>
<td>(g_{\text{DD}} (\text{cm}^{-3}\text{eV}^{-1}))</td>
<td>0.4e19</td>
<td>0.4e18</td>
</tr>
<tr>
<td>(E_{\text{dd}} (\text{meV}))</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>(E_{\text{dd}} (\text{meV}))</td>
<td>191</td>
<td>191</td>
</tr>
<tr>
<td>(E_{\text{dd}} (\text{meV}))</td>
<td>17.5</td>
<td>17.5</td>
</tr>
</tbody>
</table>
Since at the GB the lattice mismatch and the dislocation stress field cause increased scattering and hence result in lower local mobility, the scattering effect is considered by defining the GB region with low carrier mobility [22]. This modeling technique was validated by comparing the simulated results with the experimental data for a single-GB poly-Si TFT device with 2 μm channel length [92], as shown in Fig. 4.21. Since the BSD devices demonstrated better scaling capability than the RSD devices [96], the work here will focus on the BSD structure devices in the sub-100 nm regime. Fig. 4.22 shows the device structure for the simulation, and Table 4.1 and 4.2 lists the relative parameters used for the work. Unless specified, the fitted GB trap density parameters will be the default value for the GB model used in the simulation. Fig. 4.23 gives the extraction of the important device parameters including $I_{ON}$, $I_{OFF}$, and S-Slope from $I_{DS}$-$V_{GS}$ curves. 1.5 V is the power supply. $V_{th}$ is extracted as the gate voltage where $I_{DS}=100nA(W/L)$ at $V_{DS}=0.1V$. DIBL is obtained by the method shown in Fig. 4.1. Intrinsic delay CV/I is calculated with $V=1.5V$, $I=I_{ON}$, and $C$, as the gate capacitance, being extracted from AC device simulation.

![Figure 4.23: Extraction of the important device parameters including $I_{ON}$, $I_{OFF}$, and S-Slope from the $I_{DS}$-$V_{GS}$ characteristics. The power supply $V_{DS}=1.5V$.](image-url)
4.4.2 Grain-Boundary Effects in Extremely-Scaled Devices

![Conduction Band Profile](image)

**Figure 4.24:** Conduction band profile illustrating the drain induced GB barrier lowering effects in short-channel poly-Si TFTs.

![Impact of GB on Vth Roll-off Characteristics](image)

**Figure 4.25:** Impacts of GB on the $V_{th}$ roll-off characteristics.
As devices being scaled down to the sub-100-nm regime, the individual GB in the channel becomes very close to the source and drain junctions, and the GB barrier height is easily modulated by drain potential. Due to the increased drain induced GB barrier lowering (DIGBL) effects in shorter channel devices as shown in Fig. 4.24, the presence of a GB in the centre of the channel makes the $V_{th}$ roll-off in poly-
Si TFTs more sensitive to the scaling of channel length than that in c-Si SOI devices, as shown in Fig. 4.25. For long channel devices, $V_{th}$ shifted linearly depending on the trap density at the GB, but was little sensitive to variations in the GB location [95]. However, for the sub-100-nm devices, the parameters not only depend on the trap density, but are also sensitive to the GB location. In the simulation, considering the effects of TSM on the GB growth, the GB is assumed to vary within 20 nm on the left and right of the center of the channel. As shown in Fig. 4.26, when the GB is located at the right part of the channel, $I_{on}$ and $V_{th}$ become very sensitive to the GB location: $I_{on}$ increases linearly about 18 $\mu$A, while $V_{th}$ decreases linearly about 15 mV, as the GB moving 10 nm closer to the drain junction. This is in agreement with that in Fig. 4.24. When the GB is closer to the drain junction, the DIGBL effects get stronger. Therefore, the electrons can more easily conduct through the GB, resulting in higher $I_{on}$ and lower $V_{th}$. All the results indicate that the presence of GB in sub-100-nm TFTs causes serious challenges for manufacture devices with well controlled intra-chip or inter-chip uniformity.
Figure 4.26: Effects of GB location related to the centre of the channel on the device electrical characteristics with different GB trap density: (a) threshold voltage ($V_{th}$); (b) On-current ($I_{on}$).
4.4.3 Effects of Channel Thickness ($t_{si}$)

![Graph showing effects of channel thickness on device electrical parameters](image)

Figure 4.27: Effects of channel thickness on the device electrical parameters with the fitted GB trap density, and $L_s = 80$ nm.

Reduction of SCEs requires the use of thin channel films to enhance the gate control of the channel, especially for poly-Si TFTs, which have a technical limit on the scaling of gate insulator [33]. However, using an ultra-thin channel makes the device parameters very sensitive to $t_{si}$ variations, as shown in Fig. 4.27. The decrease of $t_{si}$ results lower $I_{ON}$, higher $V_{th}$, but better S-Slope due to better El. The intrinsic delay is increased due to the decreased $I_{ON}$. Since it has been achieved to deposit the a-Si thin film down to 2.0 nm with precise control of thickness by chemical-vapour deposition as shown in Fig. 4.6, the fluctuations induced by $t_{si}$ variations can be controlled well.
4.4.4 Effects of Doping Profile \(d\)

![Doping Profile Diagram](image)

Figure 4.28: The doping profiles used in the simulation

Fig. 4.28 shows the doping profile along the channel for the study. Fig. 4.29 (a-c) shows \(V_{th}\), DIBL and S-Slope as functions of lateral doping gradient \(d\) in different thick channel devices. With the nearly abrupt doping profile, the dopant diffusion into the channel is small, and the electrical parameters show little sensitivity to variations of \(d\). As \(d\) continues increasing, the effective channel length is reduced and the electrical parameters show large degradation due to the short channel effects. Thinner channel devices show less sensitivity to the variations of \(d\), which is because the effect of \(d\) on the effective channel length is better controlled due to the sustained EI in thinner channel devices.
(a) $V_{th}$ vs $d$ (nm/dec) for different $t_{Si}$: 6 nm, 8 nm, 10 nm, 12 nm.

(b) DIBL (mV) vs $d$ (nm/dec) for different $t_{Si}$: 6 nm, 8 nm, 10 nm, 12 nm.
Figure 4.29: Effects of the doping gradient ($d$) on the electrical characteristics of devices with different channel thickness: (a) $V_{th}$; (b) DIBL; (c) S-Slope.

4.4.5 Optimal Design

As shown in Fig. 4.27 and Fig. 4.29, $d$ and $t_{Si}$ can be adjustable parameters for optimal design of the devices, if they can be well controlled in the process. Fig. 4.30 gives the design trade-off between $I_{ON}/I_{OFF}$ and $CV/I$ via adjusting both $t_{Si}$ and $d$. In the TFT structure shown in Fig. 4.22, for a given $L_g$, the metallurgical channel length ($L_{met}$) and gate material can also be the adjustable parameters for the optimal design. All these parameters enable designing the extremely-scaled TFTs to meet the different requirements for low-power, high-performance applications.
Figure 4.30: (a) The $I_{OFF}$ and $I_{ON}/I_{OFF}$ ratio versus $I_{ON}$; and (b) The intrinsic delay versus $I_{ON}/I_{OFF}$ ratio with the increase of doping gradient for different channel thickness, showing the possibility of adjusting channel thickness and doping profile for optimal device design.
4.5 Summary

In this Chapter, the analysis indicates that the ultra-thin channel structure is preferred for designing extremely-scaled TFTs with sustained EI. The poly-Si films with the thickness down to 2.0 nm were successfully achieved for the TFT applications. The fabricated devices show desirable transistor performance, and ultra-low leakage current. The interesting electrical properties and carrier transport mechanisms of the devices were fully investigated by invoking the vertical quantum confinement effects in the active channels, providing important guidelines for future process on device optimization and modelling. Further simulation study of sub-100-nm single GB TFTs show the presence of GBs in extremely-scaled TFTs can seriously degrade the inter- and intra-chip uniformity of device electrical characteristics. The simulation results also indicate that, with an undoped channel, the device can be optimised to meet the different requirements for low-power, high-performance applications by adjusting the channel thickness and doping profile.
Chapter 5

Analysis of Switched-Current Pixel Circuits for Self-Emissive Displays

5.1 Introduction

Unlike LCDs, OLED displays and CNT-FEDs are both self-emissive display technologies, and the luminance of the lighting elements is proportional to its current density. Therefore current-mode pixel driving approaches appear to be a natural solution for high quality OLEDs or FEDs. Compared to the voltage-mode driving method, the current-mode one has advantages, such as improved display spatial uniformity, good environmental immunity, excellent linearity and proven long-term stability [69]. To realize current-mode active-matrix addressing, the switched-current (S-I) type pixel circuits were developed to control and drive the OLED [69], and also the FED elements [63]. And the long-time and signal-dependent settling problems in conventional S-I pixel circuits can be improved to meet the video bandwidth requirements by using current-scaling [65-67], current-feedback [68], or hybrid driving approaches [69].

This chapter is to analyse the operation behaviour and the related non-idealities of the S-I pixel circuits, and thus provide guidelines for optimal design of S-I pixel circuits for high performance OLED displays and CNT-FEDs. The analysis is based on the current-copier circuit configuration, and can be extended to other S-I pixel circuits. In this chapter, a simple and effective macro-modelling approach to integrate the emission devices into the SPICE circuit simulation is introduced.
firstly in Section 5.2. Then in Section 5.3, detailed analysis of the operation and related non-idealities in the S-I pixel circuits is presented. According to the analysis results, a simple method to suppress the operation non-idealities is proposed in Section 5.4. Considering the process variations, Section 5.5 predicts the emission current uniformity of the proposed design using Monte Carlo analysis. Finally, this chapter is summarised.

5.2 SPICE Macro-Modelling of Emission Elements

To integrate a given OLED or field emission (FE) triode device into display systems for desired performance, it is highly preferred to be able to timely and accurately evaluate the device's electrical behaviour in the early circuit and system design stage. Therefore, efficient and accurate SPICE compatible models must be developed for this purpose.

5.2.1 Modelling Challenges

For OLED devices, the electron and hole transport and injection phenomena in organic multilayers are not yet fully understood. The complicated structure and material dependent device physics makes it impractical to derive efficient and accurate SPICE models to be used in circuit simulations. This case is similar for CNT FE triode devices. The electrical characteristics of CNT FE triodes are strongly dependent on the process and device structures, and the field emission mechanisms of CNTs are fairly complicated.
In previous works, the OLED is modelled in first order by a combination of a series resistance and a capacitance in parallel with a SPICE junction diode [97], as shown in Fig. 5.1 (a). For CNT FE triodes, a two-terminal Fowler-Nordheim (F-N) SPICE diode model is used to replace the three-terminal configuration for fitting the dependence of the cathode current on the gate-cathode voltage only, as shown in Fig. 5.1 (b) [63]. These models have no physical background, but are parametric models. And to fit the models with the experimental data for the whole working area of the devices is very difficult and time-consuming. In the case of CNT FE devices, the simplified two-terminal model neglects the impacts from the gate-to-cathode leakage current.

Figure 5.1: (a) A simple SPICE model using junction diode model for OLEDs; (b) A simple SPICE model using Fowler-Nordheim (F-N) diode model to replace the three-terminal configuration for CNT field-emission triode devices.
5.2.2 The Macro-Modelling Approach

![Diagram](image)

(a)

Figure 5.2: The macro-models for (a) OLEDs and (b) CNT field emission triode devices for SPICE circuit simulation. The voltage-controlled current sources are modeled by directly specifying the experimental data points via the piecewise linear (PWL) function in SPICE.

The proposed macro-modelling approach is described in Fig. 5.2 for both OLEDs and CNT FE triodes. Both current versus voltage (I-V) characteristics are modelled by voltage-controlled current sources. The one-dimensional piecewise linear (PWL) function in SPICE is used to describe the current sources through modelling the I-V characteristics for OLEDs and the $L_C-V_C$ and $I_{ac}-V_C$ characteristics for CNT FE devices by directly specifying the experimentally measured data points. The syntax of using the PWL function is shown in the following [71]:

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For OLEDs, the experimental I-V data can be directly used in the modelling. For the CNT FE triodes, during normal electrical characterization, the experimental data of \(I_a-V_{cc}\) and \(I_{gc}-V_{cc}\) characteristics at different anode voltage (\(V_a\)) bias is obtained by varying the gate voltage (\(V_c\)) while fixing the cathode voltage (\(V_c\)). But in a display matrix, the gray-scales of each FE element are modulated by changing \(V_c\) with the fixed \(V_c\) and \(V_a\). Since the \(V_a\) is much larger than the variations of \(V_c\) during the full gray-scale modulation, the experimentally measured \(I_{sc}-V_{sc}\) and \(I_{gc}-V_{gc}\) data can also be directly used into the modelling. In Fig. 5.2, \(C\) represents the parasitic capacitance between the anode and cathode for OLEDs, and \(C_{sc}\) represents the parasitic capacitance between the gate and cathode for FE triode devices. The capacitances are important for transient circuit simulations.

The macro-modelling approach is used to model one type of inverted top-emitting OLEDs with ultrathin Alq3-LiF-Al trilayer [39], and two types of CNT FE triode devices with different structures: one is the device with CNT on silicon post structure, and the other is the device with CNT in open aperture structure and the sidewall oxide spacer to reduce the gate leakage current. Details about the fabrication of the FE devices can be found in [98] and [99], respectively. Fig. 5.3 and Fig. 5.4 show the perfect fitting of the simulation results based on the macro-models to the experimental data of all the devices. Actually, because the
experiment data of a given device is directly input into the model, the model can reproduce the real electrical characteristics of the device with no deviations, and since the modelling method doesn’t need any procedures for physical equations derivation and parameter extraction, it can also perform very efficiently for quickly developing SPICE compatible device models for the newly built devices with novel structure or processes.

Figure 5.3: Fitting of the obtained simulation results via the proposed macro-modeling approach to the experimental results for the inverted top-emitting OLEDs with ultrathin Alq3–LiF–Al trilayer [39].
Figure 5.4: Fitting of the obtained simulation results via the proposed macro-modeling approach to the experimental results for two types of field emission triode devices: (a) The device with carbon nanotube on silicon post structure [98]; (b) The device with carbon nanotube in open aperture structure and the sidewall oxide spacer to reduce the gate leakage current [99].
5.3 Analysis of the Operation of S-I Pixel Circuits

To drive the CNT FE triodes, only the n-type TFT circuits can be used. A n-type TFT based current-copier CNT-FED pixel circuit is shown in Fig. 5.5. For OLED, both n-type and p-type TFT pixel circuits can be suitable, which depends on what type of OLED technology is used, as seen in Fig. 5.6. The n-type TFT circuit in Fig. 5.6 (a) is for inverted structure top-emitting OLEDs, and the p-type TFT circuit Fig. 5.6 (b) is for conventional structure top-emitting OLEDs. Active-matrix OLED displays (AMOLEDs) with adopting top-emitting OLED structures remove limitations in the optical transparency of backplanes and the filling factor of traditional bottom-emitting OLED pixels. The inverted structure OLED technology is also preferred because for a-Si TFTs, which are often used in large-scale AMOLEDs, only n-type transistors are available, while for poly-Si TFTs, n-type TFTs usually have higher carrier mobility, and thus lower operation voltage, lower power can be achieved.
Figure 5.6: The switched-current AMOLED pixel circuits: (a) n-TFT circuit configuration for inverted structure top-emission OLEDs; (b) p-TFT circuit configuration for normal structure top-emission OLEDs.

In the following, the n-type TFT based CNT-FED pixel circuit in Fig. 5.1 (a) will be taken as an example for the analysis. However, the analysis procedure is also applicable for the OLED pixel circuits in Fig. 5.6.
5.3.1 Circuit Simulation Setup

Figure 5.7: (a) The circuit model for the simulation study, and, (b) the waveform of input signals.
In this work, the commercial SPICE circuit simulator HSPICE vended by Synopsys is used for the circuit simulation to investigate the operation of S-I pixel circuits. The TFT characteristics for the simulation are extracted based on the widely accepted RPI Poly-Si TFT model [71]. A simple circuit model and the waveform of related input signals, as illustrated in Fig. 5.7 (a), are used to emulating the pixel circuit's behaviour in the display matrix. In the middle of Fig. 5.7 (a) is the pixel of interest, denoted as P. During a full frame time, before P is selected, M2a is turned ON and draws $I_{data}$ into M1a, emulating the pixels above P of the same column. Similarly, M3b and M3b emulate the pixels below P of the same column.

Since the following study aims to investigate the performance of the pixel circuits, the total cathode emission current of the CNT FE triode devices modulated by the pixel circuits is taken for the analysis instead of the cathode-to-anode emission current.

5.3.2 Sample and Hold Operation of S-I Pixel Circuits

![Figure 5.8: Two operation phases of the n-TFT current-copier pixel circuit for CNT field emission displays: (a) sampling and (b) hold.](image)

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For the current-copier CNT-FED pixel circuit, the operation can be divided into two phases: sampling and hold, as shown in Fig. 5.8. During the sampling phase, the video signal is converted to a current signal $I_{\text{data}}$ and then sampled into the current sink transistor $M_s$ during row selection. During the hold phase, the current sink transistor $M_s$ reproduces and holds the current signal to drive the lighting element.

Theoretically, the modulated cathode emission current $I_c$ is equal to the input data current $I_{\text{data}}$, independent of the process variations of the circuit components. However, there are usually some deviations of $I_c$ from $I_{\text{data}}$ due to several undesired effects which are sensitive to the process variations of circuit components. Thus, the output linearity of the driver circuitry and the emission current uniformity may deteriorate.

### 5.3.3 Sample and Hold Non-Idealities

For the current-copier FED pixel shown in Fig. 5.5, in a realistic case, the finally modulated cathode emission current is given by [100]:

$$I_c = (\sqrt{I_{\text{data}}} - \sqrt{\beta_{M_s} \cdot \Delta V_{gs}^{M_s}})^2 + \lambda \cdot \Delta V_{ds}^{M_s} \quad (5-1)$$

where $\beta_{M_s} = \frac{W}{2} \mu_{FE} \cdot C_a$ is the transconductance factor of $M_s$, $\Delta V_{gs}^{M_s}$ and $\Delta V_{ds}^{M_s}$ are the gate stored voltage and the drain voltage shift which occurs when the pixel operation changes from the sampling phase to the hold phase, and $\lambda$ is a constant associated with the channel length modulation and the kink effects of the poly-Si TFTs.
Figure 5.9: The variation of the Ms's gate-source voltage $V_{gs}^{Ms}$ and drain-source voltage $V_{ds}^{Ms}$ when the pixel circuit in Fig. 5.5 shifts from sampling phase to hold phase: $\Delta V_{gs,M1}^{Ms}$ is the falling part due to charge injection and clock feed-through effects on M1; $\Delta V_{gs,sp}^{Ms}$ is the rising part due to Ms's drain-to-gate coupling, and $\Delta V_{d}^{Ms}$ is Ms's drain-source voltage variation.

Equation (5-1) shows that $\Delta V_{gs}^{Ms}$ and $\Delta V_{d}^{Ms}$ may cause deviation of $I_c$ from $I_{dnh}$. As illustrated in Fig. 5.9, $\Delta V_{gs}^{Ms}$ is composed of two parts: the falling part $\Delta V_{gs,M1}^{Ms}$ due to the charge injection and clock feed-through effects on M1 and the rising part $\Delta V_{gs,sp}^{Ms}$ due to Ms's drain-to-gate coupling. The following discussions will analyze the two parts of $\Delta V_{gs}^{Ms}$ and present the mechanisms that produce $\Delta V_{gs}^{Ms}$, $\Delta V_{d}^{Ms}$ as well as the relations between $I_c$, $\Delta V_{gs}^{Ms}$, $\Delta V_{d}^{Ms}$ and the circuit components.

1) Impacts of M1's switching effects

The main factor that induces the sampled $V_{gs}^{Ms}$ error is the charge injection and clock feedthrough effects of M1. In Fig. 5.1, as row sample signal begins to fall to turn off M1, mobile charges exit through both the drain end and the source end of
The charges transferred to the Cs cause a reduction to the sampled voltage, which can be expressed as [101]:

\[
\Delta V_{ch} = \frac{pWL(C_s + C_{gs})}{C_s + C_{gs}^{M1}} (V_{sam} - V_{T} - \eta V_{gs}^{M1})
\]  

(5-2)

where \( V_{T}^{M1} \) is Mi's threshold voltage, \( p \) denotes the fraction of the channel charge that flows into Cs, depending on the voltage swing and falling rate of \( V_{sam} \). A higher swing or quicker falling rate of \( V_{sam} \) will cause larger \( p \). \( \eta V_{gs}^{M1} \) represents the average channel potential, which is dependent on the input data current.

At the same time, when \( V_{sam} \) switches from high to low, the voltage difference in \( V_{sam} \) switching may be coupled into the sampled point with the clock feedthrough effect, and give rise to \( \Delta V_{cl} \), which is given by [101]:

\[
\Delta V_{cl} = \frac{V_{sam} \cdot C_{gs}^{M1}}{C_{gs}^{M1} + C_{g}}
\]  

(5-3)

For the self-aligned TFT technology, \( C_{gs}^{M1} \approx \frac{1}{2} (W \cdot L)_{M1} \cdot C_{gs}^{M1} \) is much smaller than Cs. Thus, the total amount that the settling voltage \( V_{gs}^{M1} \) is pulled down can be approximated as:

\[
\Delta V_{gs,M1}^{M1} = \Delta V_{ch} + \Delta V_{cl}
\]

\[
= \frac{(W \cdot L)_{M1} \cdot C_{gs}^{M1}}{C_s} [p (V_{sam} - V_{T} - \eta V_{gs}^{M1}) + \frac{1}{2} V_{sam}]
\]  

(5-4)
Figure 5.10: The impacts of $C_s$ with different $I_{data}$: (a) the dependence of $\Delta V_{gs, M1}$ on $C_s$, which is illustrated in Fig. 5.9, on $C_s$; and (b) the dependence of $\sqrt{I_{data}} - \sqrt{I_c}$ on $C_s$. 
Figure 5.11: The impacts of $M_I$'s width $W_{M_I}$ with different $I_{\text{data}}$: (a) the dependence of $M_S$'s gate-source voltage change $\Delta V_{gs,M_I}$, which is illustrated in Fig. 5.9, on $M_I$; (b) the dependence of $\sqrt{I_{\text{data}}} - \sqrt{I_c}$ on $W_{M_I}$.

Fig. 5.3 and Fig. 5.4 show the dependence of $\Delta V_{gs,M_I}^S$, $I_c$ on $C_s$ and the dimensions of $M_I$, respectively. They fit the linear relations of $\Delta V_{gs,M_I}^S \sim 1/C_s$, $\sqrt{I_{\text{data}}} - \sqrt{I_c} \sim 1/C_s$, $\Delta V_{gs,M_I}^S \sim W_{M_S}$, and $\sqrt{I_{\text{data}}} - \sqrt{I_c} \sim W_{M_S}$, derived from
equation (5-1) and (5-4). The decrease of $\Delta V_{\text{str},M1}^M$ with increased $I_{\text{fin}}$ shown in Fig. 5.3 and Fig. 5.4 also agrees with equation (5-4), since a larger $I_{\text{fin}}$ brings a larger $\eta V_{\text{str},M1}^M$, which causes smaller $\Delta V_{\text{str},M1}^M$ according to equation (5-4).

Based on the above arguments, $\Delta V_{\text{str},M1}^M$ can be minimized by using the largest $C_s$ possible, using minimum-geometry $M$, keeping the $V_{\text{sam}}$ swings as small as possible and slowing the falling rate. However, decreasing $M$'s length will cause larger leakage current in the hold phase; increasing $C_s$ and decreasing $M$'s width will prolong the required settling time; lowering the $V_{\text{sam}}$ swing will increase $M$'s ON resistance and thereafter the settling time; finally, the limited pixel selection time makes it difficult to slow $V_{\text{sam}}$'s falling rate too much. That implies some compromises are necessary to be considered in the design to achieve the best performance, and $\Delta V_{\text{str},M1}^M$ is difficult to be completely eliminated.

2) $M$’s drain-to-gate coupling

Another effect that contributes to the sampled $V_{\text{st},r}^M$ error is the drain-to-gate coupling of $M$ through the drain-gate capacitance $C_{gd}$. When the circuit switches from the sampling phase to the hold phase, the increase of $V_{\text{st},r}^M$ may be coupled to the gate with the parasitic drain-gate capacitance $C_{gd}$, and increase the $V_{\text{st},r}^M$ with a certain amount $\Delta V_{\text{str},M1}^M$, which can be expressed as [101]:

$$\Delta V_{\text{str},r}^M = \frac{\Delta V_{\text{str},r}^M \cdot C_{gd}}{C_s + C_{gd}}$$  \hspace{1cm} (5-5)
Figure 5.12: The dependence of $\Delta V_{gs,sp}^{Ms}$, which is illustrated in Fig. 5.2, on $\Delta V_{D}^{Ms}$, with different additional feed-back capacitances $C_f$ between Ms's drain and gate: (a) $C_f = 0.02\, \text{pF}$; (b) $C_f = 0.01\, \text{pF}$; (c) $C_f = 0$. 
Figure 5.13: The current-copier pixel driver circuit for CNT FEDs with adding a feedback capacitance $C_f$ between the drain and gate of $M_s$.

Figure 5.14: The dependence of $\Delta V_{g_s,p}^{M_s}$, which is illustrated in Fig. 5.9, on the additional feed-back capacitance $C_f$ between $M_s$'s drain and gate.

For the self-aligned TFT technology, the $C_{gd}$ is mainly composed of the gate-channel capacitance, which depends on the operation state. With the increased drain voltage, the depletion region near the drain increases and $C_{gd}$ decreases. Thus, $\Delta V_{g_s,p}^{M_s}$ may decrease with increased $V_{d_s}^{M_s}$ in this case, as shown in Fig. 5.12 (c). If adding a larger feedback capacitance $C_f$ between the gate and drain of $M_s$ as shown in Fig. 5.13, then there is $C_{gd} \approx C_f$, and in Fig. 5.12 (a), (b), $\Delta V_{g_s,p}^{M_s}$ has a linear rise
while increasing $V_{D}^{M_{s}}$, which accords with equation (5-5). The linear relation between $\Delta V_{R_{E},C_{p}}^{M_{s}}$ and $C_{p}$ from equation (5-5) also fits the simulation results in Fig. 5.14.

3) The impacts of $M_{s}$'s ON-resistance

When the data current is sampled into the current sink transistor $M_{s}$, the non-zero resistance of $M_{s}$ causes a voltage drop $\Delta V_{M_{s}}^{1}$ on the switch. So there is,

$$V_{G}^{M_{s}} = V_{G}^{M_{s}} - \Delta V_{M_{s}}$$  \hspace{1cm} (5-6)

where

$$\Delta V_{M_{s}} = - \frac{I_{data}}{\mu_{M_{s}} \cdot \left(\frac{W}{L}\right)_{M_{s}} \cdot \left(V_{G}^{M_{s}} - V_{T}^{M_{s}}\right)}$$  \hspace{1cm} (5-7)

and

$$V_{G}^{M_{s}} = V_{samp} - I_{data} \cdot r_{M_{s}}^{M_{s}}$$  \hspace{1cm} (5-8)

$\Delta V_{M_{s}}$ must be kept small enough ($\Delta V_{M_{s}} < V_{T}^{M_{s}}$), otherwise $M_{s}$ will be drawn into the triode operation region and bring a large sampled error of $V_{G}^{M_{s}}$ for reproducing the sampled current during hold phase. In the final design, $\Delta V_{M_{s}}$ can easily be made small enough. But its being sensitive to the process parameter variations of both $M_{s}$ and $M_{t}$ as seen from equation (5-6, 5-7 and 5-8), may give rise to some variations of sampled $V_{G}^{M_{s}}$ and $V_{D}^{M_{s}}$. The larger $\Delta V_{M_{s}}$ will cause smaller $V_{G}^{M_{s}}$, and for a given input data current, the smaller $V_{G}^{M_{s}}$ induces larger $V_{D}^{M_{s}}$ based on equation (5-9). Thereafter, a larger emission current will be reproduced during the hold phase.
\[ I_{\text{dsn}} = g_{m}^{M_{s}} \cdot V_{g}^{M_{s}} + \lambda \cdot V_{D}^{M_{s}} \] \hspace{1cm} (5-9)

Fig. 5.15 shows the linear relation between \( \Delta V_{M_{2}} \) and the L/W of \( M_{2} \), and the increased \( \Delta I_{\alpha} = I_{C} - I_{ss} \) with increasing L/W of \( M_{2} \), which agrees with the above arguments very well. From (5-9), increasing the conductance \( g_{m}^{M_{s}} \) of \( M_{s} \) may cause a decrease of \( V_{g}^{M_{s}} \). But, the increase of the conductance \( g_{m}^{M_{s}} \) will also increase \( \Delta V_{M_{2}} \), reduce \( V_{D}^{M_{s}} \), and finally lower the \( V_{g}^{M_{s}} \). Therefore, an increase of \( \Delta I_{\alpha} \) with increased carrier effective mobility of \( M_{s} \), \( \mu_{s} \) can be found in Fig. 5.16.
Figure 5.15: The dependence of voltage drop on $M_2$: $\Delta V_{M_2}$ and $\Delta I_{err} = I_C - I_{data}$ on $M_2$'s length-to-width ratio $(L/W)_{M_2}$. 

- $I_{data} = 0.5 \mu A$
- $I_{data} = 1 \mu A$
- $I_{data} = 2 \mu A$
Figure 5.16: The dependence $\Delta I_{err} = I_c - I_{data}$ on $M_s$'s effective carrier mobility $\mu_s$ with different input data current $I_{data}$.

5.4 Suppression of Sample and Hold Non-idealities

Figure 5.17: The similar variations of $\Delta V_{GS, M1}$ and $\Delta V_{D, M1}$ with $I_{data}$ for the pixel circuit with an additional feed-back capacitance $C_f$ between $M_s$'s drain and gate.

As discussed above, the main factor that induces the deviation of $I_c$ from $I_{data}$ is charge injection and clock through effects of $M_i$, and is possible partially cancelled
by adding a dummy transistor or using a CMOS transmission gate instead of the n-
type TFT switch [101]. But they both increase the pixel complexity with an
additional TFT and input pulse signal. From Fig. 5.9, it is seen that the \( \Delta V_{\text{gs,op}}^{\text{Ms}} \) may
counteract \( \Delta V_{\text{gs,op}}^{\text{Ms}} \). In fact, as illustrated in equation (5-5), Fig. 5.6, and Fig. 5.7,
since the curve of \( \Delta V_{\text{gs,op}}^{\text{Ms}} \sim I_{\text{data}} \) has a similar change with that of \( \Delta V_{\text{gs,M1}}^{\text{Ms}} \sim I_{\text{data}} \),
choosing a suitable \( C_f \) may produce a \( \Delta V_{\text{gs,op}}^{\text{Ms}} \) that can effectively reduce \( \Delta V_{\text{gs,M1}}^{\text{Ms}} \)
over the whole current range. Fig. 5.18 shows the improved linearity of the pixel
circuit with adding a feedback capacitance \( C_f \) between \( M_s \)’s gate and drain.

The above analysis and simulation results show that the compensation
method is effective for the n-TFT type pixel circuit in Fig. 5.5 for CNT FEDs, and
that in Fig. 5.6(a) for OLEDs. Attributed to the similar operation mechanisms, the
method can also be used to the p-TFT type pixel circuits in Fig. 5.6 (b). Fig. 5.19
shows the circuit configurations with the adding of the compensation capacitance
\( C_f \) in both the n-type TFT and p-type TFT pixel circuits for OLEDs. As shown in Fig.
5.20, in the p-type TFT pixel circuit, \( \Delta V_{\text{gs,op}}^{\text{Ms}} \) and \( \Delta V_{\text{gs,M1}}^{\text{Ms}} \) both have opposite changing
directions compared to the case in n-type TFT pixel circuits as shown in Fig. 5.9,
therefore \( \Delta V_{\text{gs,op}}^{\text{Ms}} \) may still counteract \( \Delta V_{\text{gs,M1}}^{\text{Ms}} \), with a suitable \( C_f \) between the drain
and gate of \( M_s \), as shown in Fig. 5.19 (b).
Figure 5.18: Improved output linearity of the current-copier circuit with a feedback capacitance, $C_f$, between the gate and drain of Ms.

Figure 5.19: The circuit configurations showing the adding of the compensation capacitance $C_i$ in the pixel circuits in Fig. 5.6: (a) for the n-type TFT pixel circuit; and (b) for the p-type TFT pixel circuit.
Figure 5.20: The variation of the $M_s$'s gate-source voltage $V_{gs}^{M_s}$ and drain-source voltage $V_{ds}^{M_s}$ when the p-TFT pixel circuit in Fig.5.6 (b) shifts from sampling phase to hold phase.

5.5 Current Non-uniformity due to Process Variations

| Table 5.1 Gauss distribution of the process parameters for SPICE Monte Carlo analysis |
|------------------------------------------|-----------------|-----------------|-
| Parameters                              | Normal value    | Related variation | σ  |
| $V_t(M_5,M_3,M_2)$                      | 1.5 V           | 20%              | 3  |
| $V_t(M_3)$†                            | 3.1 V           | 20%              | 3  |
| $\mu(M_3,M_3,M_3)$                     | 130 cm²/V-s     | 20%              | 3  |
| $\mu(M_3)$                             | 100 cm²/V-s     | 20%              | 3  |
| kink effect factor $M_5,M_3,M_2$       | 19.3            | 15%              | 3  |
| kink effect factor $M_3$               | 20.8            | 15%              | 3  |
| $W$, $L$ ($M_5$)                       | 10 μm           | 10%              | 3  |
| $W$ ($M_3$,$M_2$)                      | 20 μm           | 10%              | 3  |
| $L$ ($M_3$,$M_2$)                      | 5 μm            | 10%              | 3  |
| $W$ ($M_3$)                            | 15 μm           | 10%              | 3  |
| $L$ ($M_3$)                            | 30 μm           | 10%              | 3  |
| $C_s$                                  | 0.4 pF          | 10%              | 3  |
| $C_f$                                  | 0.01 pF         | 10%              | 3  |

* $M_3$ is high-voltage TFT with offset drain structure.
To predict the emission current non-uniformity of the pixel circuits fabricated in a true poly-Si TFT foundry process, Monte Carlo analysis was performed with the Gaussian statistical distribution of all related process parameters in the circuit as shown in Table 5.1. The non-uniform current-voltage characteristics and the standard deviation current errors of the CNT FE triode device model used for the simulation are shown in Fig. 5.11.

![Graph](image)

**Figure 5.21:** (a) The current-voltage characteristics of the triode field emitter model for statistical simulation; (b) the standard deviation error of the field emission current with different gate voltages of the triode field emitter model.

The distribution histogram of $I_c$ obtained by Monte Carlo analysis in Fig. 5.22 shows the circuit with a feedback capacitance $C_f$ provides better current-copy accuracy, but it has a little worse uniformity due to the additional parameter $C_f$, which is also shown in Fig. 5.23. Although compared with the original current-voltage characteristics shown in Fig. 5.21, the standard deviation error for the cathode emission current has been greatly reduced and therefore a much higher
uniformity obtained, the increasing standard deviation of $I_c$ with the increased $I_{data}$ signifies the importance for improving the process for building high-resolution and high-brightness current-mode active matrix addressed displays. Fortunately, because the human eye is not sensitive to a smooth luminance variation in the long-range regime (a range of viewing angles from about $30^\circ$ to $60^\circ$) [102] and the TFT technology in a short-range regime can show good uniformity of the electrical characteristics, it is very promising to design the current-mode pixel circuit for produce FEDs or OLEDs with good enough luminance uniformity.

![Figure 5.22: $I_c$ distribution with different input $I_{data}$ obtained by Monte Carlo statistical analysis with the Gaussian distribution of process parameters shown in Table 5.1.](image-url)
Figure 5.23: The standard deviation of $I_c$ obtained from the Monte Carlo analysis results.

5.6 Summary

The switched current (SI) pixel circuits are shown to be the most suitable candidate for driving the pixel lighting elements in active-matrix self-emissive displays including OLEDs and CNT-FEDs. The non-idealities that contribute to the current non-uniformity in the SI pixel circuit are carefully investigated based on the current-copier circuit configuration, including: 1) the charge injection and clock feedthrough effects; 2) drain-to-gate coupling of the current sink TFT; 3) the ON-resistance of the switch TFT. Detailed analysis of the modulated emission current varying with the circuit component parameters is very important for designing and optimizing the pixel circuit for high performance displays. It is also found that through a simple capacitive compensation method, the output linearity of the circuit can be improved at some compromise of emission current uniformity. Monte Carlo analysis shows the non-uniformity of the pixel circuit, and proves the importance of greatly improving the process to develop high-resolution and high-
brightness active matrix addressed displays. A simple macro-modelling approach to integrate the emission devices into the SPICE circuit simulation is also proposed in this chapter, which can also perform very efficiently for quickly developing SPICE compatible device models for the newly built emission devices with novel structure or processes.
Chapter 6

Analysis and Management of Electro-Thermal Effects in SoP Integration

6.1 Introduction

As shown in Fig. 6.1, in conventional CMOS and SOI technology based IC chips, a majority of the heat generated in the junction conducts through the silicon substrate, then package and heat-sink. However, for SoP integration on a glass or plastic substrate, the substrate with extremely-low thermal conductivity (1.35 W/mK in glass compare to 148 W/mK in silicon) eliminates the thermal paths. Heat generated in the devices and circuits during operation cannot be efficiently dissipated via the interlayer oxide and glass substrate which have poor thermal
conductivity.

With the increase of IC power densities and performance requirements for full-functional SoPs, the self-heating effect will become more and more pronounced in not only analogue IC modules but also digital VLSIs. The induced electro-thermal issues will become the most critical challenges for realising SoP integration. When determining the process, device, circuit and system design, it is thus very critical to consider the impacts of the electro-thermal effects on performance and reliability.

In this chapter, the electro-thermal effects on the analogue performance of TFTs are firstly investigated in Section 6.2. Section 6.3 studies the self-heating effects in a multi-level interconnect structure. The chip-level thermal performance is considered in Section 6.4. The final section summarises the whole chapter.

### 6.2 Electro-Thermal Effects in Analogue TFTs

When a TFT operates as an analogue device in the SoP integration, it is often biased at a high current level in the device saturation region constantly and power dissipation is thus usually very large, resulting in a high average device operating temperature. The frequency-dependent thermal behaviour, often referred to as dynamic self-heating effect, causes additional effects on the device electro-thermal characteristics [103]. The self-heating seriously degrades the device's performance due to the low thermal conductive buried oxide and substrate, and causes a reduction of drain current observed as a negative differential drain conductance. As the device geometries diminish and transconductance as well as current density increase with device scaling, the electro-thermal effects will become more and more pronounced. To gain a deeper insight into electro-thermal effects in analogue TFTs for SoP integration, the device characteristics of a 0.25 μm gate length TFT on glass substrate is studied by numerical simulation. The same device on an SOI substrate is also simulated for comparison. A possible method to enhance the heat dissipation in TFTs is introduced.
6.2.1 Simulation Setup

![Diagram of device structure](image)

**Figure 6.2**: Two-dimensional device structure used in the simulation with self-heating for the TFT on glass and the SOI transistor.

The following partial differential equation (heat flow equation) is added to the primary semiconductor equations including Poisson's equations, carrier continuity equation and transport equations, which are numerically and self-consistently solved by ATLAS [76], on the two-dimensional (2-D) domains shown in Fig. 6.2.

\[
\rho \cdot C_p \cdot \frac{\partial T_{l}(x,y)}{\partial t} = \nabla (\kappa \cdot \nabla T_{l}(x,y)) + H \tag{6-1}
\]

where \( \rho \) is the mass density, \( C_p \) is the specific heat of the material, \( \kappa \) is the thermal conductivity, \( T_{l} \) is lattice temperature, and \( H \) is the generated heat.

The specified models include lattice temperature calculations, and field dependent mobility model, energy-balance model accounting for velocity overshoot in deep-submicrometer device simulation, bandgap narrowing, SRL and Auger recombination, and temperature-dependent impact ionization model. The simulation automatically uses the built-in temperature dependence of the material parameters and the physical models that are specified.

Since the eventual goal for low-temperature poly-Si technology is to form a c-
Si structure film, the TFT device is assumed to have the same material properties with the c-Si SOI transistor, but using the glass substrate instead of the silicon substrate. The dimensions of the device structure are illustrated in Fig. 6.2. The temperature at the bottom and top of the simulation domain is fixed at the surrounding temperature of 300 K on the assumption of perfect cooling. The left and right boundaries are set as thermal insulation.

6.2.2 Results and Discussion

![Figure 6.3: The simulated $I_{ds}$-$V_ds$ characteristics of the TFT, and the SOI transistor with and without turning on self-heating.](image)

In Fig. 6.3, the simulated $I_{ds}$-$V_ds$ characteristics at various $V_{gs}$ biases of the TFT are compared with that of the SOI transistor with and without turning on self-heating. At the same gate and drain bias, the TFT device has a higher reduction of drain saturation current and stronger negative output conductance effect, compared with that of the SOI transistor. The results indicate a higher device operating temperature in TFTs, and stronger self-heating effects.
Figure 6.4: The simulated temperature contour in (a) the SOI device and (b) the TFT device at $V_{GS}=4.0\, \text{V}$ and $V_{DS}=1.2\, \text{V}$, showing a much higher temperature in the TFT device channel due to self-heating.

Fig. 6.4 shows the temperature contour in the two devices at $V_{GS}=4.0\, \text{V}$ and $V_{DS}=1.2\, \text{V}$. And Fig. 6.5 compares the temperature profile along the channel surface of the TFT and SOI transistor. In the TFT devices, heat generated in the devices during operation cannot be efficiently dissipated via the thick glass substrate which has poor thermal conductivity, and thus the heat generated in the channel is mainly
dissipated through the cap oxide layer and also the source/drain metal. In the case of SOI transistor, the main thermal path is going through the thin buried oxide layer and then the silicon substrate, which have much better thermal conductivity. Therefore, the TFT device structure has a much higher thermal resistance, as shown in Fig. 6.6.

Figure 6.5: Plots of the temperature profile along the channel surface of the TFT and SOI transistor at $V_{gs}=4.0$ V and $V_{ds}=1.2$ V. The middle part from 1.0 $\mu$m to 1.25 $\mu$m is the channel region. The plots showing the source/drain region can help dissipation of the generated heat in the device channel.
Figure 6.6: Average temperature rise in the channels of TFT and SOI transistor as functions of supply power. The thermal resistances $R_{th,TFT}$ and $R_{th,SOI}$ are extracted as the slope of the fitting curves.

Figure 6.7: Simulation data showing small-signal output conductance as a function of drain current for the TFT, and SOI device with and without considering self-heating. Output conductance was simulated at dc bias conditions, corresponding to the strongest dynamic self-heating effect.
Fig. 6.7 plots the output conductance, simulated at static conditions as a function of drain current under $V_{DS} = 1.2$ V for the TFT device, and SOI transistor with and without turning on self-heating. Negative effect due to dynamic self-heating is more pronounced at lower frequencies, therefore the dc output conductance simulation represents the worst-case for dynamic self-heating [103]. Negative output conductance is observed for the TFT device when the drain current reaches 0.45 mA, while in the case of the SOI transistor, it does not occur until the drain current reaches 0.89 mA, clearly indicating a much more significant dynamic self-heating effect in the TFT devices.

The pronounced electro-thermal effects can be a vital consideration for analogue circuit design based on TFT devices in SoP integration. For instance, in the analog circuit design that employs current matching of two transistors, their placement on different positions should be exercised carefully since output current difference due to temperature spatial variations might significantly affect circuit characteristics. The self-heating induced degradation of drain current and AC small signal parameters may also seriously affect other key design specifications of the circuit including gain, bandwidth, etc. [101].

For SOI technology, since the primary thermal path is through the buried oxide layer and silicon substrate, using a thinner or higher thermal conductivity buried oxide layer can enhance the heat dissipation for SOI technology based chips. But for the TFT device, due to the thick substrate of poor thermal conductivity, the generated heat in the device channel has to be mainly dissipated through the cap oxide layer. To improve the thermal performance, the effective thermal conductivity of the oxide layer can be improved through the fabrication of vertical heat pipes. These heat pipes do not necessarily transmit useful information and merely represent additional thermal paths to enhance the heat dissipation.

In the following, two heat pipe placement scenarios for the TFT device structure in Fig. 6.2 are investigated to understand the heat pipe effects on device characteristics. In the first scenario, one 0.15-μm-wide tungsten heat pipe was placed above the drain region and electrically isolated from active Si,
corresponding to about 7% volume density of vertical wiring; in the other scenario, additional 0.15-μm-wide tungsten heat pipe was added above the source region, thus corresponding to about 14% volume density of vertical wiring. The simulated temperature contours for the two resulted device structures are illustrated in Fig. 6.8. It can be seen that the addition of the heat pipe greatly improves the heat dissipation through the cap oxide layer. With 7% heat pipe above the drain region, the peak temperature in the device at \( V_{gs} = 4.0\) V and \( V_{ds} = 1.2\) V, decreases nearly 120 °C compared with that of the TFT device without embedding heat pipe, and with 14% heat pipe, the decreased peak temperature is about 140 °C. The temperature profiles along the device channel surface with different heat pipe placement scenarios are plotted in Fig. 6.9. To see the effects of the heat pipe lateral locations, the temperature profile in the TFT device with a heat pipe embedded above the source region is also shown. The variations of the heat pipe location change the temperature distribution in the channel. Since most heat is generated at the drain junction, when the heat pipe is placed closer to drain junction, it will be easier for the heat to be dissipated, and as a result a lower peak temperature is found in the device with heat pipe above the drain region. Fig. 6.10 gives extracted thermal resistances under the two heat pipe placement scenarios for the 1μm wide TFT device at \( V_{gs} = 4.0\) V and \( V_{ds} = 1.2\) V, which decreases 199.3 °C/mW and 248 °C/mW, respectively.

Increase of the heat pipe density improves the effective thermal conductivity of the cap oxide layer, thus reduces the device channel temperature and the thermal resistance. Attributed to the improved thermal behaviour, the drain current increases as well [Fig. 6.11]. The drain current value, at which negative output conductance occurs, increases. Negative output conductance is observed for the TFT device with 7% heat pipe when drain current reaches 0.62 mA, while in the case of 14 % heat pipe, the drain current for observing negative output conductance is 0.73 mA, as shown in Fig. 6.12, clearly indicating the decreased dynamic self-heating effect.
Figure 6.8: The simulated temperature contour in the TFT device at $V_{gs}=4.0$ V and $V_{ds}=1.2$ V (a) with 0.15 μm embedded tungsten heat pipe above the drain region, and (b) with 0.15 μm embedded tungsten heat pipe above the drain region and the same size heat pipe above the source region.
Figure 6.9: Plots of the temperature profile along the channel surface of the TFT devices with different heat pipe placement scenarios at $V_{DS}=4.0$ V and $V_{DS}=1.2$ V. The middle part from 1.0 $\mu$m to 1.25 $\mu$m is the channel region.

Figure 6.10: Average temperature rise in the channels of TFT with different heat pipe placement scenarios. The thermal resistances are extracted as the slope of the fitting curves.
Figure 6.11: The simulated $I_{DS}$-$V_{DS}$ characteristics of the TFT device with different heat pipe placement scenarios.

Figure 6.12: Simulation data showing small-signal output conductance as a function of drain current for the TFT device with different heat pipe placement scenarios. Output conductance was simulated at dc bias conditions, corresponding to the strongest dynamic self-heating effect.
6.3 Electro-Thermal Effects on Interconnects

Being the major limit for further performance increase of ICs, interconnect wires will become the targets of massive technological improvements for SoP integration. The increasing demand for high-speed and multi-functionality ICs in SoP integration requires aggressively scaling of the interconnect technology to meet the required device density and various circuit performance specifications. The aggressively down-scaling of interconnect will result in increasing current densities and associated thermal effects. Thermal effects may thus become an inseparable aspect of electrical power distribution and signal transmission through interconnects due to self-heating caused by the flow of current, and may seriously impact interconnect design and reliability. Thermal effects impact interconnects design and reliability in two ways [104]. Firstly, they limit the maximum allowable root-mean-square (RMS) current density ($\text{j}_{\text{RMS}}$) in interconnects in order to limit the temperature increase, since the RMS value of the current density is responsible for heat generation. Secondly, interconnect lifetime (reliability) which is limited by electromigration (EM), has an exponential dependence on the inverse metal temperature [74]. Hence, temperature rise of metal interconnects due to self-heating phenomenon can also limit the maximum allowed average current density, since EM capability is dependent on the average current density ($\text{j}_{\text{ave}}$). In SoP integration, the thick substrate of poor thermal conductivity eliminated the heat dissipation through the bottom substrate, and heat dissipation through the cap interlayer dielectric (ILD) layers and metal vias becomes important.

In this section, firstly, the interconnect design rules for the different current densities are introduced, and then the 0.35 µm technology node interconnect structure on glass substrate with self-heating effects is carefully characterized and compared with the structure on SOI substrate by 3-D finite-element method (FEM) simulation using the commercial tool COMSOL Multiphysics [81].
6.3.1 Interconnect Design Rules for Current Densities

High-performance interconnects design is based on the specified limits for the maximum values of three interconnect current densities: average current density ($j_{AVG}$), the root-mean-square (RMS) current density ($j_{RMS}$), and the peak current density ($j_{peak}$) [104]. The peak current density is simply the current density corresponding to the peak current of the signal waveform, and $j_{AVG}$ and $j_{RMS}$ can be related to $j_{peak}$ through:

\[
\begin{align*}
    j_{AVG} &= r \cdot j_{peak} \quad (6-2) \\
    j_{RMS} &= \sqrt{r} \cdot j_{peak} \quad (6-3)
\end{align*}
\]

where $r$ is pulse duty factor defined as $t_{on}/T$, as shown in Fig. 6.13.

For a fixed temperature, EM lifetime of interconnects is known to be determined by $j_{AVG}$, while heat generation is determined by $j_{RMS}$. As a result, keeping the average current density constant at the design rule maximum of 0.2 MA/cm$^2$, Fig. 6.14 depicts the increase of heat generated in a line when the pulse duty factor is reduced. Presently, the main power, ground, and bus lines are designed to operate at the maximum current density allowed. However, as technology moves on, even low level data lines linking individual cells of the circuit may increasingly be manufactured narrow enough to reach this level. In contrast to the main lines, these local data links tend to have a quite small $r$. Due to
their specific function in the circuit, they are usually switched-on less frequently than the main data distributors so that their average load remains pretty low. The RMS load, however, rises according to Fig. 6.14. That means, obeying all present design rules, much more heat will be generated in next generation IC's.

![Graph](image)

**Figure 6.14.** Relationship between average (AVE), root-mean-square (RMS), and peak current density for dc pulses of various duty factors.

### 6.3.2 Simulation Setup

The 3-D electro-thermal FEM simulations are performed by COMSOL Multiphysics [80] to solve the heat flow equation (6-1) coupled with electrical current induced Joule heating in the multi-level interconnects. The decisions of the simulated interconnect structure are discussed in the following.
As the technology being scaled down, the complexity of interconnects increases, including reduction of interconnect metal pitch dimensions and increase of the number of metallisation levels. A typical multi-level interconnect structure with ILD layers is illustrated in Fig.6.15. In general, local interconnects are the first, or lowest, level of interconnects at the device level. Semiglobal interconnects are used to connect devices within a block. And the global interconnects connect long interconnects between the blocks, including power, ground and clocks. Separating interconnects from each other and from the active areas and devices are dielectric materials. Vias connect interconnects through these layers. In SoP integration, the vias can be efficient heat dissipation paths from the active device channel and the lower level interconnects, because they have much higher thermal conductivities than the ILD layers.
Interconnect technologies have a significant impact on chip performance. The IC performance, however, suffers from the non-scalability of the RC interconnect delays because of the increase of the wiring resistance and capacitance. To improve the IC performance at each technology generation, an interconnect scaling scenario is proposed in [105], projecting the need for improved circuit design techniques and new interconnect process technologies. The reasonable interconnect structure data for 0.35μm technology node to be used in the work is based on this scaling scenario, as illustrated in Fig. 6.16. Assuming that all metal lines are uniformly placed with these data and infinitely long, a unit cell can be defined to represent the periodic multilevel interconnect structure for the FEM simulations [Fig. 6.17], where four side walls satisfy symmetric (adiabatic) boundary conditions [106]. The constant temperature of 300 K is applied at both the bottom of the unit cell and at the top of the equivalent, assuming perfect cooling. Aluminium is used for the metal wires and vias, and SiO₂ for the ILD material. To compare the thermal performance of the interconnect structure in SoP integration with that in SOI technology, 500 μm thick glass substrate and silicon substrate is used in the two
technologies, respectively. The silicon active layer is 50 nm thick. And between the substrate and the active layer is 200 nm SiO₂. The dielectric SiO₂ beneath the first metallization level was 0.88 μm thick. The oxide passivation on top of the structure has a total thickness of 3.52 μm. RMS currents are applied to the wires as the input loads in the electro-thermal FEM simulations.

![Figure 6.17: The unit cell geometry representing the periodic multilevel interconnect structure for FEM simulation in the study.](image)

6.3.3 Results and Discussion

A. Comparison of Heating Effects in SOI and SoP Interconnects

In the first attempt, the self-heating effects in the SoP and SOI technology as a result of current loads are comparably studied. The selected range of RMS current density between 0.5 MA/cm² and 2.5 MA/cm² is commonly used in accelerated EM tests. Besides the load application to each metal level of the structure individually, simultaneous loading of the combination of all the metal levels, have been included in the simulation.
Figure 6.18: Temperature rise beyond 300 K in the metal interconnects of (a) M1 and (b) M5, when stressed individually (M1_ON and M5_ON) or simultaneously (all levels). Assuming an average current density of $j_{avg} = 0.2$ MA/cm$^2$, the RMS current densities are reached by pulse signals that have the indicated duty factors. Thus, the decrease in interconnect EM lifetime with respect to the level at the reference temperature (300 K) can directly obtained from the results.
Fig. 6.18 shows the simulated temperature rise in M1 and M5 metal interconnects for SoP and SOI technologies under different current stress conditions. And Fig. 6.19 plots the simulated temperature profile along the vertical direction (Z-direction) in the interconnect structure. In the interconnect structure shown in Fig. 6.17, generally, the generated heat in each metal layer can be dissipated through the bottom substrate (thermal path A) or the top passivation layer (thermal path B) to the ambient.

Metal layers underneath that interconnect, which is stressed by the current, can increase the effective conductivity of thermal path A, and metal layers above the interconnect can help the heat dissipation through thermal path B. However, when the current density in the lower level interconnects and higher level interconnects reaches a significant level as well, the thermal situation exacerbates. For both SoP and SOI technologies, the maximum temperature rise occurs when all lines are loaded simultaneously. The most important results of this set of simulations are the much higher temperature rise in the SoP technology than that.
in the SOI technology, and quite different temperature profiles along the vertical
direction in the interconnect structure for the two technologies [Fig. 6.19].

![Temperature Contour Plots](image)

**Figure 6.20:** The simulated 3D temperature contour plots for the interconnect structure in (a) SOI technology, and, (b) SoP technology, when all metal levels are loaded with the current stress.

In SOI technology, both thermal paths are helpful on the heat dissipation, and thermal path A is more efficient due to the much higher thermal conductivity of silicon than SiO₂. When all metal levels are loaded with the current stress, the heat generated in the interconnects, which are closer to the substrate, is easier to be dissipated through path A, while the heat in the interconnects, which are closer to the cap passivation layer, is easier to be dissipated through path B. As a result, the peak temperature is at the middle metal layer (M4) as shown in Fig. 6.19. In SoP technology, the thermal path A is nearly eliminated due to the thick substrate of poor thermal conductivity, thus the heat is mainly dissipated through thermal path B. When all metal levels are loaded, the heat generated in the interconnects, which are closer to the cap passivation layer, is easier to be dissipated and the peak temperature is at the lowest metal layer (M1) [Fig. 6.19]. The 3-D temperature contours of the interconnect structure for both SOI and SoP technologies are
plotted in Fig. 6.20 for the comparison. The interconnect temperature in SOP is about 60 °C higher than that in SOI. The peak temperature is at M4 for SOI technology and at M1 for SoP technology, which agrees with the previous results. Since the thermal path A in SoP technology is eliminated, the generated heat cannot efficiently dissipated only through thermal path B, resulting in much higher temperature in all metal levels than that in SOI technology, as already shown in Fig. 6.18 and 6.19. The resulted high temperature in SoP interconnects may cause extremely severe degradation of the interconnect lifetime, especially for low duty signal interconnects, as indicated in Fig. 6.18. These effects pose big challenges for designing high performance interconnects in SoP integration.

B. Via and Heat Pipe Effects on the Thermal Performance of SoP Interconnects

In real circuits, the lines of multilevel interconnect systems usually handle a mixture of different pulses. With the same EM design rule, more reasonable duty factors are assumed for different level interconnects as: \( r_{M1} = 0.006, r_{M2} = 0.01, r_{M3} = 0.1, r_{M4} = 0.25 \) and \( r_{M5} = 0.5 \). Based the assumptions, all levels of interconnects are loaded with corresponding RMS current for the following analysis.

As discussed above, in SoP technology, the generated heat is mainly dissipated through the cap passivation dielectric layer. The vias connecting different layers of metal interconnects may play vital roles for the heat dissipation, especially for the lowest level interconnects (M1). As discussed in Section 6.2, to further improve the thermal performance, dummy heat pipes can also be fabricated into the cap passivation layer as additional thermal sub-paths to enhance the heat dissipation. Fig. 6.21 shows the effects of via density and heat pipe density on the temperature rise in interconnects of M1. For the purpose of simplifying the analysis, the inter-layer vias density is assumed same for all levels. It can be seen from the results that the increase of via density can improve the thermal performance, but when the via density reaches about 4%, the effect becomes weak [Fig. 6.21 (a)]. Since the whole thermal path from the M1 level to the ambient is dominated by the thick
passivation layer due to its low thermal conductivity, further improvement of the thermal performance requires the placement of heat pipes in this layer. Fig. 6.21 (a) and (b) show the great reduction of the temperature rise with the heat pipes. And it can also be observed that, after the density of heat pipes reaches a certain value (depending on the interconnect structure, 5% in this case), placement of more heat pipes will have no significant contributions to the improvement of the thermal performance.
Figure 6.21: Temperature rise beyond 300 K in the metal interconnects of M1 in SoP integration of a function of (a) via density, and, (b) heat pipe density.
6.4 Chip-level Electro-Thermal Effects

![Graph showing active power density and sub-threshold leakage power density trends vs. gate length.](image)

**Figure 6.22:** Active power density and sub-threshold leakage power density trends, calculated from industry trends, are plotted vs. gate length (points) for a junction temperature of 25°C. (Adopted from [107])

The primary route to build ICs with increased speed and functionality for SoP integration is through aggressive technology scaling, which is similar to the case for conventional silicon chip ICs. According to traditional CMOS device scaling rule, when device dimensions are scaled downward by a factor $S$, all other parameters are scaled by the same factor, either downward (physical features, supply voltage...) or upward (frequency and capacitance per area...), in order to maintain a fixed power density per unit area. However, as dimensions become smaller, manufacturers must deviate from this, and especially from voltage scaling, because of intrinsic limitations of silicon bandgap and built-in voltages. Since the supply voltage can not decrease as fast as the technology feature size and the clock frequency increases, the power density will grow in fact, as shown in Fig. 6.22. The power consumed by the ICs is converted into heat, resulting in rising heat densities, and junction temperature. The increased IC junction temperature can seriously affect the VLSI design metrics including performance (via decreased transistor
switching speed resulting from decreased charge carrier mobility and increased interconnect latency), power and energy consumption (via increased leakage power), reliability (via thermal cycling, time-dependent dielectric breakdown, etc.), and price (via increased system cooling cost) [108].

In this section, the chip-level thermal performance in SoP integration is analysed and compared with that in CMOS bulk and SOI technologies. The effects of heat pipes on the management of the thermal behaviour are also studied.

6.4.1 Simulation Setup

Figure 6.23: The 3-D structure and related structure data for the FEM simulations. For the simulation in CMOS bulk technology, there is no buried SiO$_2$ layer in the structure.

In this section, the chip-level thermal performance of SoP integration is analysed based on the solutions of the heat flow equations using the 3-D FEM simulation method via COMSOL Multiphysics. The simulated chip-level IC structure is shown in Fig. 6.23. The die length and width are both 2 mm, and the die is composed of 18 circuit blocks. The constant temperature of 300 K is applied at both the bottom and at the top of the structure for perfect cooling, while the four side walls are set as adiabatic boundary conditions.
6.4.2 Results and Discussion

Figure 6.24: (a) Functional block layout of an IC showing power density associated with each block. The average power density is about 60 W/cm². (b) Simulated spatial junction temperature profile of the IC in SoP integration.
Fig. 6.24 (a) gives the power density for each function block in the IC with the average power density of about 60 W/cm², which corresponds with the power density of 0.13 μm technology node (gate length of 80 nm) as shown in Fig. 6.22. Fig. 6.24 (b) plots the spatial junction temperature profile (extracted as the temperature at the surface of the active layer) of the IC in SoP integration. Compared to the simulation results based on the same IC structure, but in CMOS bulk and SOI technologies, as shown in Fig. 6.25, the junction temperature in SoP based ICs is quite high, due to the poor thermal conductive substrate.

To improve the thermal performance, a simple effective way is to increase the vertical wiring in the cap passivation layer, as discussed above. The multi-level interconnect wires and vias above the active layer may help the heat dissipation. However, due to the high current density in these wires and vias for signal and power transmission, their effects on enhancing the heat dissipation will be exacerbated [106]. Therefore, adding dummy heat pipes to increase the vertical wiring density is required. For the 0.13 μm technology, copper is needed for designing high performance interconnects [105]. Assuming the heat pipes can be fabricated using the copper metallization technique, 0.5% copper is uniformly placed into the cap SiO₂ layer of the simulated IC structure, and the junction temperature in the IC is seen to be greatly reduced, as shown in Fig. 6.26 (a). Although the global placement of heat pipes can effectively reduce the junction temperature over the whole chip, the thermal gradients may still remain and cause large performance variations for the system due the temperature sensitive device characteristics, and the global placement of heat pipes is also limited by the wiring of interconnects. Localised heat pipe placement seems more effective and feasible. Fig 6.26 (b) shows the simulated temperature profile of the IC through only placing 0.5% copper heat pipe in the hot spot regions shown in Fig. 6.24 (b), which occupies about 12.5% of the whole chip area. The results indicate that during design stage, the placement of heat pipes can be optimized based on the spatial temperature profile obtained from primary simulations to remove the hot spots for better thermal performance as well as lower cost and higher electrical performance.
Figure 6.25: Simulated spatial junction temperature profile of the IC in (a) CMOS bulk technology; and (b) SOI technology.
Figure 6.26: Simulated spatial junction temperature profile of the IC in SoP integration with placement of heat pipes. (a) Global placement of heat pipes over the whole chip; and (b) localised placement of heat pipes only in the hot spot regions as shown in Fig. 6.24 (b).
6.5 Summary

In this Chapter, electro-thermal effects at analogue devices and interconnects, and the chip-level in SoP integration are investigated and compared with that in SOI and CMOS bulk technologies by different simulation approaches. For analogue applications, the device is often biased at a high current level constantly and power dissipation is thus usually very large, resulting in serious self-heating effects. The self-heating causes high reduction of the drain current, inducing negative output conductance. As the technology being down-scaled to build high-performance, multi-functional ICs for SoP integration, the complexity of interconnects increases, and self-heating effects at interconnects are found to become also very significant. As a result, the EM lifetime of interconnects may be severely degraded. Similarly, due to the increase of IC power densities with the technology scaling, the self-heating effect will become more and more pronounced in not only analogue IC modules but also digital VLSIs. For SoP integration, due to the thick substrate of poor thermal conductivity, the heat can only dissipate through the ILD layer and top passivation dielectric, resulting very high thermal resistance and thus much serious self-heating effects than that in SOI and CMOS bulk technologies. The study shows the metal wiring in the dielectric layers may help the heat dissipation in SoP. To further improve the thermal performance, dummy heat pipes can be fabricated in the dielectric materials as additional heat dissipation paths. The results prove that such a method is very useful not only for decreasing the heating effects in devices and interconnects, but also for remove the hot spots and managing spatial thermal gradients in chip-level design.
Chapter 7

Conclusions and Future Work

7.1 Conclusions

In summary, this dissertation has explored the technological issues in three aspects of SoP integration for next generation display applications:

(i). Device structure and design implications for extremely scaling of poly-Si TFTs

To realise high-level SoP integration, scaling-down of device design rules is required to improve the device speed and drivability for achieving higher-performance, low-power ICs based on poly-Si materials. The ultra-thin channel, thick source/drain structure is shown to be a good choice for design of extremely-scaled poly-Si TFTs with well sustained EI, and also low source/drain parasitic resistance. Ultra-thin poly-Si films pose difficulties in terms of device fabrication, as well as understanding the electronic transport mechanisms. In this work, the nanometre-scale ultra-thin poly-Si films with thickness down to 2.0 nm were successfully achieved in the fabricated TFT devices. The devices are demonstrated with desirable performance and ultra-scaling capability. A qualitative percolation transport model was proposed to investigate the electrical properties and carrier transport mechanisms of the devices by invoking the vertical quantum confinement effects in the active channels, thus providing important guidelines for future processes on device optimization and modelling. Further analysis by numerical device simulation shows the presence of GBs in extremely-scaled TFTs can seriously degrade the inter- and intra-chip...
uniformity of device electrical characteristics, and also the scaling capability. The simulation results also indicate that with an undoped channel the device can be optimised to meet the different requirements for low-power, high-performance applications by adjusting the channel thickness and doping profile.

(ii). Switched-current pixel circuits for self-emissive displays including OLED displays and CNT-FEDs

The switched current (SI) pixel circuits are shown to be the most suitable candidate for driving the pixel lighting elements in active-matrix self-emissive displays including OLEDs and CNT-FEDs, in which the luminance of the lighting elements is proportional to its current density. The sample and hold operation induced non-idealities in this type of pixel circuits, that contribute to the current non-uniformity in the SI pixel circuit, are carefully investigated based on the current-copier circuit configuration. A simple capacitive compensation method was proposed to suppress these effects, and with this method, the output linearity of the circuit can be improved at some compromise of the emission current uniformity. Monte Carlo analysis proves benefits of the process to develop high-resolution and high-brightness active matrix addressed displays. In the simulation analysis, a simple macro-modelling approach to integrate the emission devices into the SPICE circuit simulation is also proposed, which can perform very efficiently for quickly developing SPICE compatible device models for the newly built emission devices with novel structures.

(iii). Electro-thermal effects in devices, interconnects and chip-level thermal effects in SoP integration

In SoP integration, heat generated in the devices and circuits during operation cannot be efficiently dissipated via the thick glass substrate which has poor thermal conductivity. The analysis results show the electro-thermal effects in the analogue TFTs, multi-layer interconnects, and chip-level thermal effects in SoP integration can thus be much more significant than that in conventional bulk CMOS and SOI technologies. This study shows the metal wiring in the dielectric layers may help the
heat dissipation in SoP. To further improve the thermal performance, dummy heat pipes can be fabricated in the dielectric materials as additional heat dissipation paths. The results prove that such a method is very useful not only for decreasing the heating effects in devices and interconnects, but also for removing the hot spots and managing spatial thermal gradients in chip-level design.

7.2 Future Work

To achieve high-level SoP integration, all front- and back-end technologies and design methodologies are required to be developed for building silicon-on-glass (or even silicon-on-plastics) ICs, integrated with high quality display technologies. With the knowledge developed in this dissertation, the following three aspects could be investigated in future work:

(i). Roadmap for SoP integration

The International Technology Roadmap for Semiconductors (ITRS) has pushed the rapid progress of CMOS technology in the last decade, and now it is becoming more and more difficult for further down-scaling of the technology. However, for the SoP technology, such progress has just started. Therefore, a similar technology roadmap on process integration, device structure, interconnect and system design requirements, is also needed for pushing the development of SoP integration. This may be important not only for designing high-performance display products, but also for building other systems including sensors, solar cells, and even a hybrid multi-functional system built on low cost substrates.

(ii). Design methodologies considering the electro-thermal effects

The electro-thermal issues may become the most critical challenge for high-level SoP integration. When determining the process, device, circuit and system design, it is thus very critical to consider the impact of the electro-thermal effects on performance
and reliability. Thermal-aware design methodologies at device, circuit and system levels are all required. Some low-power, temperature-aware circuit and system design methods in CMOS ICs can be adopted in SoP integration for this aim. But new cooling and package design schemes are needed to be re-considered for SoP integration. According to the work in this dissertation, the optimal placement of the heat-pipes in the integration is also vital.

(iii). Hybrid technology and system integration

![Hybrid SoP Integration Diagram](image)

Figure 7.1: Illustration of the concept of three-dimensional hybrid SoP integration and the device design requirements.

In the past, methods have been developed to deposit and process material like amorphous-Si, poly-Si, c-Si and organic/inorganic nanostructured semiconductor materials that provides integrated devices by considering process constraints, cost and performance to perform different functions. For different functions like analogue signal processing, digital computing, RF communication, and pixel controlling in large-area display, imager or sensor arrays, different device technologies or configurations may required to achieve the best trade-off between performance and cost. Therefore, the processing of different function block at different layers may be preferred for such heterogeneous integrations, as shown in Fig. 7.1.
Bibliography


List of Publications

Journals


Conference Proceedings


Oral Presentations


• “A macro-modeling approach to integrate CNT field emission triode devices into circuit simulations,” IDW’06, Otsu, Japan, Dec. 2006.

• “Performance evaluation and design guidelines of sub-100-nm source/drain unilater-crystallized poly-Si TFTs for SoP applications,” IDW’06, Otsu, Japan, Dec. 2006.


• “Electrical properties and carrier transport mechanisms of nanometer-scale ultra-thin channel poly-Si transistors,” ICISCT, Shanghai, China, Oct. 2006.

• “Active-matrix addressed carbon nanotube field emission displays,” Northern Ireland Semiconductor Research Centre (NISRC), Queen’s University, Belfast, Nov., 2005.