Characterisation of Source-Gated Transistors in Amorphous Silicon

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Summary

This thesis is concerned with new devices named Source-Gated Transistors (SGT) prepared in hydrogenated amorphous silicon. The aim of the thesis is to characterise SGT's having Schottky barrier sources in order to obtain a clear understanding of how they work, how they compare with a standard FET and their potential application.

The construction and the principle of SGT operation differs from a conventional FET where the channel conductance is modulated by the gate voltage and current saturates when the drain region is depleted of charge. In comparison the current in the SGT is controlled by a reverse biased source barrier located opposite a gate electrode. Changing the gate potential affects the magnitude of the electric field at the source barrier and thereby the magnitude of the current flowing through the reverse biased barrier. Furthermore, saturation occurs when the semiconductor film is depleted by the reverse biased source barrier.

The electrical characteristics of the SGT are very different from those of standard FET. In the first place the saturation voltage can be very much smaller and therefore the device can be operated in saturation at lower drain voltages giving less power dissipation. Secondly, the SGT is much less sensitive to the drain field than a FET which is manifested as a much better output impedance. Due to its specific device construction, the SGT can be operated with lower carrier concentrations, higher internal fields and reduced short channel effects enabling the possibility of devices at sub-micron or nanometres scale to be prepared with superior characteristics. SGT's prepared in amorphous silicon are much more stable than FET's for the same driving current. Also for the same device stability the SGT can operate at higher currents.

Good agreement between experimental and simulated SGT transistor characteristics is presented allowing us to use Silvaco ATLAS modelling to obtain much deeper insight into SGT device physics. Where it was possible, experimental results are supported by modelling and vice versa. The influence of device geometry parameters such as source length, s-d separation, source barrier height, thickness of a-Si:H and SiN on the SGT properties is shown. It will be seen that these parameters are very closely linked together. These findings are used to improve transient and small signal response. The close link between the transient response and small signal response is presented and one can optimise the SGT device performance in both areas at once. In general the results show that stable, high performance electronics featuring SGT devices in amorphous silicon is a real possibility.
Declaration

This thesis is submitted for the degree of Doctor of Philosophy at the University of Surrey. It describes the research undertaken in the Nano-electronics group at the Advanced Technology Institute of the School of Electronics and Physical Sciences between January 2003 and October 2005. This work has been carried out under the supervision of Professor J.M. Shannon and Professor B.J. Sealy. Except where referenced, this work is original and has not been the result of collaboration. No part of this thesis has been or is currently being submitted for any other degree, diploma or any other qualification.

F. Balon
2005

Key words: Source-Gated Transistor, Amorphous Silicon, Field-Effect Transistor, TFT, Schottky barrier.
Acknowledgments

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Publications

Journal publications (related to SGT only)

- **F. Balon** and J. M. Shannon: *Analysis of Schottky Barrier Source-Gated Transistors in a-Si:H*, *Solid-State Electronics*, (accepted for publication), (2005)

Conference publications (all arising from oral presentations)

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\( C_s \) capacitance of the semiconductor per unit area [F/m\(^2\)]
\( C_G \) capacitance of the insulator per unit area [F/m\(^2\)]
\( C_a \) capacitance of the semiconductor under the active source barrier region [F]
\( C_g \) capacitance of the insulator over the active gate region [F]
\( t_{SN} \) thickness of silicon nitride (SiN) [nm]
\( t_{a-Si} \) thickness of amorphous silicon (a-Si:H) [nm]
\( S \) area of the source [um\(^2\)]
\( s \) length of the source barrier [um]
\( d \) source-drain separation of the parasitic FET [um]
\( w \) width of the source barrier [um]
\( g_m \) transconductance (or mutual conductance) of the device [S]
\( g_d \) output conductance of the device [S]
\( I_{SD} \) source-drain current [A]
\( J_S \) source current per unit area [A/um\(^2\)]
\( V_D \) drain voltage [V]
\( V_G \) gate voltage [V]
\( V_{SAT} \) drain saturation voltage [V]
\( V_{TH} \) threshold voltage [V]
\( q\Phi_B \) Schottky barrier height [eV]
\( \alpha \) tunnelling constant [nm]
\( \tau \) charging time [s]
\( \tau_{ON} \) turn-on time [s]
\( \tau_{OFF} \) turn-off time [s]
\( f_I \) cut-off frequency [Hz]
\( f_{MAX} \) maximum oscillation frequency [Hz]
Chapter 1

1 Introduction

History and present status

Electronics has the largest and most rapidly moving technological activity in world industrial development. People are still trying to improve the quality of their life. Consequently, there is more pressure from the electronics industry to develop even smaller and faster devices with very low energy consumption and high reliability at low cost.

The basic building block of all electronic systems is the Transistor, invented by Shockley, Brattain and Bardeen in 1947. The transistor was probably the most important invention of the 20th Century, and the story behind the invention is one of clashing egos and top-secret research. The first transistor was about half an inch high. That's mammoth by today's standards; now hundreds of millions of transistors can fit on a single chip. But in 1960 Bell scientist John Atalla developed a new transistor design based on Shockley's original field-effect theories. Today, most transistors are field-effect transistors.

Field-effect transistors (FET's) are so named because a relatively small electrical signal coming in through a controlling electrode creates an electrical field through the rest of the transistor. This field can be positive or negative to the other electrodes and controls a second current travelling through the body of the transistor. The field modulates the second current, which can be substantially larger. Consequently devices in which only one type of carrier participates in the current flow mechanism were developed. These are known as unipolar devices.

Transistors are based on semiconductor material. Currently more than 90% of world production of transistors is based on silicon. The rest of the production is dedicated to III-V semiconductors such as GaAs or GaN. When we say silicon, crystalline silicon is the normal form of silicon that comes to mind. However there are other forms of silicon such as polycrystalline and hydrogenated...
amorphous Silicon (a-Si:H). Both of these forms of silicon have become very popular because they can be deposited over large areas and be therefore useful for large area electronics. Displays and scanners that form the user interface between people and the electronic world, as well as solar cells and X-ray imagers, are examples of electronic devices where a large size is essential. This whole area in which inexpensive glass sheets or metal foils form the substrate and the active materials (e.g. a-Si:H) are deposited as a thin film, using thin film technology, at low temperatures is called Large area electronics.

**Novel Work Undertaken**

This thesis focuses on the characterisation and simulation of a new device – a Source Gated Transistor (SGT) made in hydrogenated amorphous silicon. To date the only transistor in large area electronics is a thin-film FET device (TFT), which has the characteristics of a conventional MOSFET. It has been proposed that SGT devices are able to overcome some fundamental limitations of FET’s.

The aim of this thesis is to fully characterise the SGT with a Schottky barrier source in hydrogenated amorphous silicon with the purpose of establishing exactly how it works and how its characteristics compare with a conventional thin-film FET. Having established the advantages and disadvantages of the SGT, the range of its application and potential can be explored.

**Structure of Thesis**

Work is developed in two main sections. The first section is based on the literature review of material properties, transport mechanism and structural stability of a-Si:H (chapter 2.) which is necessary for a deeper understanding of some of the SGT features. Furthermore this review summarises the physics and nature of the Schottky barrier which is a vital part of the SGT’s prepared in a-Si:H (chapter 3.). Next in chapter 3, the basic principles of FET’s (IGFET, MOSFET and thin-film FET) are discussed since it is necessary to be familiar with the FET prior the introduction of the SGT concept in order to better understand the differences and the SGT principle. Consequently the following chapter of this section (chapter 4.) introduces the concept and basic SGT transistor characteristics. The significant part of this thesis consists of the simulated and modelled results using ATLAS Silvaco device simulator package. Therefore chapter 5. introduces this simulation package and briefly deals with some issues such as density of states and boundary conditions related to the simulation of SGT devices in a-Si:H.

The second section dealing with experimental, modelled and calculated results is divided into several chapters. Firstly (chapter 6.) covers the technology part of preparation the SGT devices,
then the 2D simulations are shown to support the SGT concept suggested by Shannon and Gerstner [1] and deals with the importance of the source barrier. This is followed by discussions regarding the main distinguishing features of the SGT: small saturation voltage and high output impedance. A deeper insight into the SGT principle can be seen in chapter 7, where the dependence of device geometry (e.g. source length, source-drain separation, and thickness of a-Si:H and SiN) on the SGT properties is presented. An essential part of the SGT device is the source barrier therefore chapter 8, deals with analysis of the Schottky source barrier. The stability of the thin-film transistors in a-Si:H is a big problem because FET’s are notoriously unstable and degrade with time; therefore this issue is addressed in chapter 9, which compares FET and SGT device stability. The chapters 10, and 11, are important in view of applications and knowing the basic principle and properties of SGT from previous chapters one can effectively address the issues of the transient response and small signal response. The final section chapter 12, summarises the properties of a SGT and also compares SGT and FET properties in a-Si:H for the same layer thickness and dimensions.

This is followed by conclusions and future work in chapter 13. An example of the source code for Silvaco ATLAS device simulator can be seen in the Appendix.
Chapter 2

2 Hydrogenated amorphous silicon

2.1 Introduction

Hydrogenated amorphous silicon (a-Si:H) has become a well established material in semiconductor technology mainly for photovoltaic and active matrix display applications [1]. The most significant benefit of the a-Si:H is its large area deposition capability, which opens the possibility of new applications where large area is essential.

A-Si:H normally contains about 10% of hydrogen and exhibits the full range of semiconductor properties. Despite lower speed and current compared with standard single crystal silicon devices, there are many application areas where its properties in connection with thin film technology play an important role (e.g. thin film transistors (TFT’s) and photodiodes).

Hydrogenated amorphous silicon (a-Si:H) has proved to be material of choice for large area electronics basically for four reasons.

1) amorphous silicon can have the required semiconducting properties of doping, photoconductivity, junction formation and so on,
2) the plasma CVD deposition process lends itself to cover large areas, and indeed the material tends to have higher purity and greater uniformity, as the reactor size gets larger,
3) a-Si:H has similar chemical properties as its crystalline cousin – silicon. Therefore device fabrication takes advantage of much of the knowledge about processing crystalline silicon (c-Si) that has been gained through the microelectronics industry,
4) using a plasma CVD process allows the formation of a diverse set of alloy materials, which provide the passivation layers needed for electronics devices as well as semiconductors with a range of band gaps.
In this chapter we discuss the theoretical background of a-Si:H properties that are most relevant to its application in Thin-Film Transistors (TFTs), namely the structure, electronic density-of-states, the function of hydrogen and metastability.

### 2.2 Structure and Density – of – States of a-Si:H

The bonding disorder of the atomic structure is the main feature of amorphous materials and influences the electronic properties and design of the devices. The characterisation of amorphous materials demands different theoretical approaches with emphasis on the short-range chemical bonding interactions. Although there is disorder on an atomic scale the chemical bonding is the same as in c-Si, where the silicon atoms are 4-fold coordinated. As a model for amorphous material the random covalent network (RCN) is frequently used, in which each atom has a specific number of bonds with its neighbour - called coordination. Coordination can vary between 1, 3 and 4. This coordination factor significantly influences the doping and defect properties of a-Si.

The disorder is mainly represented by a distribution in the bond lengths and bond angles and it causes the broadening of the electron distributions of states, electron and hole localization as well as strong carrier scattering [2]. Scattering length of free electrons and holes is comparable with the interatomic spacing and consequently the free carrier mobility is decreased (10-20 cm²/Vs for electrons and less than 1 cm²/Vs for holes).

To conclude the main features of amorphous materials we can consider the three main features; the short-range order of an ideal network, long-range disorder and coordination defects [2].

1) Because the short-range order is preserved it results in a similar overall electronic structure as crystalline materials (e.g. conduction band, valence band, energy gap)

2) A broadening tail of states extending into the band gap replaces the abrupt band edges of crystalline material. This originates from the deviations of the bond length and angle arising from the long-range structural disorder. Despite the relatively small concentration of states in band tails they play an important role, because electronic transport occurs at the band edge. There are mostly weak Si-Si bonds in the band tails and the further they are from the band edge the weaker is the bonding.

3) Coordination defects and Si-dangling bond states deep within the band gap are localised. These defects determine many electronic properties by controlling trapping and recombination.

The electronic structure of an amorphous semiconductor depends sensitively on the density and energy distribution $N(E)$ of the localised gap states. Resembling the concept as used for crystalline semiconductors, the a-Si:H Density-of-States (DOS) distribution is divided into extended states of
the valence band and the conduction band, and band tails localized states within the band gap [2]. Tails of localized states extend from both bands deep into the gap. The DOS distribution including both intrinsic and extrinsic defect states is shown schematically in Fig. 2.1.

The simplest intrinsic defect is an unsaturated bond — the so-called "dangling" bond (DB) — the neutral state of which is located around midgap in undoped material. A silicon atom is able to create bonds to up to four neighbouring atoms however during the deposition process it is more likely that not all 4 covalent bonds are created to silicon atoms and each of the unsaturated positions is one DB. DBs can be occupied by zero, one, or two electrons, which results in a positive, neutral or negative charged state, respectively. Dangling bonds are effective recombination centres [3] and reduce the lifetime of free carriers.

![Fig. 2.1 Schematic density of states distribution in a-Si:H.](image)

In a-Si:H containing typically around 10 at.% hydrogen, the vast majority of DBs are passivated with hydrogen by forming Si – H bonds. This reduces the defect density substantially to typically around $10^{16}$ cm$^{-3}$ in the middle of the band in the case of undoped a-Si:H. Both the concentration and energy distribution of these states are determined by the position of the Fermi level [1, 2, 3].

It has been found that in a-Si:H semiconductors, deep defects are created by breaking of weak bonds when the bandtail states are populated. This can be achieved by longer exposure to light [4], strong accumulation in the conduction channel of an a-Si:H TFT [5] and doping [6].

These defect states have a major effect on the doping efficiency, transport and recombination as well as width and potential profile of space charge layers in devices. Moreover all these material properties are defined at the time of growth and depend on details of the deposition process and growth conditions respectively. Therefore the optimisation of growth process is essential to achieve suitable material properties of a-Si. The growth process is beyond the scope this work, but there is one significant issue that has to be mentioned, the role of hydrogen in a-Si.
2.3 Hydrogen in a-Si:H

Hydrogen-free a-Si films prepared by evaporation or sputtering contain a large number of microvoids of size 1-10 nm. If the surface is devoid of hydrogen, then the arriving species such as Si or Si₆ can have only a very small surface diffusion coefficient \(D_s\). This fact suppresses the structural relaxation and causes the development of microvoids in the Si network [2].

One of the methods for growing a-Si:H films is plasma enhanced chemical vapour deposition (PECVD) [2, 7]. During PECVD atomic hydrogen can partially penetrate the silicon network. The stable bonding configurations are the Si – H bonds and unstrained Si – Si bond which are too strongly bonded to be broken by hydrogen. On the other hand, the chemical potential of the hydrogen is high enough to break the highly strained Si – Si bonds. The broken bonds either remain as Si – H bonds or are reconstructed into stronger Si – Si bonds. Fortunately the hydrogen in the growing film gets rid of its weak strained bonds, resulting in a more relaxed and ordered network. Of course such a process occurs only when there is sufficient hydrogen diffusion at the surface during the growth. Secondly this is a reason why an elevated growth temperature is needed for best quality films.

The ability of hydrogen to move into, out of, and within a-Si:H has both beneficial and undesirable properties (see Fig. 2.2). The low defect density is a beneficial result of the hydrogen bonding to weak or broken silicon bonds. Hydrogen is also considered to relieve stress and saturate dangling bonds. However, hydrogen is responsible for the instability of a-Si:H at increased temperature and is completely removed from a-Si:H above 400 °C causing deterioration of properties [2].

![Fig. 2.2 Schematic diagram showing a possible hydrogen diffusion mechanism: (a) the potential wells corresponding to the trapping sites and the energy of the mobile hydrogen; (b) the motion of the hydrogen through the Si – Si bonds.](image_url)
2.3.1 Stability of a-Si:H

According to Stutzman et al. [8] the applicability of any electronic material for device applications is determined by two requirements – i) electronic quality and ii) structural stability.

The electronic quality is a relative measure of the efficiency with which a material can be excited out of its ground state, \( Q \), into an excited state, \( Q^* \). Excitation can be presented in many forms e.g. by irradiation with photons, charge carrier injection or applying of an external field.

The structural stability describes how the bonding configurations of the same material may change under conditions of prolonged or repeated electronic excitation. Repeated electronic excitation is generally encountered in all electronic devices during their operation.

In structurally stable materials, the energy minima of the ground state, \( Q \), and excited state, \( Q^* \), occur close together so that excitation (transition \( Q \rightarrow Q^* \)) or relaxation (transition \( Q^* \rightarrow Q \)) do not give rise to significant changes in the atomic positions. This situation is denoted in Fig. 2.3a.

In contrast, unstable or metastable structures are characterised by energy minima \( Q \) and \( Q^* \) which occur at sufficiently different configurations. Electronic excitation is then followed by a significant lattice rearrangement as the system relaxes into the new structure corresponding to the minimum of the \( Q^* \)-curve (see fig. 2.3b). If this minimum is at lower energy than the crossing point of the \( Q \) and \( Q^* \) curves, the relaxed excited state is metastable in the sense that the system has to overcome an energy barrier \( E_b \) in order to return to its ground state [8].

![Fig. 2.3 Energy configuration diagrams for a) stable and b) metastable structural configurations.](image)

Fig. 2.3 Energy configuration diagrams for a) stable and b) metastable structural configurations.

\( Q \) and \( Q^* \) represent the ground state and excited states of the system. [8]

Generally, the formation of metastable states will be more pronounced for systems where electronic excitation energy can be coupled back to the structural degrees of freedom effectively
in other words where the states are localised. Metastable states should occur more commonly in materials containing configurational coordinates with small force constants for lattice distortions, or in atomic configurations with closely spaced potential energy minima, because in such systems relatively large atomic displacements are possible with small increase in potential energy.

The bonding disorder in amorphous materials gives rise to both a large density of localised electronic levels (tails in valence and conduction band) and a large number of prestrained structural units with low force constants for atomic displacements (weak or wrong bonds). The only criterion that is not generally met in amorphous materials is their lack of the electronic quality due to high deep defect density. Nowadays it is possible, however, to prepare amorphous silicon (a-Si:H) with electronic quality acceptable for practical applications (see chapter 2.5). The presence of hydrogen is not only responsible for the better electronic quality but also introduces an additional structural component with a high lattice mobility. Thus it is now widely believed that many but not all of the metastability effects encountered in a-Si:H are related to the presence of hydrogen.

As it was said, additional energy is required to transfer a system to its metastable configuration. This additional energy has to be provided by an external excitation source (e.g. by irradiation with photons, charge carrier injection or applying of an external field). In the literature the most frequently discussed instability phenomena is light or irradiation induced metastability. This effect was firstly observed by Staebler and Wronski [4]. Staebler and Wronski found that glow discharge deposited a-Si:H films illuminated with strong light (~200mW/cm²) suffered from reduced photoconductivity and dark conductivity and that these properties return to their as-deposited values after annealing at temperatures above 160°C.

Numerous models have been proposed to explain this effect [9]. It became clear that dangling bonds were produced (by breaking weak Si-Si bonds), which acted as recombination centres located near midgap thus reducing the dark conductivity. Latest results show that not only dangling bonds are produced but also larger structural changes in the material involving the Si-network [10].

Jackson et al. [11] suggested that band-tail carriers must be involved in the creation of deep defects. There are two proposed ways, how carriers can induce bond rearrangements and produce metastable defects deep in the gap approximately at the energy location of the silicon-dangling bond:

i) the excess of the carriers break weak Si – Si bonds which are subsequently stabilised by the diffusion of hydrogen

ii) the excess of the carriers can increase the release rate of hydrogen from the silicon (break Si – H bonds)
and also the combination of both can be true. In doped a-Si:H a third possibility for metastable changes has been proposed due to changes in dopant bonding configuration.

This hydrogen-diffusion model for the creation of defects is pictured in Fig.2.4. The hydrogen atom diffuses to a special site (weak Si – Si bond) where it creates a dangling bond and leaves behind another dangling bond ($D^0$).

$$\text{SiH} + \text{SiSi} \leftrightarrow D^0 + \text{SiHSi} \quad (2.1)$$

The breaking of the weak Si – Si bond, creation of the dangling bond and trapping of the hydrogen at this site occurs only if a band-tail carrier is present. Therefore in accumulation when tail states are populated and carrier (electrons or holes) density is increased at the nitride a-Si:H interface (e.g. like in FET transistor in accumulation) defects are created inside the a-Si:H. In particular this means that if the Fermi energy is near the conduction band (for electron accumulation), dangling bonds deep in the gap are most likely to appear which are energetically more favourable [12].

![Fig. 2.4 Hydrogen diffusion model for creation of DB defects. a) Before hydrogen diffusion and b) after DB creation. [11]](image)

The presence of electrons in the accumulated region changes the equilibrium point of the reaction (2.1), and as a consequence the equilibrium point of the reaction (2.2) is pushed to the right site, which results in higher defect formation and new equilibrium state.

$$D^0 + e^- \leftrightarrow D^- \quad (2.2)$$

In other words neutral dangling bonds ($D^0$) that trap one electron become negatively charged ($D^-$) and reduce the band-tail carrier density which brings the quasi-Fermi level back towards midgap. The process stops only after the Fermi-level is restored to midgap (in undoped material). Alternatively, holes in the valence-band tail states can also break weak Si-Si bonds. But when the Fermi level is close to the valence band, dangling bonds are more likely to be created high in the band gap (energetically favourable states for holes) creating positively charged DB’s ($D^+$).
The process of creating metastable states is independent of the origin of the extra electrons and can result from applied fields, light exposure or doping, all of which can change the position of the quasi-Fermi level. The situation, in the case of doping, is shown in Fig. 2.5 where the calculated and experimentally measured gap-state defect distributions for n-type, intrinsic and p-type a-Si:H are shown [13].

As described above if the Fermi level lies near the conduction band-tail (for n-type) the defects are created at low energy near the valence band-tail in order to acquire chemical equilibrium. In the case of p-type material defects are created at a high energy level, which is more favourable for holes [14]. The $\mathcal{U}$ shown in Fig. 2.5 is the correlation energy, defined as an extra energy required to place a second electron on a singly occupied localized defect level.

![Fig. 2.5](image)

**Fig. 2.5** a) The calculated and b) experimentally measured gap-state defect distributions for n-type, intrinsic and p-type a-Si:H. [13]

### 2.4 Transport mechanism and properties

In an amorphous semiconductor the electronic states are localised below some energy $E_C$ in the conduction band and above $E_V$ in the valence band (Fig. 2.1). The energies $E_C$ and $E_V$ that separate extended and localized states are called mobility edges. The mobility edge at energy $E_C$ derives its name because at zero temperature, only electrons above $E_C$ are mobile and contribute to conduction. The energy of the mobility edge within the band depends on the degree of disorder and is typically $0.1 - 0.5$ eV from the band edge in all amorphous semiconductors. The higher degree of disorder the further will be the mobility edge from the band edge. In hydrogenated a-Si:H the mobility gap is $\sim 1.8$ eV. The disorder also influences the mobility of the electrons and
holes above the mobility edges. In the extended states the mobility is considered to be in the range 1 — 10 cm²/Vs, while in localised states the mobility is much lower and determined by thermal activation and hopping between states.

The values for the carrier mobilities at the mobility edges $\mu_n$ and $\mu_p$ are obtained from transient experiments (Table 2.1). A multiple trapping model is frequently used to interpret the measured data. This model proposes that carriers move at the mobility edges and interact with localised states in the bandtails by trapping and thermal release. Therefore values of $\mu_n$ and $\mu_p$ are based on assumptions about the distribution of the localized states. The drift mobility is the free carrier mobility reduced by the fraction of time that the carrier spends in the traps, so

$$\mu_D = \frac{\mu_0 \tau_{\text{free}}}{(\tau_{\text{free}} + \tau_{\text{trap}})}$$

Table 2.1 Transport properties of undoped a-Si:H [3].

<table>
<thead>
<tr>
<th></th>
<th>Drift Mobility ($\mu_D$) (cm²/Vs)</th>
<th>Activation Energy (eV)</th>
<th>Band Mobility ($\mu_{b}^f$) (cm²/Vs)</th>
<th>Bandtail Slope (eV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrons</td>
<td>$&lt;0.8$</td>
<td>0.13</td>
<td>10</td>
<td>0.027</td>
</tr>
<tr>
<td>Holes</td>
<td>$10^{-3}$</td>
<td>0.32</td>
<td>0.67</td>
<td>0.043</td>
</tr>
</tbody>
</table>

In doped a-Si:H films the Fermi level moves into the band tails, but never closer than 0.1 eV from the mobility edge. Therefore there is no metallic conduction, but there are other possibilities for current transport. Three main conduction mechanisms are [2]:

1. **Extended state conduction** — Conduction is by thermal activation of carriers from $E_F$ to above the mobility edge. The activation energy is the separation of the mobility edge from the Fermi level, and can vary from 1 eV in undoped a-Si:H to 0.1 eV in n-type material.

2. **Band tail conduction** — Carried by hopping conduction in localized states. It is possible only at elevated temperatures and depends on density-of-states and the overlap of the wavefunctions.

3. **Hopping conduction at the Fermi energy** — This conduction mechanism occurs when the density-of-states is large enough for tunnelling of electrons and varies greatly with defect density. Conductivity is small but weakly temperature dependent. It tends to dominate at the lowest temperature. In a-Si:H hopping conduction is almost completely suppressed by adding hydrogen (strongly decreased defect density).

An important property of a-Si:H is the presence of midgap states. As a result the absorption of this material in the visible wavelength region is about 100 times higher than that of crystalline silicon.
2.5 Current applications of a-Si:H

Thin film silicon (a-Si:H) prepared at low temperatures is an attractive semiconductor material for industry. It has been applied in a variety of large area devices. In this part the most common applications of a-Si:H are described. Extensive descriptions of these applications can be found, e.g. in the book by Street R. [1, 15].

2.5.1 Active matrix liquid crystal displays (AMLCD)

The AMCLD is a flat panel display in which the display medium is a liquid crystal and each pixel is controlled by active devices. These active devices are arranged in a matrix on a glass substrate to control each pixel. The most commonly used active device is a thin film transistor (TFT) described in chapter 3.

The crossed polarizer TFT LCD consists of the backlight, rear polarizer, TFT substrate (glass), liquid crystal, colour filter substrate and front polarizer respectively. The twisted-nematic type of liquid crystal cells are generally used where orientation of the liquid crystal molecules (LCM) is twisted 90° between the TFT substrate and color filter substrate. The first polarizer works as a backlight polarizer and the other acts as an analyser. In this system light passes through analyser when there is no applied voltage on the cell, and is blocked when the applied voltage is sufficient to align the LCM vertically. White light illumination is generally used as a backlight with the three primary colours, red, green and blue, selected using a colour filter (see Fig. 2.6).

![Fig. 2.6 Vertical structure of a pixel in a colour LCD panel [16].](image)

The TFT substrate consists of two arrays; the TFT and external terminal pads on which LSI (large system integration) circuits are bonded to drive the TFT panel. The LSI is usually a scan generator for horizontal and vertical buslines. The TFT is formed at each intersection of these buslines and acts as a switch through which the voltage is applied to the liquid crystal cell (see Fig. 2.7). This
cell, which effectively behaves as a capacitor ($C_{le}$), is in parallel with a storage capacitor ($C_s$) or additional capacitor to improve the retention characteristics of the signal charge.

![Diagram of one pixel of a TFT panel with equivalent circuit diagram](image)

**Fig. 2.7** Drawing of one pixel of a TFT panel with equivalent circuit diagram [16].

### 2.5.2 PLED and OLED displays

The history of organic electro-luminescence diode is quite short. It began in 1987 when Kodak and Pioneer decided to invest in OLED technology [17]. Their approach was to use metallic impurities acting as recombination centres inside the host matrix of small organic molecules (Diamine). But an equally significant development came in 1990 with the discovery that conjugated polymers such as Poly(p-phenylenvinylene) (PPV) were able to emit light and were suitable for organic light emitting diodes (OLED) [18]. This area is progressing very rapidly and is considered to be a replacement for AMLCD displays (mentioned above) in the near future. OLED displays offer significant advantages over AMLCDs:

a) OLED displays require no backlighting, which means they are smaller in size (thinner), use less power, weigh less and cost less. By contrast, AMLCDs require either an external light source (reflective type) or a fluorescent or LED backlight (transflective type).

b) OLED's self-luminous nature is also responsible for other important advantages. They have a virtually unlimited viewing angle (165°). LCDs, on the other hand, are limited by the "aperture" effect. In addition, OLED's have very high brightness and contrast (>100:1). Moreover a backlit LCD typically looks "washed out" under bright light.

c) OLED displays have almost instantaneous update speed. The slow response time of LCDs due to relaxation of the liquid crystal has always been a problem for high definition displays, particularly when displaying real-time video. The switching speed of the OLED is in the microsecond region and this problem has been eliminated.
There are two basic OLED concepts: i) small molecular OLEDs (SMOLEDs) use organic material with very small molecular structures and layers can be deposited by vacuum vapour deposition, ii) polymer OLED (PLED or Poly-LED) utilise organic materials with much longer polymer chains often applied by spin coating or ink-jet printing methods [19].

Active matrix AMOLED displays stack cathode, organic, and anode layers on top of another layer - or substrate - that contains the drive circuitry. On the substrate there is a TFT backplane made in amorphous silicon or organic material (similar to that described in section 2.5.1). Since amorphous silicon technology is more mature and widely used the backplane is mostly in a-Si:H. The driving circuits can be based on poly-Si or Si circuits bonded to the substrate. Each pixel is driven independently: a corresponding circuit delivers current to the cathode and anode materials, holes and electrons are injected and light is emitted during recombination.

Organic light emitting diodes consist of one or more semiconducting organic layers, which are positioned between two electrodes. First a conductive, transparent anode material such as indium-tin-oxide (ITO) is deposited on a transparent substrate (plastic or glass). Next, the organic layers are added. The organic layer stack consists of a hole-injection layer, a hole-transport layer, an emissive layer, and an electron-transport layer (see Fig. 2.8). Lastly, a reflective metal cathode of magnesium-silver alloy or lithium-aluminium completes the structure. Nowadays the thickness of the structure, minus the substrate, is only about 100nm [20].

![Fig. 2.8 Schematic structure of bottom emitting OLED device.](image)

When an appropriate voltage (typically between 2 and 10 volts) is applied to the cell, the injected positive and negative charges recombine in the emissive layer to produce light (electroluminescence). In order to maximize the light output (efficiency) from the OLED device the structure of the organic layers and the choice of anode and cathode are designed to maximize the recombination process in the emissive layer.
Typically the luminance intensity in practical display applications is about 500 cd/m$^2$ per pixel. In the past OLED devices had poor efficiency and the driving voltage (6-7V) and current densities (~5mA/cm$^2$) were quite high (driving current ~1uA per pixel of 175x175um) [17] but with the latest development in the material and technology the efficiency and lifetime has improved rapidly. Very good results have been reported by Novaled GmbH, Germany [20] the current efficiency at 1000cd/m$^2$ is above 61cd/A driving the OLED device at 2.9V with current density 2mA/cm$^2$ (see Fig.2.9). In Fig.2.9 the luminance intensity versus applied field is shown for an OLED device. The efficiency and driving current/voltage usually varies with the wavelength emission (colour) of the LED. Novaled GmbH announced the world best results (in Feb. 2005) for a green OLED with measured power efficiency 110 lm/W and luminance in excess of 1000cd/m$^2$ [21]. The most technologically challenging issue is creating a blue OLED with good efficiency and lifetime (to date achieved above 6000hrs) [22, 23].

![Fig. 2.9 Electroluminescence intensity versus applied field for CBP * Ir(ppy), active layer electrophosphorescent OLED's.](image)

There are also two possible constructions of OLED devices with i) bottom (see Fig.2.8 above) and ii) top emission. The importance of top emission OLEDs originates from the specific layout of active matrix backplanes. A substantial part of the backplane area is covered with non-transparent TFTs, capacitances and supply lines. Furthermore electron injection occurs from the substrate contact and therefore the organic layer stack is inverted (Organic Inverted LED-OLED) [24]. In the case of a bottom emission display this design leads to a decreased overall aperture ratio, whereas a top-emitting display can still offer a high fill factor and thus a higher lifetime. An increase of the overall aperture ratio from 40% (a typical value for a bottom emitting display) to 75% which are obtainable for top emitting devices reduces the necessary pixel brightness by 47%. The current densities are reduced and thus device lifetime higher by a factor of three – under the assumption that lifetime and efficiency of top and bottom emitting OLEDs are similar [25].
2.5.3 Large area image sensor arrays

The majority of the imaging sensors for the visible wavelength such as used in the digital cameras and camcorders is very small and use lenses to focus the projected image down to small size recorded by the sensor. However it is not possible to use the lenses for X-ray therefore here a large size of image sensor is a must.

Large area image sensors are two-dimensional arrays of pixels frequently used for medical and industrial X-ray imaging, X-ray crystallography and document scanning. Each pixel is light sensitive and transforms radiation to a corresponding charge. This charge is stored in a capacitor until it is transferred to the external electronic circuits. Any pixel consists of a sensor, a charge storage capacitor to hold the charge until it is read out, and a switching unit to control the readout. The pixels are linked together with address lines that cross the sensor array.

TFT’s and p-i-n diodes are mostly used in image sensor arrays. A schematic view of an a-Si:H p-i-n photodiode is illustrated in Fig. 2.10. The photodiode consists of very thin p and n doped layers with a thicker undoped layer between. The doped layers provide rectifying contacts but do not contribute to the light sensitivity, because doping causes a high density of charged dangling bond defects in a-Si:H - negative in n-type and positive in p-type material. Therefore the minority carrier lifetime in doped a-Si:H is so small that most electrons generated in the p-region and holes in the n-region recombine before they can cross the reverse biased junction. At shorter wavelength the absorption is stronger and therefore losses in the doped contact layer become more important.

Absorption of light in the photodiode generates electron-hole pairs in the intrinsic layer. The charges separate under the action of the electrical field and cause a current to flow when an electrical circuit is closed. The electric field includes the internal built-in potential and the applied reverse voltage. The photocurrent \( J_{ph} \) as a result of a light flux \( G_L \) and quantum efficiency \( \eta_{qie} \) \((V, \lambda)\) is given by
The quantum efficiency includes a bias dependent charge collection efficiency and wavelength dependent absorption that generates electron-hole pairs.

The reverse bias dark current is mainly attributed to the thermal generation of electron-hole pairs via mid-gap defect states. Here electrons are thermally excited from the valence band to empty or singly occupied defect states to the conduction band, resulting in electron-hole pairs, which are collected by the electrodes under the reverse electric field.

### 2.5.4 Solar cells

A-Si:H has major advantages compared to crystalline Silicon – the absorption efficiency is approximately from 1 to 2 orders of magnitude higher in the visible and UV spectra due to mid gap defect states [2]. Since the first a-Si:H solar cell was made by Carlson et al. [26] the technology has improved tremendously, leading to reported initial efficiencies exceeding 15\% [27]. A schematic layout of an a-Si:H solar cell is shown in Fig. 2.11 [28]. The construction and principle is very similar to a p-i-n photodiode. In this case the active device consists of three layers: a p-type a-SiC:H layer, an intrinsic a-Si:H layer and an n-type a-Si:H layer. Because the intrinsic layer is sandwiched in between the doped layers, an internal electric field is present across the intrinsic layer. Therefore the intrinsic layer is depleted of free charge carriers. After irradiation, electron-hole pairs are generated in the intrinsic layer and separated by the internal electric field. The carriers then drift under the influence of the internal electric field to the electrodes.

![Schematic representation of an amorphous silicon solar cell](image)

Glass covered with transparent conductive oxide (TCO - SnO\textsubscript{2}) is used as a substrate. In order to obtain a high efficiency solar cell, this TCO is textured. Consequently incoming light is scattered and absorption of the light is enhanced. It is desirable that the contribution to the photocurrent from the absorption in p-type a-Si:H layer should be rather low. A smaller absorption (i.e. higher
optical gap) is achieved by alloying the a-Si:H with carbon. Next the combination of ZnO layer with Ag layer leads to a highly reflective back contact and an improved solar cell response [28].

Despite all sustained and intense efforts to eliminate the Staebler-Wronski effect (S-W effect, discussed in chapter 2.3.1) from a-Si:H materials and solar cells it has remained a problem for three decades. Under the influence of S-W effect the electrical output of a solar cell decreases over a period of time when first exposed to sunlight. Eventually, however, the electrical output stabilizes. This effect can result in up to a 20% loss in output before the material stabilizes. This instability severely limits the opto-electronic properties of the material and the performance of corresponding devices.

On the other hand, the S-W effect can be substantially reduced by diluting the silane (SiH₄) source gas used for plasma-assisted deposition of amorphous silicon with hydrogen [9, 13]. Today's multi-bandgap, multijunction designs are driven by the need to make thin layers to minimize the S-W effect. Another promising concept of the “sunproofing” of solar cells is to use mixed-phase cell materials that consist of clusters of nanocrystalline silicon embedded in an amorphous matrix [29]. The crystallites make this mixed phase material quite stable with the exception of the grain boundary region. There is a large excess of hydrogen at the boundary due to mismatch of the material and this is necessary in order to remove light-induced damage (degradation).

2.6 Chapter summary

In this chapter the basic properties of hydrogenated amorphous silicon are summarised. The chapter deals with the structure of a-Si:H, density of states and their distribution. Next the role of hydrogen was discussed and its importance during the growth and the influence on material metastability. The degradation of a-Si:H under prolonged exposition of light and electric field was outlined and a model suggesting of the importance of band tails carriers was presented based on the literature. This was followed by outlining the transport mechanisms in a-Si:H and the most common applications of a-Si:H in large area electronics.
Chapter 3

3 Basic concepts of standard unipolar devices

3.1 Introduction

Unipolar devices are a category of semiconductor devices in which only one type of carrier predominantly participates in the conduction process. Several types of unipolar devices have been developed [30]. The simplest unipolar device (UD) is the metal-semiconductor contact. Among the best known UD’s are the junction field-effect transistor (JFET), the metal-semiconductor field-effect transistor (MESFET) and the metal-oxide-semiconductor field-effect transistor (MOSFET).

This chapter concentrates on the basic principles of the metal-semiconductor contact and the most frequently industrial used device the Insulated-Gate Field-Effect Transistor (e.g. MOS FET) and its thin film equivalent known as the thin-film transistor (TFT).

3.2 Metal – Semiconductor contacts

The metal – semiconductor (M-S) contact is the most commonly used structure to interconnect electronic devices within the chip as well as create connection with the “outside world”.

The properties of the M-S contact vary widely but mainly depend on the metal and on the type of semiconductor used. Such devices may pass current easily into and out of junction (labelled ohmic contacts) or they may be rectifying and allow easy current flow in only one direction. This rectifying property is employed in MESFET’s and Schottky barrier diodes [30, 31].
3.2.1 Rectifying junction - Band diagrams

The band diagrams for a metal (gold) and N-type semiconductor (silicon) that are not in contact are shown in Fig. 3.1. For comparison of both diagrams the common energy level, the vacuum level \( E_0 \) is used. The vacuum level, \( E_0 \), is defined as the energy that an electron needs to just become free and rest outside of the solid. \( E_0 \) is taken as a zero energy level and all other energy levels shown in figures represent negative energies.

The Fermi energy level \( E_F \) represents the average energy of an electron in the system. The energy difference between the \( E_0 \) and \( E_F \) is labelled the work function (\( \Phi \)) of the solid. The work function is therefore defined as the energy required to move an electron from \( E_F \) to \( E_0 \), where it is at rest and free of the influence of the solid. The Fermi level in extrinsic semiconductors is not fixed and is determined by the degree of doping and is located between the valence (\( E_V \)) and the conduction (\( E_C \)) bands. However in metals the Fermi level is located slightly above the bottom of the \( E_C \). In semiconductors the energy difference between \( E_0 \) and \( E_C \) is fixed and labelled as the electron affinity (\( \chi_s \)).

When the metal work function (\( \Phi_m \)) is greater than the semiconductor work function (\( \Phi_s \)), the electrons in the semiconductor have an average energy higher than those in metal. This is the reason why above \( E_C \) of the semiconductor, the density of electrons is greater than that of electrons in the metal. This particular case is shown in Fig. 3.1.

Fig. 3.1 (a) Energy levels of metal and N-type semiconductor (not in contact). (b) Fermi function. (c) Carrier density distribution function [30, 31].

Also in Fig. 3.1 the Fermi distribution function \( f(E) \) and density of states distribution \( N(E) \) versus energy are shown. Fermi distribution deals with the probability of occupancy by electrons, of a state, at energy \( E \).
When the metal makes an intimate contact with the semiconductor, due to different work functions, electrons will travel from the semiconductor into the metal until equilibrium is reached and Fermi levels are aligned (Fig. 3.2). As a result the semiconductor becomes positively charged with respect to the metal and a depletion layer is formed. An electric field is thus built in and a potential barrier is established, accompanied by the bending of the bands \((E_C, E_V \text{ and } E_0)\). In thermal equilibrium the total electron flow in both directions will be the same and current across the junction is zero. An energy barrier for electrons \(qV_{bi}\) is formed in the semiconductor at the surface of the contact with the metal, preventing electrons from moving into the metal. This barrier \(V_{bi}\) (where \(V_{bi}\) is built-in voltage) is defined as:

\[
qV_{bi} = q(\Phi_m - \Phi_s)
\]

(3.1)

The barrier for electrons in the metal is called a Schottky barrier. The Schottky barrier \(q\Phi_B\) represents the energy barrier that electrons in the metal must overcome to move into the semiconductor and for an ideal contact is expressed by this formula

\[
q\Phi_B = q(\Phi_m - \chi_s)
\]

(3.2)

The ideal values of the Schottky barrier height are in general smaller than actual values mainly due to surface states that are produced as the crystal lattice is disrupted. These provide a large number of energy states located within the forbidden gap at the interface, which are characterised by a neutral level \(E_N\) \([31, 32]\). The surface states are occupied up to \(E_N\) and empty above. In practical M-S contacts whenever \(E_N > E_F\) the net charge of the interface is positive, or donor like, so that fewer ionised donors are needed in the depletion layer to reach equilibrium. As a result the
built-in potential is reduced as well as the barrier height. If $E_N < E_F$, the barrier is increased to bring $E_F$ closer to $E_N$ and reach equilibrium.

Thus charge on the interface has a negative feedback effect, which tends to keep $E_F$ closer to $E_N$. If the interface states density is large enough then the Fermi level is effectively pinned down at $E_N$ and $\Phi_B$ becomes independent of the work function.

Although this theory explains the Fermi level pinning effect it assumes that the distribution of interface states is a property of only the bulk semiconductor material and is difficult to rationalize from the standpoint of general physics and chemistry. Lately two other models have been developed i) Metal-induced gap states and ii) bond polarization theory in order to explain Fermi level pinning [33]. Clearly when metal and semiconductor form a M-S interface a significant redistribution of charge is expected due to the overlap of the tails of the wave functions of the conduction band electron from both sides. The effect of metal is to perturb intrinsic states by changing the matching conditions at the surface. Even though these theories have different explanation the final outcome of these theories is the same - Fermi level pinning.

### 3.2.2 Current-transport mechanism

When a metal semiconductor junction is under bias there are several ways in which charge carriers can be transported across a metal-semiconductor junction. Under forward bias these mechanisms are:

- a) emission of electrons from the semiconductor over the top of the barrier into the metal;
- b) quantum-mechanical tunnelling through the barrier;
- c) recombination with minority carriers in the space-charge region;

The same processes take place under reverse bias. It is possible to make a practical Schottky-barrier diode where (a) is the most important transport mechanism and then these diodes are labelled as 'nearly ideal'. The processes (b and c) cause departures from ideal behaviour.

#### 3.2.2.1 Forward biased

An applied voltage causes a change in the bending of the bands in the semiconductor and a corresponding change in the electric field at the metal-semiconductor (M-S) junction [30, 31].

The barrier in the semiconductor is reduced when a forward bias is applied (positive polarity on metal). As the barrier is reduced, more electrons cross from the semiconductor into the metal. But the number of electrons from metal to semiconductor is still the same because the Schottky barrier height is unchanged (Fig. 3.3).
Before electrons can be emitted over the barrier into the metal they have to be transferred from the inner semiconductor to the interface. During the transfer this process is governed by usual mechanisms of diffusion and drift in the electric field of the barrier. When they arrive at the interface the emission is determined by transfer rate of electrons across the boundary at the M-S interface. Effectively these two processes are in series and the current is determined by whichever causes bigger obstruction to the flow of electrons. If the first process is dominant limiting factor, the a) diffusion theory (of Wagner 1931, Schottky and Spenke 1939) is more applicable but if the second is more important the b) thermionic-emission theory (of Bethe 1942) can be applied [34]. The diffusion theory assumes that at the interface the electron quasi-Fermi level in semiconductor drops down through the depletion region and coincides with Fermi level in the metal. The assumption made in thermionic-emission theory is that the electron quasi-Fermi level remains flat and does not coincide at the interface with Fermi level of the metal.

In practice the true behaviour of the transport can lie somewhere between these theories and a combined thermionic-emission/diffusion theory has been developed (by Crowell and Sze, 1966) [30, 34] which fully reflects the original Bethe criterion. The Bethe’s criterion for thermionic-emission is that the mean free path for electrons $l$ must exceed the distance $d$ ($= kT/qE_{max}$) in which the barrier falls through an amount $kT/q$ (Fig. 3.4). The electrons moving towards the metal will make their last collision at the distance $q$ from the maximum and after collisions their energy drops. They will only be able to surmount the barrier if their kinetic energy is higher than the energy by which conduction band rises over a distance $l$. Hence if the conduction band rises more than $kT$ at distance $l$, only small fraction of electrons will be able enter the metal and the vast
majority will be reflected back. On the other hand if \( t \ll d_i \), nearly all electrons will be able to cross the barrier and the flow into the metal.

**Fig. 3.4** Electron quasi-Fermi level in a forward-biased Schottky barrier: i) according to the diffusion theory (dotted line) and ii) thermionic-emission theory (dashed line). The broken circle shows the energy distribution of electrons which make their last collision at a distance \( l \) from interface [34].

The analysis reveals that diffusion and thermionic emission theories have almost similar conclusions and for the crystalline semiconductors (high mobility materials) where Bethe's criterion for thermionic emission is fulfilled the current can be rewritten in the following form

\[
J_n = J_0 \left\{ \exp \left( \frac{qV_a}{kT} \right) - 1 \right\}
\]

(3.3)

here the \( J_n \) is the current density and \( J_0 \) saturation current density defined as

\[
J_0 = A^* T^2 \exp \left( - \frac{q\Phi_B}{kT} \right)
\]

(3.4)

where \( T \) is absolute temperature, \( k \) is the Boltzmann constant and \( V_a \) the applied voltage. The \( A^* \) is Richardson constant modified to take in to account the effective mass of electrons in the semiconductor, quantum-mechanical reflection of those electrons which are able to negotiate the barrier, and phonon scattering of electrons between the top of the barrier and surface of the metal.

The minus one term (in Eq.3.3) ensures that the current is zero if no voltage is applied as in thermal equilibrium any motion of carriers is balanced in both directions. In low mobility semiconductors (such as amorphous materials) the current transport in forward direction is controlled by diffusion theory.

In practice Schottky diodes never satisfy the ideal equation (3.3), but can be more closely described by the modified equation
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\[ J_n = J_0 \exp \left( \frac{qV_a}{nkT} \right) \left[ 1 - \exp \left( -\frac{qV_a}{kT} \right) \right] \]  \hspace{1cm} (3.5)

where \( n \) is an ideality factor (which might depend on temperature) approximately independent of \( V_a \) and is greater than unity. There are many reason why \( n > 1 \) the most common is the bias dependence of \( \Phi_B \).

In the case of very heavily doped semiconductors particularly at low temperature it is possible for electrons with energies below the top barrier to penetrate the barrier by quantum-mechanical tunnelling. If the current arises from the electron tunnelling with energies close to Fermi level this is known as field emission. If the temperature is raised, electrons are exited to higher energies and tunnelling probability increases because the electrons see thinner and lower barrier but number of electrons decreases with increasing energy. Therefore there will by a certain maximum of current contribution at energy \( E_m \) above the conduction band (see Fig.3.5). This process is known as thermionic-field emission. Eventually with further temperature increasing the point is reached at which all electrons have enough energy to cross the barrier and thermionic emission process becomes dominant.

\[ \text{Thermionic-field emission} \]
\[ \text{Field emission} \]

**Fig. 3.5** Field and thermionic-field emission under a forward bias. The diagram refers to a degenerately doped semiconductor for which \( \xi \) is negative [34].
3.2.2.2 Reverse biased

Reverse bias increases the barrier to electrons moving from the semiconductor to the metal. This situation is depicted in Fig. 3.6.

According to the thermionic-emission theory, the reverse current density of an ideal Schottky diode should saturate at the value \( J_0 \) (given by Eq. 3.4) because for the electrons in metal there is still the same barrier \( \Phi_0 \) which they have to overcome to enter the semiconductor.

However, it is a universal observation that the reverse current never saturates but increases with increasing voltage. This is partly due to the change of the barrier height by image-force lowering. The effect of the image charge is a dynamic effect reflecting the fact that when an electron passes from the metal to the semiconductor it creates a positive charge (mirror image of electron) in the metal. This results in electrostatic field perpendicular to the surface with maximum effect at the interface. The potential associated with these charges reduces the effective barrier height. This barrier reduction \( \Delta \Phi_{bi} \) is rather small but it leads to a voltage dependence of the reverse current for reverse biases M-S junction. The energy diagram showing image force lowering is shown in Fig. 3.7.

This barrier lowering \( \Delta \Phi_{bi} \) depends on the square root of the maximum electric field at the interface \( E_{\text{max}} \) (where \( \varepsilon_s \) is the permittivity of the semiconductor) and is given by

\[
\Delta \Phi_{bi} = \sqrt{\frac{qE_{\text{max}}}{4\pi\varepsilon_s}}
\]  
(3.6)
When the electric field is small (<2x10^5 V/cm) it is possible to explain reverse characteristics completely in terms of image force lowering. However, at higher fields the barrier lowering necessary to explain the lack of saturation in the reverse direction is considerably greater than that due to image force. This is because tunnelling through the barrier becomes significant at the high electric fields induced when the reverse bias is high or the doping is high. At electric fields (>3x10^5 V/cm) in the reverse direction the potential barrier becomes thin enough for significant tunnelling of electrons from the metal to semiconductor to occur. The effect of tunnelling can be again described as either field or thermionic-field emission as shown in Fig.3.8 but also can be a mixture of both.
The theory regarding thermionic-field emission and field emission was developed by Padovani and Stratton, 1966 [35] and indeed thermionic-field emission dominates over thermionic emission at surface fields > 3x10^5 V/cm for silicon Schottky barriers at room temperature [36].

Detailed calculations of the thermionic-field emission current through a reverse biased triangular Schottky barrier with image force correction, assuming also that the current is limited by the supply of electrons and not the rate at which they diffuse deep into the semiconductor, show that it is a reasonable working approximation to assume that the current increases exponentially with electric field [37, 38]. Making this assumption the current density \( J_s \) becomes

\[
J_s \approx A T^2 \exp \left[ - q \frac{\Phi_s + \alpha E_s}{kT} \right]
\]

(3.7)

Where \( E_s \) is the electric field (negative) at the surface and \( \alpha \) is a tunnelling constant defined as

\[
\alpha = \left( \frac{kT}{q} \right) \frac{\partial \ln J_s}{\partial E_s}
\]

(3.8)

In amorphous materials (such as a-Si:H) the mobility of electrons is low but provided that the electric field \( E_s \) is high enough the drift mobility can be sufficiently large enough to meet the Bethe criterion for thermionic emission. Calculations show that this approximation (Eq.3.7) is reasonable over the field range 3~8x10^5 V/cm with an electron effective mass \( m^* \sim 0.1 \) but for higher fields the current against field curve rolls off and becomes dependent and limited by supply of electrons from the metal. The tunnelling constant \( \alpha \) was found to be \( \sim 3-4 \text{nm} \) [37]. However, when the current through the a-Si:H is high one has to be aware that the magnitude of the current could be affected by space charge or restricted by diffusion of electrons away from the barrier particularly when the applied field is small.

### 3.2.3 Control of Schottky barrier height by ion implantation

It was shown by Shannon [39] that the effective height of the Schottky barrier can be controlled over a wide range using highly doped surface layers. The introduction of donor or acceptor impurities changes the electric field at the interface. If the electric field is very high then carriers are able to tunnel through the potential barrier by thermally assisted tunnelling and in some circumstances by field emission directly between the metal and semiconductor. Therefore the presence of a surface layer containing the donor impurities increases the surface field and reduces the effective barrier height. On the other hand using the acceptor impurities reverses the sign of the surface field and a potential maximum occurs which increases the effective barrier height. Surface layers used to reduce the barrier height must be thin (<15nm) and fully depleted of the free carriers by the built-in potential between the metal and semiconductor.
For barrier lowering using a dose $D$ of impurities the effective barrier height due to implanted field becomes, when using Eq. 3.7

$$\Phi'_B = \Phi_B - \left( \frac{qD\gamma}{\varepsilon_s \varepsilon_0} \right)$$

(3.9)

where $\gamma$ is the fraction of electrically active impurities. Therefore the resulting effective barrier is influenced by two factors a) field due to the implant and b) field due to the applied voltage between the electrodes.

It is predicted that a decrease of the barrier height by ~0.3eV can be achieved using surface layers 10nm thin with metals having a high barrier to n-type silicon without any degradation of reverse characteristics. Chai et al. [40] showed using the same principle (described above) that the effective barrier height of Schottky diodes in a-Si:H can be varied over a wide range. For small changes in the barrier height, damage effects are negligible and dopant activity is high, leading to minimal changes in ideality factor and leakage currents.
3.3 Insulated Gate Field Effect Transistor (IGFET)

All field effect transistors operate in the same way: a gate voltage modulates the conductance of a channel and the current saturates when the drain end is depleted of charge carriers. The gate electrode can form a Schottky contact (in the MESFET’s) or be isolated from the semiconductor as in an insulated gate field effect transistor (IGFET). The most common type is the MOSFET where an oxide insulating layer is used [30, 31, 32].

![Diagram of an n-channel MOS transistor](image)

**Fig. 3.9** An n-channel MOS transistor.

The structure shown in Fig.3.9 has a p-type substrate and an n-type source and drain contact region. With no applied voltage to the gate the two p-n junctions of MOS structure between drain and source prevent current flow in both directions since one or other will be reverse biased and in the blocking state. When a positive voltage is applied to the gate, mobile negative charge is induced in the semiconductor below the oxide-semiconductor interface. The conductance of this induced channel, created between source and drain region, increases with the magnitude of the gate voltage.

For the function of the device the key mechanism is channel formation. For a better explanation of surface space-charge region formation the band diagrams of idealized MOS structures are shown in Fig.3.10 and it is assumed that (1) there is no charge located in the oxide or at the interface between oxide and semiconductor and (2) that the work function difference between metal and semiconductor is zero.

The application of voltage across the MOS structure (capacitor) establishes an electric field $E$ between the plates. As a result, a displacement of mobile charge carriers in the surface region of each plate takes place, giving rise to two space-charge regions. The penetration of the field into the semiconductor produces a potential barrier beneath the surface with the penetration depth
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proportional to the \( N_D^{-1/2} \), where \( N_D \) is the net donor doping concentration. Thus the applied voltage is shared by the voltage drop across the oxide \( V_o \) and surface potential \( \psi_s \).

Depending on the polarity and magnitude of the gate voltage it is possible to realize three different surface conditions (Fig.3.10): (1) carrier accumulation, (2) carrier depletion and (3) carrier inversion [30, 31].

![Energy band diagrams and charge distributions of an ideal MOS structure](image)

Fig. 3.10 Energy band diagrams and charge distributions of an ideal MOS structure

(a) Accumulation. (b) Depletion. (c) Inversion [30].

Carrier accumulation – when a negative voltage is applied to the gate, the bands near the semiconductor surface are bent upward (Fig.3.10a). This causes an increase in the energy difference between intrinsic Fermi level \( E_i \) and Fermi level \( E_i - E_F \), which finally gives rise to an enhanced concentration – an accumulation of holes near the oxide-semiconductor interface. This is called the carrier accumulation and carrier density \( p_p \) is determined by

\[
p_p = n_i e^{(E_i - E_F)/kT}
\]

where \( n_i \) is the intrinsic carrier concentration.
Carrier depletion — when a small positive voltage is applied to the gate, the energy bands bend downward and majority carriers (holes) are depleted. The space charge per unit area $Q_{sc}$, in the semiconductor is given by the charge within the depletion region

$$Q_{sc} = -qN_A W$$  \hspace{1cm} (3.11)

where $W$ is the width of the surface depletion region and $N_A$ density of acceptor impurity.

Carrier inversion — when a large positive voltage is applied to the gate, the bands bend downward even more so that the intrinsic Fermi level $E_i$ at the surface crosses the Fermi level $E_F$ (Fig.3.10c). Then the number of electrons $n_p$ (minority carriers), defined by Eq.3.12, at the surface is greater than the number of holes (majority carriers) — called carrier inversion.

$$n_p = n_i e^{(E_F - E_i)/kT}$$  \hspace{1cm} (3.12)

Once an inversion layer is formed, the surface depletion layer width reaches a maximum. Even if there is a very small increase of band bending it results in a very large increase of inversion layer charge $Q_n$. Since the bands are flat at zero bias the required surface potential for strong inversion is given by

$$\psi_{si} = 2\phi_f$$  \hspace{1cm} (3.13)

where $q\phi_f$ is defined as the difference between $E_i$ and $E_F$ in the bulk of the semiconductor. The gate voltage required to bring an MOS structure to strong inversion is defined as the threshold voltage $V_{TH}$.

$$V_{TH} = -\frac{Q_{sc}}{C_o} + \psi_{si}$$  \hspace{1cm} (3.14)

$C_o$ is defined as oxide capacitance per unit area, where $x_{ox}$ is oxide thickness, $\varepsilon_{ox}$ is oxide permittivity and $\varepsilon_r$ is the permittivity of free space.

$$C_o = \frac{\varepsilon_{ox}\varepsilon_r}{x_{ox}}$$  \hspace{1cm} (3.15)

In the previous part we assumed an idealised MOS structure. In practice the energy bands are not flat when the gate voltage is zero [31, 32]. This is due to work-function difference and charges in the oxide and surface states. Therefore the bands tend to be bent down to accommodate this effect and the metal is positively charged and the semiconductor surface is negatively charged at thermal equilibrium. So as to achieve a flat-band condition we have to apply a negative voltage to the gate called the flat-band voltage $V_{FB}$. Then the new threshold voltage $V_{TH}$ is the sum of (1) flat-band voltage, (2) the voltage to support a depletion region charge $Q_{sc}$ and (3) voltage to produce band bending for strong inversion [14].
3.3.1 I-V transistor characteristics

Let us consider what happens when a voltage is applied to the gate $V_g$, causing inversion at the semiconductor interface. If a small drain voltage is applied, electrons will flow from the source to the drain through the conducting channel. The channel acts as a resistance and the drain current $I_D$ is proportional to the drain voltage $V_D$. This part of the transistor characteristic is called the linear region and drain current in this linear region is defined as

$$I_D = \frac{\mu_s C_0 w}{L} \left[ (V_G - V_{TH})V_D - \frac{V_D^2}{2} \right]$$  \hspace{1cm} (3.17)

where $w$ is channel width, $L$ channel length and $\mu_s$ mobility of electrons [41].

When the drain voltage increases and it reaches a point at which the width of the inversion layer is reduced to zero (normally at drain end of the channel), this point is called the pinch-off point (where $V_D = V_{SAT}$). Beyond the pinch-off point, even if the drain voltage is increased (where $V_D > V_{SAT}$), the drain current remains "the same" (see Fig.3.11). So the carriers arriving (similar to carrier injection) at this point from the source remain the same. The saturation current is defined as

$$I_{SAT} = \frac{\mu_s C_0 w}{2L} V_{SAT}^2$$ \hspace{1cm} (3.18)

where $V_{SAT}$ is the drain-source saturation voltage and defined as

$$V_{SAT} = V_G - V_{TH}$$ \hspace{1cm} (3.19)

so $V_{SAT}$ increases by 1V for every 1V on the gate.

In fact for $V_D > V_{SAT}$ the pinched-off region of the channel becomes wider, spreading out from just a point into a depleted section towards the source. The depleted section is $\Delta L$ and adsorbs the drain voltage that exceeds $V_{SAT}$.

For long channel devices, $\Delta L$ is much smaller than the length of channel $L$, so that a drop of $V_{SAT}$ across $(L - \Delta L)$ results in a small increase in the current. However for modern short-channel transistors, where $\Delta L$ is no longer negligible, increasing $V_D$ beyond the $V_{SAT}$ causes significant increase in drain current. This effect is called channel length modulation and is one of several "short channel effects" (SCE) [31].
If the gate voltage is below $V_{TH}$, there is no conducting channel, and a potential barrier exists between the source and drain that prevents a large current from flowing, even if the voltage is applied between them. In a real device there is a small and undesired 'subthreshold leakage current' flowing between the source and drain even in this case, when the gate voltage is low and the device is in its off-state.

Reducing the channel length $L$ is the best way to raise circuit speed, current and circuit packaging density (ULSI). However, decreasing the $L$ comes to a price that devices are suffering from "short channel effects" [42] and a rapid deterioration of device characteristics. These effects are directly related to $L$ and drain voltage, and are affected directly or indirectly, by the dimensions of the source and drain junctions. The most common SCE are: i) drain induced barrier lowering (DIBL), ii) hot electrons effects and iii) source-to-drain punchthrough breakdown. One way of reducing short channel effects it is to use ion implantation to create ultra shallow junctions and to use low substrate doping [43].
3.4 Thin Film Transistor

Thin film transistors (TFTs) based on a-Si:H were first reported in 1979 [1]. The TFT differs from the IGFET (MOSFET) device (described above) in that it is entirely composed of very thin layers deposited on an insulating substrate, whereas the IGFET is formed by diffusion, deposition or ion implantation on a semiconducting substrate [1, 44]. Another difference is that TFT operates by forming an accumulation layer rather than by forming an inversion layer. The accumulation layer is formed by the metal gate charge attracting majority carriers to the semiconductor-insulator interface. If a sufficient number are attracted to fill up all the traps, the conductance from drain to source will be increased.

![Cross-section of inverted staggered (back channel etched) TFT structure.](image)

Due to the versatility of thin-film technology the design of TFTs can vary. The most common configuration is called an inverted staggered TFT shown in Fig.3.12 where the gate electrode is placed on the glass substrate followed by deposition of the insulating layer (Si$_3$N$_4$), undoped amorphous silicon (a-Si:H) and highly doped n$^+$ amorphous silicon layer. Finally the two ohmic contacts (Drain and Source) are placed on the a-Si:H and the n$^+$ layer etched away between the contacts before passivation. When such a structure is placed on an insulating substrate (such as glass or plastic) there is no need for device self-isolation as required in standard silicon technology.

The transfer characteristics of TFTs shown in Fig.3.13 [45] feature low off-current, threshold voltage (5V), steep sub-threshold slope and wide dynamic range. There is virtually no p-type conduction at negative gate voltage, because of the blocking contact at the source and the low hole mobility of a-Si:H. Two important parameters of TFT's are the carrier mobility $\mu_n$ and the threshold voltage $V_{TH}$. As it can be seen in Fig.3.13 the saturation of drain current occurs when the drain voltage equals $V_G - V_{TH}$. 
3.5 Chapter summary

This chapter deals with basic concepts of common unipolar devices. The simplest unipolar device the Schottky contact was discussed in detail in the context of transport mechanism through forward and reverse biased rectifying M-S junctions because of their great importance in SGT devices. Then we have examined the principle of the insulated gate FET transistor and its characteristics and its nearest relative prepared by thin-film technology used mainly in large area electronics: the TFT. This was necessary in order to understand the differences in device concepts and principles of operation between thin-film SGT and FET devices.
Chapter 4

4 Source-Gated Thin-Film Transistor

4.1 Introduction

The SGT was introduced by Shannon and Gerstner [46]: it forms a new class of unipolar device where current is entirely controlled by the Source. Instead of using the field effect to modulate the channel conductance, the carrier flow is constricted by a source barrier and the electric field induced by the gate is used to change the magnitude of current flowing across the reverse biased source barrier. Furthermore the source barrier is located above or below the gate so that saturation occurs when the semiconductor under the source is depleted of charge. The source is also screened from the drain by the gate electrode.

There has been some interest in Schottky Barrier MOSFET, because the Schottky barrier reduces short channel effects [47] and the device shows some potential for nanoscale high speed devices with very short channel (i.e. less than 20nm) potentially suitable for logic and memory applications [48]. In recent years, some simulations of SB-MOSFET's have been reported [49, 50] which show that saturation of drain current in the low voltage region becomes a problem because most of the drain voltage will be dropped across the source barrier and current will increase strongly with drain voltage. SGT transistors, however, can easily reach the saturation in the low voltage region by using advantages of thin film technology and properties of a-Si:H and locating the gate directly above or below the source Schottky barrier.

4.2 Concept of the Source-Gated Transistor (SGT)

The structure of a SGT is shown in Fig.4.1. As the drain voltage is increased, the space between the source and gate becomes depleted of charge carriers by the reverse biased source barrier (a Schottky barrier in this case). Saturation in the SGT is due to depletion of the source (while in
a conventional FET it is depletion at the drain region). For drain voltages above saturation the source current is determined by the voltage on the gate since this determines the electric field at the source barrier and therefore the current. Furthermore this field is insensitive to any further increase of drain voltage.

![Diagram of SGT structure]

**Fig. 4.1** Schematic pictures showing electrode structure of a SGT with bottom gate and top source barrier opposite to it.

The basic principle and SGT model proposed by Shannon [46, 51] can be better understood from band diagrams through the gate-source region shown in **Fig. 4.2**. In this case the source is a Schottky barrier. When a positive bias is applied to the gate relative to the source, electrons are accumulated at the semiconductor-insulator interface. Concurrently, when a small positive bias is applied to the drain the Schottky barrier will be polarized in the reverse direction and current will flow over the source potential barrier towards the drain.

![Band diagrams for SGT](a) (source) (b) (gate)

**Fig. 4.2** Electron energy bands through the source (a) when a small drain bias is applied and (b) when a drain voltage sufficient to deplete the semiconductor is applied and the current saturates. In both cases, a large gate voltage is applied relative to the source [46].
As the drain voltage $V_D$ is increased more of the a-Si:H becomes depleted by the reverse biased Schottky barrier until the depletion layer reaches the semiconductor-insulator interface. At this moment all the charge carriers are depleted and $V_D = V_{SAT}$. For drain voltage above saturation the source behaves as two dielectrics in series (Fig. 4.2b) and further increase of drain voltage has no effect on the potential at the interface or on the electric field at the source barrier and the current remains at the same saturated level.

The increase of the current is possible only by applying higher voltage on the gate. Any change of gate voltage $AV_G$ relative to the source will change the potential $\psi_S$ at the interface by an amount,

$$\Delta \psi_S = \frac{C_g AV_G}{C_g + C_s} = AV_{SAT}$$

where $C_s$ and $C_g$ are capacitances per unit area of the semiconductor and insulator, respectively.

Since the drain voltage has to be more positive than $\psi_S$ in order to sweep out the electrons under the source we define $V_{SAT}$ as

$$V_{SAT} = \left( \frac{C_g (V_g - V_{TH})}{C_g + C_s} \right) + K$$

where $K$ is voltage required to deplete the semiconductor and charge at the semiconductor-insulator interface (at $V_g = V_{TH}$). As can be seen the change of the saturation voltage with the gate voltage depends on the relative magnitude of the capacitances. If $C_s >> C_g$ then $dV_{SAT}/dV_G$ is $<<1$.

### 4.3 SGT transistor characteristics with Schottky barrier source

Shannon and Gerstner [46] assumed that the current through the reverse biased Schottky barrier under high field ($> 3 \times 10^5$ V/cm) is caused by thermionic-field emission, i.e. tunnelling described in chapter 3. Under high electric field it has been shown [36, 37] that the change of current under reverse bias can be assumed to increase exponentially with electric field. Then the current density through the source barrier becomes

$$J_s = A^* T^2 \exp \left( -\frac{q}{kT} \left( \phi_B - \alpha \left( \frac{C_g (V_g - V_{TH})}{C_g + C_s} + K \right) \frac{C_s}{\varepsilon_S \varepsilon_0} \right) \right)$$

where $\alpha$ is a tunnelling constant [36] given by Eq. 3.8.

As it can be seen $J_s$ strongly depends on the height of the source barrier $\phi_B$. Therefore modifying the barrier height $\phi_B$ it is possible to control the current through the device. Ion implantation is particularly easy to use and shows very good barrier height control [39] (section 3.2.3).
In Fig. 4.3 the measured transistor characteristics of an a-Si:H SGT are shown [46] and compared with those of a FET made with the same layers. It can be seen that the drain current in the SGT saturates more sharply and at much lower drain voltage in comparison with the conventional TFT. The change of saturation voltage is 0.16V per 1V change on the gate in excellent agreement with interface potential calculations using the dielectric model described earlier (Eq.4.1).

![Graphs showing transistor characteristics](image)

**Fig. 4.3** Measured transistor characteristics of (a) SGT and (b) a conventional FET operating at similar current levels. Both had the same semiconductor and insulator layer depositions.

\( \mu = 600 \) microns [46].

### 4.4 Chapter summary

In this chapter the concept and principle of SGT device proposed by Shannon and Gerstner [46] is described and how it differs from standard field-effect transistors. This is followed by experimental SGT device characteristics together with FET characteristics. Clearly it might be seen that the SGT has, in comparison with the FET, a much lower saturation voltage and a higher output impedance.
5 ATLAS simulation package

5.1 Introduction

The ATLAS software, developed by SILVACO International Inc. (USA), provides general capabilities for physically based two-, and three-dimensional simulation of semiconductor devices. ATLAS has a modular architecture that includes several licensable tools and is designed to be used in conjunction with the VWF Interactive tools. The VWF Interactive tools include DECKBUILD (Run time environment), TONYPLOT (Visualisation tool), DEVEDIT (Structure and mesh editor) [52]. The process flow is depicted in Fig.5.1. The device structure is designed in DevEdit and source code is written in DeckBuild where the structure file is included. The simulation is running in ATLAS module. The output the Log and solution files are visualised in the TonyPlot module. The ATLAS developer version v.5.7.28.c and v.5.8.0 were used to perform all simulations in this thesis.

Fig. 5.1 Atlas inputs and outputs [52].
5.2 Principle of ATLAS simulation

ATLAS is a physically-based device simulator. Physically-based device simulators predict the electrical characteristics that are associated with specified physical structures and bias conditions. This is achieved by approximating the operation of a device onto a two or three-dimensional grid, consisting of a number of grid points called nodes. By applying a set of differential equations, derived from Maxwell's laws which are numerically solved, for this grid it is possible to simulate the transport of carriers through a structure. This means that the electrical performance of a device can now be modelled in DC, AC or transient modes of operation.

Physically based simulation provides three major advantages: It is predictive, it provides insight, and it captures theoretical knowledge in a way that makes this knowledge available to non-experts. Physically based simulation is different from empirical modelling. The goal of empirical modelling is to obtain analytic formulae that approximate existing data with good accuracy and minimum complexity. Empirical models provide efficient approximation and interpolation. They do not provide insight, or predictive capabilities, or encapsulation of theoretical knowledge. Physically based simulation is an alternative to experiments as a source of data.

5.2.1 Boundary conditions

ATLAS supports several boundary conditions: ohmic contacts, Schottky contacts, insulated contacts, and Neumann (reflective) boundaries. Voltage boundary conditions are normally specified at contacts, but current boundary conditions can also be specified. Lumped elements can be connected between applied biases and semiconductor device contacts. In simulations presented in this thesis following types of boundaries were used:

**Ohmic Contacts** - are implemented as simple Dirichlet boundary conditions, where surface potential, electron concentration, and hole concentrations \( (\psi_s, n_s, p_s) \) are fixed. Minority and majority carrier quasi-Fermi potentials are equal to the applied bias of the electrode. The potential \( \psi_s \) is fixed at a value that is consistent with space charge neutrality.

**Neumann Boundaries** - Along the outer (non-contact) edges of devices, homogeneous (reflecting) Neumann boundary conditions are imposed so that current only flows out of the device through the contacts. In the absence of surface charge along such edges, the normal electric field component becomes zero. Current is not permitted to flow from the semiconductor into an insulating region except via oxide tunnelling models. At the interface between two different materials, the difference between the normal components of the respective electric displacements must be equal to any surface charge.
**Schottky contacts** - The Schottky contact boundary condition realizes that at the metal semiconductor interface a barrier exists due to the difference in work functions. In the simulation of the Schottky contact a surface potential is applied at this contact that is calculated according to

$$\Psi_s = \text{AFFINITY} + \frac{E_g}{2q} + \frac{kT}{2q} \ln \frac{N_C}{N_V} - \text{WORKFUN} + V_{\text{APPLIED}}$$  \hspace{1cm} (5.1)

where \(\text{AFFINITY}\) is the electron affinity of the semiconductor material, \(E_g\) is the bandgap, \(N_C\) is the conduction band density of states, \(N_V\) is the valence band density of states, \(\text{WORKFUN}\) is the workfunction of metal and \(T\) is the ambient temperature. For example, if one would like to have effective barrier height of 0.6eV then user have to define the metal work function of 4.77eV with the \(\text{CONTACT}\) statement (considering the electron affinity for semiconductor e.g. default silicon value \(\sim 4.17\text{eV}\))

```
CONTACT NAME=ANODE WORKFUN=4.77
```

The ATLAS Schottky model also accounts for a field-dependent barrier-lowering mechanisms. These mechanisms discussed in chapter 3. are caused by image forces and possible static dipole layers at the metal-semiconductor interface. The amount by which this barrier is lowered in the ATLAS simulation becomes

$$\Delta \phi_s = \frac{q}{4\pi\varepsilon_0} E + (\alpha E) E$$  \hspace{1cm} (5.2)

where \(E\) is the magnitude of the electric field at the interface and \(\alpha\) is the linear dipole barrier lowering coefficient. A finite surface recombination velocity can be imposed at a contact by specifying the parameter \(\text{SURF.REC}\) on the \(\text{CONTACT}\) statement.

Further it is important to define the mesh for the simulation. In other words defining the number and density of simulation points. In the case of the Schottky barrier the most critical part is the region under the Schottky contact for the depletion region calculation. Fermi-Dirac statistics and SRH models were chosen to resolve carrier concentration statistics and thermal recombination and generation respectively [52]. The example of the ATLAS source code is found in the Appendix.

### 5.3 Simulations of a-Si:H

ATLAS - TFT module enables the user to define an energy distribution of defect states in the band gap of semiconductor materials. This is necessary for the accurate treatment of the electrical properties of such materials as polysilicon and amorphous silicon. Disordered materials contain a large number of defect states within the band gap of the material. In order to accurately model
devices made of polycrystalline or amorphous materials it is necessary to use a continuous density of states.

Firstly the material is defined as crystalline silicon and then the DEFECT statement is used to enable the TFT module and specify the density of defect states (DOS) as a combination of exponentially decaying band tail states and Gaussian distributions of midgap states.

In that statement, parameters ending in 'a' are for acceptor-like states and those ending 'd' are for donor-like states, while 'e' and 'h' are designated for electrons and holes respectively. The following statements define material properties and density of states of a-Si:H schematically shown in Fig. 5.2.

```
MATERIAL material=silicon mun=15 mup=0.5 nc300=2.5e20 \\
    nv300=2.5e20 eg300=1.8 taun0=1e-8 taup0=1e-8

DEFECT continuous nta=1.12e21 ndt=4.e20 wta=0.025 wtd=0.05 \\
    nga=1.0e16 ngd=1.0e16 ega=0.4 egd=0.4 wga=0.1 wgd=0.1 \\
    sigtae=1.e-16 sigtah=1.e-14 sigtdc=1.e-14 sigtdh=1.e-16 \\
    siggae=1.e-16 siggah=1.e-14 siggde=1.e-14 siggdh=1.e-16
```

![Distribution of DOS for a-Si:H in the ATLAS.](image)

For an exponential tail distribution, the DOS is described by its conduction and valence band edge intercept densities (NTA and NTD), and by its characteristic decay energy (WTA and WTD). For Gaussian distributions, the DOS is described by its total density of states (NGA and NGD), its characteristic decay energy (WGA and WGD) as well as its energy/peak distribution (EGA and EGD) [27]. The syntax SIGxyz are the capture cross sections for different distributions.
be either $t$ for the tail or $g$ for the Gaussian states respectively. The $y$ can by either $a$ or $d$ for acceptor or donor states. Finally, $z$ can by either $e$ or $h$ for electrons and holes respectively.

5.4 Simulation of reverse biased Schottky barrier

The mobility of electrons is low in amorphous materials but provided the electric field is high enough the drift mobility can be sufficiently large to meet the criterion for thermionic emission. In a-Si:H this condition is reached for electric fields $>2\times10^5$ Vcm$^{-1}$. Moreover these simulations under high electric field are particularly of importance for the operation of a Source-Gated Transistor and its reverse polarized source barrier (Schottky contact). Under high reverse biased conditions the electrons cross the barrier by tunnelling (described in chapter 3.) and the current is given approximately by Eq.3.7.

Electron tunneling through the barrier can be taken into account by specifying the ATLAS parameter $E.TUNNEL$ and the relative effective mass for electrons ($ME.TUNNEL$) on the CONTACT statement. However as can be seen in Fig. 5.3 the current version 5.8.1.R of ATLAS (after several updates in 2003 and 2004) is unable to simulate correctly the Schottky barrier under high electric field for different effective mass. Whenever the parameter $ME.TUNNEL$ is changed the reverse current remains at the same value. What we expected is illustrated in figure (Fig.5.4) where the variation of reverse current due to change of effective mass can be clearly seen [37].

![Fig. 5.3 Simulation of current for reverse biased a-Si:H SBD against electric field for different values of relative effective mass (parameter ME.TUNNEL).](image-url)
Therefore we can conclude that present ATLAS model for tunneling current is very poor (i.e. it does not work). The proper model needs to include the field dependence of thermionic-field emission plus the image charge correction. However it is found that we have been very fortunate because the approximation for the current (considering thermionic-field emission) under large electric field (exponential term in Eq.3.7) is similar to the expression using the linear dipole lowering (Eq.5.2) in ATLAS. In another words mathematically these expressions for the barrier lowering $\Delta \Phi_b$ are the same even though the $\alpha$ stands for a tunnelling constant in Eq.3.7 and $\text{ALPHA}$ is a linear dipole lowering coefficient in ATLAS. Therefore the change of current and effective barrier height with the change of electric field can be simulated using the dipole expression when substituting the tunnelling constant (of 4 nm) in place of dipole coefficient ($\text{ALPHA}$).

5.5 Modelling of the SGT with Schottky barrier sources

The modelling of the SGT devices is very similar to modelling of inverted staggered thin-film FET’s. The major difference is that here instead of the ohmic source contact (for the TFT) the source barrier in the SGT is a reverse biased Schottky barrier having a barrier lowering mechanism described above and given by Eq.5.2. There is also a difference in geometry of the
devices. The length of the source barrier of the SGT can vary from 0.25um to 10um and it is longer than the gate-source overlap was used for the simulation of a TFT (0.25um). On the other hand no gate-drain overlap used in all SGT simulations. Detailed discussion regarding the geometry of SGT devices can be found in sections 6.4 and 7.3 (Fig. 6.4 and Fig. 7.6).

Throughout this thesis we are concerned with the simplest barrier, naturally formed at the M-S interface; the Schottky barrier. In fabricated SGT devices the source barrier height was modified using a phosphorus implantation to increase the surface field and raise the source current by thermionic-field emission (described in Section 3.2.3). However in the modelling an effective Schottky barrier height (reflecting the implanted dose) was used directly to specify the barrier height (by changing the metal-work function in the model). Then the surface electric field was simply that induced by the gate. In this simulation the field was low (or moderate) and the barrier changes were due to image-force corrections and dipole lowering with a distance corresponding to the tunnelling constant as described above. This situation is depicted in figure (5.5) where the current density of the reverse polarised Schottky barrier is plotted as a function of electric field.

**Fig.5.5** Current density of the reverse polarised Schottky barrier plotted as a function of electric field for a barrier $\Phi_b = 0.85$eV. The calculated results are shown together with the exponential and ATLAS approximation. The ATLAS approximation is presented for two barrier heights.

Here the calculated current density for $\alpha = 4$nm, $m^* = 0.1$, $\Phi_b = 0.85$eV (red curve; taken from Ref. [37]) and its exponential approximation (blue curve; given by Eq.3.7) is shown. It is seen that this approximation works only for certain range of the electric field ($3-8 \times 10^5$ V/cm). For higher
fields the estimation of the current density using this exponential approximation is not very accurate. The green line stands for the ATLAS model approximation where is no built-in field due to implant \(E_{\text{built-in}}\) and the resulting effective barrier height due to the implant built-in field is substituted in the ATLAS simulations. Therefore the green line starts off with a higher current density due to the lower effective barrier height when accounting for the barrier lowering implant. The electric field, in this case is just the applied field, induced by the gate electrode. The estimation of the effective barrier height due to the implant is described in chapter 8. Two effective barrier heights are shown in Fig.5.5 representing two different doses of implanted phosphorus doses.

### 5.6 Chapter summary

In this chapter the modular concept of the ATLAS simulation package is briefly described as well as the principle of ATLAS device simulator based on numerically solving the differential equations, based on Maxwell's laws and approximating the operation of a device onto a two or three-dimensional grid. The description of how ATLAS handles the boundary conditions for different situation is given as well as introduction into the TFT module which handles the simulations of amorphous and polycrystalline materials.

The problems of the ATLAS model for tunnelling current are briefly addressed in particular the inability of the model to simulate the reverse polarised Schottky barrier for different effective masses. Thus the SILVACO support was contacted (April '03) and they acknowledged that the present model underestimates the current through the reverse bias Schottky contact under high electric field. Since this acknowledgement other model updates (during 2003 and 2004) were developed, however without significant difference.

Fortunately by specifying the value of the effective barrier height (reflecting the modified height due to the implant) directly in to ATLAS model showed good results because the expressions for the field dependence of barrier lowering for thermionic-field emission and linear dipole lowering are similar. Fortunately the linear dipole lowering correction in ATLAS does work, so we can simulate the reverse biased Schottky by changing the barrier height and using the dipole expression with a tunnelling constant substituted for dipole length and low fields. In this case the electric field is just that induced by the gate.
Chapter 6

6 SGT with Schottky barrier source

6.1 Introduction

As described in section 4.2 the basic SGT structure has a potential barrier at the source that restricts the current in the on-state. The barrier could comprise any form of unipolar junction as long as the semiconductor layer can be depleted under a reverse bias. The simplest source barrier is the metal-semiconductor Schottky barrier. In this chapter we are concerned with SGT's having a Schottky barrier source. Furthermore the conductance of the extrinsic drain region is modulated by extending the gate under the region between the source and drain. This extrinsic drain region forms a parasitic FET in series with the source barrier and controls the off-state of the SGT. Because the resistivity of a-Si:H is very high the extrinsic drain resistance would be very high without the parasitic FET.

6.2 Device preparation and Technology

The SGT samples were prepared in PHILIPS Research laboratories, Redhill, UK. Transistors were made in a-Si:H using a 4 mask process with thin-film technology and low temperature processes compatible with these commercially used by the display industry. Firstly a chromium gate was deposited on glass and photolithographically defined, followed by deposition of 300nm (or 150nm) silicon nitride and 100nm of undoped a-Si:H using PECVD at 250°C. The a-Si:H was then dry-etched to leave islands on the nitride and contact holes to the gate pads were opened in the nitride. Implantation of 10keV phosphorus was used as a barrier modification before the drain and source Schottky contacts were deposited and defined [39]. Next the second BF$_2$ ion implantation of 12 or 13keV was used for compensation of donors in the extrinsic drain region [53]. Following the BF$_2$ implantation the samples were annealed at 250°C for 30min in nitrogen. This annealing technique seems to give the best results as a trade-off between the electrical activity of the implant and defect
Chapter 6. SGT with Schottky barrier source

concentration in a-Si:H grown at 250°C [40]. The final structure is schematically shown in cross section in Fig.6.1.

![Cross section of a SGT device with Schottky source and drain](image)

**Fig. 6.1 Cross section of a SGT device with Schottky source and drain**

A photograph of a transistor is shown in Fig.6.2. The gate is on the bottom of the structure. The source and drain contact are placed on the top of the a-Si:H island and separation between the source and drain \((d)\) is ~2 microns. The width of the device is ~12 microns and length of the source that overlaps the gate \((s)\) is ~9 microns. The mask set contains a range of different structures with various \(s, d, w\) values.

![Top-view of SGT layout](image)

**Fig. 6.2 Top-view of SGT layout.**

### 6.3 SGT transistor characteristics

Indeed as described by Shannon and Gerstner [46] the most striking and obvious features of SGT transistors are a low saturation voltage and a high output impedance. In Fig.6.3 one of the first experimentally measured transistor (output) and transfer characteristics is shown. The source
barrier has been modified using the $5 \times 10^{13}$ cm$^{-2}$ 10keV P$^{31}$. The width of the device is ~18 microns, length of the source $s = 5$ microns and source-drain separation $d \sim 3$ microns. The SGT output characteristics (Fig. 6.3a) shows a sharp increase of the current with drain voltage and a low saturation voltage $V_{\text{sat}} \sim 1$V at $V_G = 10$V which is much smaller than found in a conventional FET. For a FET this compared to $V_{\text{sat}} \approx 7$V ($V_G - V_{TM}$). Furthermore the current after saturation is flat giving the SGT device a very high output impedance which is very important for many applications. The SGT's can therefore be operated in saturation at much lower drain voltages and with smaller power dissipation than a conventional FET. The saturated current of this “low current” device is quite small and in the range nA because the dose of the barrier modification implant was quite small and the source barrier is still high. The on-off ratio is only 4 orders of magnitude high. It can be seen that low leakage current is possible to achieve using compensation technology. The $V_{TM}$ of the parasitic FET estimated from the transfer characteristics ($V_D$ vs. $V_G$) at low gate voltages was ~3V and the subthreshold slope ~1V/dec.

![Fig. 6.3 Low current SGT device a) output and b) transfer characteristics.](image)

### 6.4 Simulated IV characteristics

With achieving first experimental results there was a strong need for simulation of the SGT devices to obtain a closer understanding and providing deeper insight into the device physics as well as to support the claims expressed in Ref. [46] regarding the SGT device concept. Therefore simulations were started using SILVACO Atlas (described in chapter 4.).

Structures similar to that shown in Fig.6.4 were defined in Devedit. The simulated structure consists of three contacts where gate and drain were defined as ohmic and the source as a Schottky barrier contact. The $n^+$ doped drain region is used in order to ensure that the drain metalization creates good ohmic contact to undoped $a$-Si:H. The thickness of silicon nitride (SiN) and amorphous silicon (a-Si:H) is defined as $t_{SiN}$ and $t_{aSi}$ respectively. Other important parameters of
the SGT device are length of the source barrier \( s \) and source-drain separation \( d \) also shown in Fig.6.4.

![Diagram of SGT structure](image)

**Fig. 6.4** Schematic drawing of a SGT structure used in simulations showing the spreading of the reverse biased source barrier depletion region towards the semiconductor-insulator interface.

Modeling of the SGT was done using the developer version of the Silvaco ATLAS v.5.7.28.C and v.5.8.1.R programme with the latest implementation of the model for the barrier tunnelling and lowering mechanism [52, 54]. As described in section 5.5 an effective Schottky barrier height was used and the electric field was simply that induced by the gate with no built-in field due to the implant. In this simulation the field was low and the barrier changes were due to image-force corrections and dipole lowering with a distance corresponding to the tunnelling constant.

The main parameters are specified in Table 6.1. \( \Phi_{bi} \) is the effective barrier height and \( \alpha \) the dipole barrier lowering coefficient. It is assumed that the total density of states in amorphous silicon (10% hydrogen content) is composed of four bands: two exponential tail bands (a donor-like valence band \( (N_{tail}^{D}) \) and an acceptor-like conduction band \( (N_{tail}^{A}) \)) and two deep level defect bands (one acceptor-like \( (N_{deep}^{A}) \) and the other donor-like \( (N_{deep}^{D}) \)), which are modeled using a Gaussian distribution (shown graphically also in Fig.5.2). The values for these concentrations and corresponding decay constants \( E_{x}^{X} \) are summarized in Table 6.1 [2, 3, 55]. Mobility in extended states, which is different from field-effect mobility, for electrons and holes was taken from references [2, 3]. Next the values for a-Si:H bandgap \( E_{g}^{a-Si} \) and dielectric constant \( \varepsilon_{a-Si}^{o} \) are also shown in Table 6.1. For the rest of the amorphous silicon parameters (such as surface recombination velocity, electron affinity, effective density of states) the ATLAS default values were used [52]. In the case of the silicon nitride insulating layer all values were default values apart from dielectric constant of \( \varepsilon_{SN}^{o} \). The simulation deck (source code) is shown in the Appendix.
Table 6.1 Parameters used in the simulations.

<table>
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<th>Parameter</th>
<th>Value</th>
<th>Unit</th>
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<td>$\alpha$</td>
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<td>nm</td>
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<td>$\text{cm}^{-2}(\text{eV})^{-1}$</td>
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<td>eV</td>
</tr>
<tr>
<td>$N^D_{Deep}$</td>
<td>$1 \times 10^{16}$</td>
<td>$\text{cm}^{-3}(\text{eV})^{-1}$</td>
</tr>
<tr>
<td>$E^D_{Deep}$</td>
<td>0.1</td>
<td>eV</td>
</tr>
<tr>
<td>$\mu_e$</td>
<td>15</td>
<td>$\text{cm}^2/V\cdot\text{s}$</td>
</tr>
<tr>
<td>$\mu_h$</td>
<td>0.5</td>
<td>$\text{cm}^2/V\cdot\text{s}$</td>
</tr>
<tr>
<td>$E_g^{a-Si}$</td>
<td>1.8</td>
<td>eV</td>
</tr>
<tr>
<td>$\varepsilon^{a-Si}$</td>
<td>11.7</td>
<td>-</td>
</tr>
<tr>
<td>$\varepsilon^{SiN}$</td>
<td>6.5</td>
<td>-</td>
</tr>
</tbody>
</table>

The experimental transistor characteristics of an SGT are shown in Fig. 6.5. The thickness of a-S:H and silicon nitride was 100nm and 300nm respectively. The length of the source $s$ was estimated to be 4 um, width ($w$) of the device 12um and source-drain separation 2um. A chromium Schottky barrier modified using ion implantation (phosphorous 10keV, $1 \times 10^{14}$ cm$^{-2}$) was used for the source barrier and a compensating implant BF$_2$ (13keV, $5 \times 10^{13}$ cm$^{-2}$) was used to passivate and provide field relief at the edge of the source barrier. Assuming uniform emission over the area of the source barrier, the current density and the effective barrier height, $\Phi_B$ of the source was determined from the measured transistor characteristics using the SGT model developed by Shannon [51]. The procedure of barrier height determination from transistor characteristics and barrier analysis is described in detail in chapter 8. The effective barrier height of 0.57eV determined from these experimental characteristics was used as input data for the simulations. The simulated and experimentally measured SGT transistor characteristics are shown in Fig.6.5. The characteristics were normalised per one micron device width. It also should be noted that all simulations done by ATLAS are for unity device width of 1micron and therefore for the comparison, all the experimental results had to be normalised over device width.
The magnitude and shape of the characteristics for simulated and experimental transistor characteristics per unit width are found to be in good agreement (Fig.6.5) particularly in view of the sensitivity of the current to the electric field at the source. There is excellent correspondence in the shape of the characteristics and the saturation voltage. The discrepancy between the simulated and experimental results for the magnitude of the current could arise from an error in estimation in barrier height from the transistor characteristics (the estimate used for current vs electric field). Also another discrepancy could arise from differences between real and estimated dimensions in source length and device width because the current is dependent mainly on barrier height and area of the source. So after this consideration the achieved results are remarkably good and it was possible to carry on with further analysis of the SGT device.

Fig.6.6 shows Atlas simulations of the concentration of electrons under the source (in 2D-perspective) and at the interface between the a-Si:H and SiN. The simulated structure is described on the side of Fig.6.6 for each sub-picture. Each sub-picture shows the source edge, 60nm thick a-Si:H and S-I interface. The color scale of density of electrons [1/cm²] and its corresponding order of magnitude is shown in the legend (Fig.6.6). All sub-pictures have the same barrier height (0.6eV).

With positive voltage on the gate (15V in this case) and zero drain voltage, negative charge is accumulated at the S-I interface (Fig.6.6a). Also the space charge region is visible underneath the source barrier. As the drain voltage is increased in the positive direction (1V) the depletion region under the reverse biased source spreads towards the S-I interface (Fig.6.6b). Further increase in the drain voltage (above 2V) causes the depletion region to reach the S-I interface and pinch-off the channel in the SGT device under the source (exactly under the source edge (Fig.6.6c). At this drain voltage, $V_D = V_{Sat}$ (saturation voltage), and the current saturates.
Fig. 6.6 Simulations of density of electrons in SGT transistor underneath source barrier for different $V_D$. 
Another increase of the drain voltage (i.e. 10V) leads to an extension of depletion region towards the drain (Fig.6.6d), however there is no further increase of current because the electric field at the Schottky barrier is screened from the drain field by the gate located opposite the depleted source. There is therefore very little penetration of the drain field (see section 6.7). In this situation where the source is depleted and the current is saturated, the surface field and the magnitude of the current is controlled by the gate.

Indeed these modelling results supports claims about the SGT device concept expressed by Shannon [46] that saturation occurs when the semiconductor beneath the source barrier is depleted of carriers. Also the approximation, known as the dielectric model [51], that in saturation the semiconductor and insulator behave as two dielectrics in series is correct (predominantly at the edge of the source barrier).

6.5 SGT device current and barrier height

As stated above the height of the source barrier is the main constricting factor for the current through the SGT device. Fig.6.7 shows simulated transistor characteristics of the SGT for four different barrier heights of 0.6eV, 0.5eV, 0.4eV and 0.3eV. Device geometry is exactly the same as in the previous section with 60nm of a-Si:H and 300nm of SiN. The length of the source is 4um and s-d separation is 1um. This device is considered as a short channel device. The shape of the SGT transistor characteristics for barrier 0.6eV and 0.5eV looks rather similar only one change is obvious - the current level. It can be seen that with decreasing of the barrier height the drain current level is increased because more electrons can cross the barrier (reverse biased Schottky contact) and raise the source current by thermionic-field emission (i.e. mathematically expressed by Eq.4.3). The saturation voltage is almost the same in both cases and well defined e.g. for $V_g = 20V$ it is less than 2V. The change of saturation voltage is 0.1V per 1V change on the gate, which is 10 times less than that for a FET.

A further decrease of the barrier height to 0.4eV leads to a further increase of the drain-source current (Fig.6.7c). Here it can be seen that a slight deterioration of the device properties occurs but the SGT features are still well preserved. The saturation voltage is shifted up to 2.5V and is less well defined in comparison with the previous two cases. $V_{sat}$ is increased due to the fact that there is now a much higher electron accumulation and additional drain voltage is necessary to deplete this excess of carriers in comparison with 0.6eV and 0.5eV barrier heights. Decreasing the barrier further to 0.3eV the SGT starts to behave as a FET. This is because the source barrier is not high enough to restrict current flow which is now becoming limited by the parasitic FET in series with the source. The saturation voltage is shifted to the higher values characteristic of a FET and there is a deterioration of the output characteristics (Fig.6.7d). The situation is more complicated by the fact
that the device has very short s-d separation (of 1 μm) and there are short channel effects such as channel length modulation.

(a) 

\[ V_g = 20V \]
\[ \Phi_s = 0.6eV \]
\[ V_D = 0.6eV \]
\[ q = 8x10^{-5} \]
\[ t = 3.5x10^{-5} \]
\[ \alpha = 2.5x10^{-2} \]
\[ \rho = 1.5x10^{-2} \]
\[ \sigma = 1.0x10^{-2} \]
\[ \theta = 5x10^{-2} \]

(b) 

\[ V_g = 20V \]
\[ \Phi_s = 0.5eV \]
\[ V_D = 0.5eV \]
\[ q = 8x10^{-5} \]
\[ t = 3.5x10^{-5} \]
\[ \alpha = 2.5x10^{-2} \]
\[ \rho = 1.5x10^{-2} \]
\[ \sigma = 1.0x10^{-2} \]
\[ \theta = 5x10^{-2} \]

(c) 

\[ V_g = 20V \]
\[ \Phi_s = 0.4eV \]
\[ V_D = 0.4eV \]
\[ q = 8x10^{-5} \]
\[ t = 3.5x10^{-5} \]
\[ \alpha = 2.5x10^{-2} \]
\[ \rho = 1.5x10^{-2} \]
\[ \sigma = 1.0x10^{-2} \]
\[ \theta = 5x10^{-2} \]

(d) 

\[ V_g = 20V \]
\[ \Phi_s = 0.3eV \]
\[ V_D = 0.3eV \]
\[ q = 8x10^{-5} \]
\[ t = 3.5x10^{-5} \]
\[ \alpha = 2.5x10^{-2} \]
\[ \rho = 1.5x10^{-2} \]
\[ \sigma = 1.0x10^{-2} \]
\[ \theta = 5x10^{-2} \]

Fig. 6.7 SGT transistor characteristics for (a) 0.6eV, (b) 0.5eV, (c) 0.4eV and (d) 0.3eV barrier height.

Atlas simulations of the concentration of electrons under the source in a-Si:H (in 2D-perspective) and at the S-I interface for four different barrier heights of 0.6eV, 0.5eV, 0.4eV and 0.3eV and the same SGT device geometry (corresponding to Fig. 6.7) are shown in Fig. 6.8. The applied drain and gate voltage is 10V and 15V respectively. Here it is shown how the barrier height influences the charge under the source and how the charge builds up at the S-I interface as the barrier height is reduced. In the case of barrier height 0.3eV even for the large drain voltages it is not possible to deplete the region under the source barrier and reach saturation.
Chapter 6. SGT with Schottky barrier source

(a) $\phi_B = 0.6\text{eV}$  
(b) $\phi_B = 0.5\text{eV}$

(c) $\phi_B = 0.4\text{eV}$  
(d) $\phi_B = 0.3\text{eV}$

Fig. 6.8 Simulations showing density of electrons in SGT transistors having different barrier heights.

As previously mentioned the source Schottky barrier height was modified using a phosphorus implantation to increase the surface field (implant depth was very shallow 10-15nm) and increase the current by thermionic-field emission. SGT transistor characteristics with 1x, 2x, 3x and 4x$10^{14}$ phosphorus cm$^{-2}$ are shown in Fig.6.9. With increasing dose the effective Schottky source barrier decreases due to increase in electric field, which increases the tunnelling probability for electrons. The device width and s-d separation was 12 and 2 microns respectively for all devices ($t_{SN} = 300\text{nm}$, $t_{SG} = 100\text{nm}$). When source barriers are high and currents are low the transistor characteristics show strong saturation with high output impedance (Fig.6.9a). The $V_{SAT}$ at $V_{DG} = 10\text{V}$ is only $1.8\text{V}$ for the lowest doses (1x and 2x$10^{14}$ cm$^{-2}$). With further increasing dose the current level increases together with $V_{SAT}$. For doses of 3x and 4x$10^{14}$ cm$^{-2}$ the $V_{SAT}$ is ~2V and ~2.2V respectively. Furthermore the I-V curves around saturation are more rounded and less well defined. This feature was also observed in the simulated results (see Fig.6.7) and explained on the basis of the increased electron concentration at the S-I interface and the need for higher drain voltage to deplete the region underneath the source barrier.
Chapter 6. SGT with Schottky barrier source

Fig. 6.9 Experimental SGT transistor characteristics with (a) 1 (b) 2 (c) 3 and (d) 4x10^14 phosphorus cm^-2. The w = 12um and d = 2 um for all devices (t_{SiN}=300nm, t_{Si}=100nm).

It can be seen (Fig.6.10) that the SGT can be operated over a wide range of currents by controlling the source barrier height using ion implantation. In Fig.6.10 the saturated drain current is plotted as a function of ion dose for different gate voltages.

Fig. 6.10 Saturated drain current plotted as a function of implant dose for different gate voltages.
Furthermore this figure shows how the gate voltage controls the current by affecting the electric field at the source barrier. The barrier is pulled down by the field induced by the gate and the drain current is increased (weak exponential function) due to higher emission and tunnelling of electrons through the barrier. Then total electric field at the barrier is a sum of the field due to the implant and the applied field induced by the gate electrode.

In Fig. 6.11 comparison between the simulated and an experimental SGT transistor characteristic normalised for the width of 12 microns is shown. The width, s-d separation and source length ($s$) of the SGT device was 12um, 2um and 5um respectively. The estimated barrier height obtained from experiment was 0.54eV (more details regarding this estimation are given in chapter 8.) for a dose of $2 \times 10^{14}$ cm$^2$. This was used in the simulation. The agreement between the experiment and simulation is remarkably good.

![Fig. 6.11 Comparison between a simulated and an experimental SGT transistor characteristic for a width of 12 microns.](image)

The comparison between the simulated and experimental results of saturated drain current obtained at $V_g = 10$V (and normalised for the width of 12 microns) is shown in Fig. 6.12 for different implant doses. Note that x axis is valid just for experimental results because the simulations used the effective barrier height to substitute the effect of the implant field (reason was discussed in section 5.5). It is seen that there is again good agreement between simulated and experimental results.
### 6.6 Saturation voltage of SGT devices

As shown in the previous section 6.5 the saturation voltage of SGT's is much smaller than in conventional FET devices. Simulation of the saturation voltage and its dependence on the gate voltage for different s-d separation \(d\) is shown in Fig.6.13a. It is seen that for small \(d\) when there is no constriction of the current the slope of the curve is given very well by the dielectric model [51] where the semiconductor is assumed to be depleted of charge at saturation and the slope \(dV_{\text{SAT}}/dV_G\) is \(C_G/C_S + C_G\) where \(C_S\) and \(C_G\) are the semiconductor and insulator capacitances per unit area. For the structure shown in Fig.6.4 \((t_{aSi} = 300 \text{ nm} \text{ and } t_{aSi} = 100 \text{ nm})\) this calculated value is 0.155.

![Graph showing simulated and experimental results of saturated drain current](image)

**Fig. 6.12** Comparison between the simulated and experimental results of saturated drain current obtained at \(V_G = 10\text{V}\) and normalised for the width of 12 microns.

![Graph showing dependence of saturation voltage on gate source voltage](image)

**Fig. 6.13** Dependence of saturation voltage on gate source voltage for various source-drain separations \(d\) a) modelled and b) measured.
As the gate voltage increases the saturation voltage increases because electron accumulation at the S-I interface is higher and additional voltage (electric field) is necessary to deplete the region underneath the source barrier. As the s-d separation increases (looking at the same $V_G$, e.g. 10V) the $V_{Sat}$ also increases because there is more potential drop across the parasitic FET. It is seen that the change of saturation voltage with gate voltage can be ten times lower than a conventional FET. Similar trends are seen in the experimental results shown in Fig.6.13b and shows that the ATLAS model is able to predict the saturation voltage for a given geometry.

Furthermore, according to Eq.5.2 the saturation voltage of the SGT is defined as $V_{Sat} = C_G (V_G - V_{th})/(C_G + C_J) + K$ where $K$ is the additional voltage needed to deplete the semiconductor under the barrier at S-I interface. Therefore if we plot the saturation voltage as a function of $V_G - V_{th}$ then the slope of the curve gives us the change of $V_{Sat}$ with $V_G$ (because $V_{th}$ is constant and independent from $V_G$) and the intersection of the fitted curve with the y-axis gives a value of $K$. The estimation of $K$ is shown in Fig.6.14 where $V_{Sat}$ is plotted against $V_G - V_{th}$ for different doses used for barrier modification (corresponding to measured SGT transistor characteristics shown in Fig.6.9).

![Fig. 6.14 Plot of the saturation voltage as a function $V_G - V_{th}$ for $d = 2\mu m$.](image)

The slope of the curves is in good agreement with theoretical value (0.16) for $t_{SiN} = 300 \text{ nm}$ and $t_{Si} = 100 \text{ nm}$ and is varying from 0.15 (corresponding to dose $1\times10^{14} \text{ cm}^{-2}$) to 0.21 for the highest dose. The value of $K$ for the lowest dose is almost zero so no additional voltage is necessary for depletion of source region. However, for the higher doses $K$ is no longer zero and increases to 0.1V, 0.2V and 0.5V for doses 2x, 3x and $4\times10^{14} \text{ cm}^{-2}$ respectively.
6.7 Output impedance

The output impedance, source impedance, or internal impedance of an electronic device is the opposition exhibited by its output terminals to the flow of an alternating current (AC) of a particular frequency as a result of resistance, inductance and capacitance. The impedance at DC is the same as the resistive component of the impedance.

Ideally field-effect transistors have a voltage controlled current source with infinite output impedance. This rough approximation is more valid for long channel devices (L>10um) but this is very far from true for modern short channel devices where channel modulation and short channel effects are present. There are ways to reduce the short channel effects using ion implantation but this feature of FET devices remains a problem.

It is found that SGT devices have much higher output impedance than conventional FET devices using the same layer thickness and dimensions and this is even more obvious for very short channels. The measured values of DC output impedance obtained from transistor characteristics at $V_g = 10V$ ($d = 2\mu m$ and $w = 12\mu m$) are shown in Fig.6.15.

![Fig. 6.15 Experimental values of DC output impedance for FET and SGT devices ($V_g = 10V$).](image)

It can be seen that with increasing dose of barrier modification implant the output impedance decreases. In the linear region of the SGT the output impedance is lower than in the saturation region by up to 2 orders of magnitude. For low doses there is a sharp transition between linear and saturation region because the $V_{sat}$ is better defined for low current devices. At similar saturated current levels in the FET (SG32-T26 L~10um) and SGT (doses 4x and 5x$10^{14}$cm$^2$) the output impedance of the SGT is approximately a factor of 10 higher. There is a change in the output impedance (the slope of the curve in saturation region) for the dose of 5x$10^{14}$cm$^2$ towards higher $V_d$ this is due to higher leakage current (similar to that shown in Fig.12.3).
The reason why SGT devices have such high output impedance is due to their geometry and fact that the gate electrode is directly located below (or could be above) the source barrier. For large drain voltages the gate electrode acts as a screening shield preventing the penetration of drain field into the source region. The most crucial region is the edge of the source barrier where the effect of drain field might be most obvious. Simulations shown in Fig.6.16 indicate that indeed there is very little drain field penetrating into the source region.

![Fig. 6.16 Simulation of electric field distribution a) x-axis and b) y-axis taken along the a-Si:H 1nm underneath the source barrier. Source length and s-d separation was 4 and 1micron respectively.](image)

The electric field (in 2D simulation) has two components x (Fig.6.16a) and y (Fig.6.16b). It is seen that (for barrier 0.4eV, s = 4um and d = 1um) the drain field penetrates a very small distance into the source area and peaks at the edge of the source. The edge of the source is at a distance of 4um from the origin and the drain contact is at 5um. The screening factor of the gate may be seen for x < 4um (Fig.6.16a) where there is very little electric field in the x direction due to the drain field but the field induced by the gate is significant in the y-direction (Fig.6.16b). The y component of the electric field is the most important for the SGT and its operation. For low drain voltages (<1V) the y-component is quite uniform along the source. However for higher $V_D$ (e.g. 2.5V) the y-component peaks at the edge (x = 4um) and is responsible for depletion of the source (underneath the source edge). Further increase of $V_D$ (to 15V) increases the electric field only marginally (by a factor of 1.5) over a very small region (~0.1um) under the source region.
6.8 Chapter summary

In this chapter the general features of SGT devices having Schottky barrier sources are described as well as device preparation and technology. It was shown that the concept of how the SGT works suggested by Shannon and Gerstner [46] is valid and SGT device behaves entirely differently from its nearest relative - the FET. A more detailed description of the principles of SGT operation is given and supported by 2D simulation of electron concentration beneath the source barrier. Good agreement between the experiment and simulation of SGT characteristics was presented allowing us to use the ATLAS Silvaco model to predict device behaviour for various device geometries. However it is worth noting that for lower barriers the current through the source barrier is underestimated which means that in reality one should be able get higher current from SGT devices than those predicted by simulations. It was shown that indeed the current depends on effective barrier height and it is constricted at the source.

The most striking features of SGT were discussed – the very low saturation voltage and high output impedance. Both these features arise from the different device geometry and the reverse biased source barrier. The saturation voltage can be very much smaller than that of a FET when the semiconductor layer is thin and lightly doped. The output impedance depends on how well the source can be screened from the drain field. If the penetration of the drain field is small then devices have excellent output characteristics. It was shown that for the similar saturated current levels in the FET and SGT the output impedance of the SGT is approximately a factor of 10 higher.
Chapter 7

7 Dependence of SGT characteristics on device geometry

7.1 Introduction

Since the on-characteristics of the SGT are controlled by the effect of the gate on the source barrier we expect the on-current to be independent of the separation between the source and drain contacts \( d \) Fig.6.1. This is indeed the case as shown in Fig.7.1 where the saturated drain current at \( V_G = 5, 10, 15 \) and 20V is plotted against the length \( d \) of the parasitic FET. Both experimental (Fig.7.1a) and simulated (Fig.7.1b) results show conclusively that the current through the SGT is independent of \( d \). Note that in conventional (long channel) FET devices the current obeys the scaling rule \( w/L \) where \( w \) is width and \( L \) is length of the channel. Clearly this is not the case for SGT devices.

Fig. 7.1 Plot of the normalised saturation current per unit width as a function of source-drain separation \( d \); a) experimental and b) simulated (for barrier height 0.63eV) results.
The drain current in a SGT, therefore, should scale only with source width $w$ whilst for a FET it scales as $w/L$. Therefore we expect the linear relationship between the drain current and device width. Indeed as expected, a linear relationship between saturation current and source width $w$ is found as shown in Fig. 7.2 for four different gate voltages.

![Fig. 7.2 Plot of the saturation current as a function of source width $w$.]

### 7.2 Source length

The current ($I_D$) through the SGT is determined by a reverse biased source barrier i.e. it depends on $\Phi_B$ and its field dependence and the area of the source. Previously, it has been shown that $I_D$ scales linearly with the source width but is "independent" of s-d separation $d$. In case of source length $s$ (defined in Fig. 6.4) it is found that $I_D$ increases linearly with $s$ for high $\Phi_B$. However for lower $\Phi_B$ the current has a tendency to saturate with increasing source length $s$ (Fig. 7.3a).

The dependence of current on source length $s$ calculated using Silvaco ATLAS is shown in Fig. 7.3b. It is seen that the trend between source current with source length is in reasonable agreement with experiment (Fig. 7.3a).

With low barriers and high currents the source current tends to saturate with increasing source length. The reason why the current tends to saturate can be seen with reference to Fig. 7.4 where the current density normal to the Schottky barrier interface (taken 1nm from the source barrier along the x-axis) is calculated.
Chapter 7. Dependence of SGT characteristics on device geometry

It is seen that for higher current (barrier height of 0.4eV) passing across the interface (Fig. 7.4a) the current density is not uniform and is more concentrated towards the edge of the source opposite the drain contact. As the current through the source increases there is a lateral voltage drop under the source barrier (Fig. 7.5a) with a large electric field gradient away from the edge of the source and as the source length is increased a smaller fraction of current per unit source length is added to the source current.

With low currents (barrier height of 0.6eV), however, the lateral voltage drop is much smaller (Fig. 7.5b) and there is a fairly uniform current density along the source (Fig. 7.4b) giving a linear dependence between source current and source length $s$ for low current SGT devices.
Chapter 7. Dependence of SGT characteristics on device geometry

7.3 Source-Drain separation

A general form of SGT is shown in Fig. 7.6a. This is a symmetric structure with an ohmic drain contact on either side of a source barrier. The gate lies opposite the source so that it can modulate the whole of the source barrier when a voltage is applied. The current flows over the source barrier to the semiconductor-insulator interface and then laterally to an ohmic drain region. This structure is suited to high mobility semiconductors such as polysilicon since the extrinsic drain resistance between the source and the drain contact will be low. In this case, the off-state depends on the height of the source barrier and its dependence on drain voltage whilst the on-state is determined by the effect of the gate voltage on the effective barrier height.

For low mobility semiconductors the extrinsic drain resistance is prohibitive without using conductivity modulation at the semiconductor-insulator interface as in a FET. The structure (Fig. 7.6b) has more parasitic capacitance but low drain resistance. Effectively we now have an SGT in series with a parasitic FET of length $d$. The off-state is now determined by the threshold characteristics of the FET whilst the on-state is determined by the characteristics of the SGT and effect of the gate voltage on the effective barrier height. In Fig. 7.6b the drain and source contacts are assumed to be Schottky barriers; reverse biased at the source and forward biased at the drain.

The good modelling results around saturation enabled us to predict the effect of the source-drain separation and the parasitic FET in series with the source (channel length $d$ in Fig. 7.6). Clearly for a given source current the characteristics will become increasingly influenced by the parasitic FET as $d$ increases and the current becomes limited by the FET. However if the $d$ is small the voltage drop in the parasitic FET at $V_{Sat}$ is very small. An example can be seen in the previous Fig. 7.5. When $V_d$ is above the saturation voltage (~2V) the source depletion layer extends into the...
Chapter 7. Dependence of SGT characteristics on device geometry

Fig. 7.6 (a) General form of SGT where the gate lies opposite the source barrier and the drain contacts are ohmic; (b) SGT with extended gate in order to minimize the extrinsic drain resistance.

channel of the parasitic FET (region \(d\) between source and drain). At low drain voltages the potential drop across the FET is negligible while the source potential of the FET floats upwards to a value relative to the drain potential such that it just carries the saturation current supplied by the source barrier (Fig. 7.5). When \(V_D > V_G - V_{TH}\), which is around 7V in this case, the device pinches off at the drain (see also Fig. 9.6b) and the parasitic FET also operates in saturation and becomes depleted. This situation at large drain biases leads to further improvements to the output impedance.

The influence of the parasitic FET in series with the source is shown experimentally in Fig. 7.7a for a high barrier device \(t_{aSi} = 100\) nm. For short source-drain separations the change of \(V_{SAT}\) with \(V_G\) is in good agreement with the dielectric model for the SGT \(^{51}\) \((dV_{SAT}/dV_G = C_G/(C_G + C_S))\) while for large separations it tends to the FET limit for long channel devices \((dV_{SAT}/dV_G = 1)\) \(^{42}\). Computer calculations (Fig. 7.7b) show the same behaviour \((t_{aSi} = 60\) nm\). Overall these results show that \(V_{SAT}\) is not strongly dependent on \(d\) and wide variations can be tolerated without large changes in \(V_{SAT}\). For example for a source-drain separation as large as 10 microns \(dV_{SAT}/dV_G\) is still four times lower than a FET \(^{56}\).

It was shown in Fig. 7.1 that the saturation current is independent of s-d separation. However for large s-d separation the situation is different, here the current starts to be restricted by the parasitic FET and falls. This is shown in Fig. 7.8, where the simulated SGT device output characteristics are shown for different \(d\) and gate voltage. The s-d separation varies from 2 to 40 microns and gate voltage from 10V to 20V with steps of 5V.
Chapter 7. Dependence of SGT characteristics on device geometry

Fig. 7.7 The change in saturation voltage with gate voltage for SGT's with a range of source-drain separation (a) experimental and (b) simulated results ($\Phi_B = 0.4$eV, $s = 5$ microns) [56].

Fig. 7.8 Simulated SGT transistor characteristics plotted for different s-d separations and gate voltage ($\Phi_B = 0.4$eV, $s = 4$ microns, $t_{s-ST} = 60$nm, $t_{STN} = 300$nm).

Clearly it can be seen how with the increasing of the parasitic FET channel the transistor characteristics deteriorate: i) the saturation voltage increases because of higher voltage drop across the parasitic channel $d$ and ii) the current falls due to current restriction by the parasitic FET. Consequently as one would expect the SGT behaves as a conventional FET for the widest s-d separations.

On the other hand using the simulations to explore SGT possibilities for very small s-d separations leads to very interesting results. The simulated device was the same as in previous figure ($\Phi_B = 0.4$eV, $s = 4$ microns, $t_{s-ST} = 60$nm, $t_{STN} = 300$nm) but the s-d separation varied from 2 to 0.5 micron. Generally these transistor characteristics for $\Phi_B = 0.4$eV shown in Fig. 7.9 are considered as a high current device ($2 \times 10^{-7}$A/um). It might be seen that for shortest s-d separation
the slope of the linear part is getting steeper and as a consequence \( V_{SAT} \) is lower because the voltage drop across the parasitic channel is now smaller. As we see, the low saturation voltage is preserved albeit less well defined in comparison with a low current device (see e.g. Fig.6.9a). Furthermore the output impedance remains high with very little deterioration even for sub-micron source-drain separations. This feature illustrates the good screening of the source from the drain field provided by this geometry and shows that it should be possible to make sub-micron structures while preserving good transistor characteristics.

![Graph](image)

**Fig. 7.9** Simulated SGT transistor characteristics for high current devices with small s-d separations.

Comparison of the simulated SGT and FET transistor characteristics for devices with sub-micron dimensions and the same geometry \((d = L = 250\text{nm}, \ s = 1\ \text{microns})\) is shown in figure 7.10. It is seen that the SGT indeed preserves its characteristics for very short s-d separation of 250nm.

![Graph](image)

**Fig. 7.10** a) SGT \((\Phi_B = 0.35\text{eV})\) and b) FET output characteristics for the same device geometry \((d = L = 250\text{nm}, \ s = 1\ \text{microns})\) showing the superiority and perspective of SGT at sub-micron scale.

The layer thickness of a-Si:H and SiN was 25nm and 100nm respectively.
Chapter 7. Dependence of SGT characteristics on device geometry

The current level for the SGT is quite high due to the small barrier height of 0.35eV. Unlike the SGT, the FET characteristics for the same channel length show rapid deterioration of device performance and lack of saturation due to short channel effects.

7.4 Semiconductor and insulator layer thickness

The relationship between the semiconductor and insulator layer and their influence on SGT device performance is well described by the dielectric model (Eq.4.1). The dielectric model assumes that in saturation the semiconductor layer is depleted and the semiconductor and insulator layer are behaving as two dielectrics in series. In the model these layers are related using their capacitances per unit area. Here we are mainly concerned with a-Si:H and SiN used as semiconductor and insulator layers.

1) Semiconductor layer - In Fig.7.11 the simulated SGT transistor characteristics for different thickness of a-Si:H are shown. The thickness of SiN was 300nm, $\Phi_b = 0.6$eV, $s = 4$ microns, and $d = 1$ micron. Clearly it can be seen that reducing the thickness to 60nm reduces $V_{sat}$ and increases the saturation current. The reason for the higher $I_{sat}$ is that in the case of a thinner a-Si:H layer there is higher electric field induced by the gate pulling the effective source barrier down and therefore more electrons can tunnel through the barrier down to the S-I interface and then laterally towards the drain. Also the slope of the curve in the linear region is steeper due to a higher conductivity in the parasitic channel and a higher electron accumulation layer. $V_{sat}$ will consequently be lower due to the fact that the charge accumulated at the S-I interface underneath the source barrier will be depleted faster with applied drain voltage because now we have a higher electric field for the same potential. Also note that saturation is reached earlier even though there are more electrons at the S-I interface that have to be depleted in order to reach saturation. Obviously then $V_{sat}$ below 1V (at $V_G = 10$V) for the thinner a-Si:H can be achieved.

![Fig. 7.11 Simulated SGT transistor characteristics for different thickness of a-Si:H ($t_{SiN} = 300$nm).]
2) Insulator layer - The situation in the case of the SiN layer and its influence on SGT device performance is similar in terms of saturated drain current. Here, decreasing the thickness of SiN increases \( I_{Sat} \) for the same reasons as for the a-Si:H layer. The barrier is pulled down by the higher electric field induced by the gate for thinner SiN. Consequently the electron accumulation at the S-I interface is higher and it takes a higher drain field (voltagge) to deplete the region underneath the source barrier. Therefore \( V_{Sat} \) will be higher for thinner SiN layers but it is still much lower than in a FET device. The relationship between \( V_{Sat} \) and layer thickness is very well given by the dielectric model (Eq.4.1). The dependence of \( V_{Sat} \) and \( I_{Sat} \) on the SiN thickness from simulations is shown in Fig.7.12. The thickness of a-Si:H was 60nm, \( \Phi_0 = 0.4 \text{eV}, \) \( s = 2 \text{ microns}, \) and \( d = 0.5 \text{ micron}. \) The change of \( V_{Sat} \) per 1V change of \( V_G \) can be obtained from the slope of the curve (Fig.7.12a). It can also be seen that this change even for 100nm of SiN (0.26) is almost 4 times lower than for a conventional FET.

![Graph showing the dependence of \( V_{Sat} \) and \( I_{Sat} \) on SiN thickness](image)

*Fig. 7.12 Dependence of a) \( V_{Sat} \) and b) \( I_{Sat} \) on the SiN thickness plotted as a function of gate voltage (\( t_{a-Si} = 60nm \)).*

The experimental results show a similar trend. The experimentally measured transfer characteristics of a SGT device for SiN of 150nm and 300nm is shown in Fig.7.13. The additional parameters were the ion dose of \( 1 \times 10^{14} \text{ p}^{-3} \text{cm}^{-2}, \) thickness of a-Si:H = 100nm, \( s = 5 \text{um}, w = 12 \text{um} \) and \( d = 2.5 \text{um}. \) The transfer characteristics were measured at \( V_G = 5 \text{V} \) and for both 300nm and 150nm of SiN show the on-off ratio >5 orders of magnitude. The off current is very low in both cases (~50fA) which is the resolution of the measurement setup but for the higher negative \( V_G \) and SiN = 150nm the current increases due to leakage between the source and drain caused by a non-optimal value of the compensating implant. As expected the on-current, however, is different and approximately a factor of ~3 higher for 150nm compared with 300nm of SiN. The value of dynamic range for \( V_G \) up to 20V has increased from ~40 (\( t_{SiN} = 300nm \)) to ~150 (\( t_{SiN} = 150nm \)).
Also the subthreshold slope for thinner SiN is steeper (~0.6V/dec) in comparison with 300nm of SiN (~0.9V/dec).

![Graph showing the measured transfer characteristics of a SGT device for SiN thickness of 150nm and 300nm.](image)

**Fig. 7.13** The measured transfer characteristics of a SGT device for SiN thickness of 150nm and 300nm.

We also expect similar behaviour for higher doses of barrier lowering implant and this situation is shown in figure 7.14 where the comparison between the 150 and 300nm of SiN is shown for different ion doses. Indeed the saturated drain current (for $w = 12\,\mu m$) is raised with ion dose due to the higher electric field applied to the barrier for the same gate voltage. The saturation voltage is plotted against ion dose in Fig. 7.14b. The $V_{sat}$ for 150nm of SiN increases due to the higher electron accumulation and the need for higher drain field to deplete electrons under the source barrier.

![Graph showing the saturated drain current and saturation voltage plotted as a function of barrier lowering implant for different thickness of SiN (150nm and 300nm) and the same $V_g = 10V$.](image)

**Fig. 7.14** a) Saturated drain current and b) saturation voltage plotted as a function of barrier lowering implant for different thickness of SiN (150nm and 300nm) and the same $V_g = 10V$. 
7.5 Chapter summary

In this chapter the key effect of geometrical parameters: source length, s-d separation and thickness of semiconductor and insulator layer on SGT device performance were discussed. Generally when increasing the source length the current through the device increases linearly but for lower barrier, high current devices it has the tendency to saturate. The source current is independent of s-d separation up to a value that depends on current density. Long s-d separation can significantly influence the SGT device performance because the parasitic FET starts to limit the current and the majority of the drain voltage will be dropped across the parasitic FET region resulting in an increase in \( V_{\text{sat}} \). Simulations and experiments showed that as expected \( V_{\text{sat}} \) and \( I_{\text{sat}} \) increase with thinner layers of SiN for a given thickness of a-Si:H. On the other hand lowering the thickness of a-Si:H reduces \( V_{\text{sat}} \) and increases \( I_{\text{sat}} \) for a given thickness of SiN.
Chapter 8

8 Characterisation of the Schottky source barrier

8.1 Introduction

The key feature of the Source-Gated Transistor is the source barrier. In chapter 5 and papers on the source-gated transistor containing a Schottky source barrier it has been stated that the current is determined by the magnitude of the electric field at the barrier and its effect on current transport through the reverse biased barrier. Therefore the current through the device is determined by the effective barrier height of the Schottky barrier and its mutual conductance (transconductance \( g_m \)) is determined by the change of this current with the gate voltage. In this chapter we examine the assumptions more closely by analysing the transistor characteristics in closer detail and comparing them with what we expect from thermionic-field emission based on previous measurements of this phenomenon in a-Si:H. This is necessary because some published simulations of the SGT in a-Si:H (Lindner et al., 2005 [57]) suggest that the source behaves as a large series resistance that is limiting the current and no assumptions about tunnelling through a source barrier are needed.

8.2 Barrier analysis

Source-Gated Transistors have been made in a-Si:H with a Schottky barrier acting as a source. The effective barrier height of the Schottky source was adjusted using a shallow phosphorous implant to control the electric field at the surface and modify the amount of quantum-mechanical tunnelling through the barrier [51]. The surface field, therefore, had two components, one due to the implant and the other dependent on the voltage applied to the gate. In Fig.8.1 the modified
Chapter 8. Characterisation of a Schottky source barrier

band diagram through the source of the SGT device in saturation is shown. Also the modified surface field due to the implant and gate bias can be seen. It has been shown in the past [37] and discussed in section 3.2.2.2 that for fields greater than \(-3 \times 10^5\) V/cm in a-Si:H, current through a reverse biased Schottky barrier is determined by thermionic-field emission with an electron effective mass of \(-0.1 m_e\).

Since surface fields are large following the implant we can assume that thermionic-field emission applies in this case. However when the current through the a-Si:H is high one has to be aware that the magnitude of the current could be affected by space charge or restricted by diffusion of electrons away from the barrier particularly when the applied field is small.

Detailed calculations of the thermionic-field emission current through a reverse biased triangular Schottky barrier with image force correction shows that it is a reasonable working approximation to assume that the current increases exponentially with electric field [37, 38] (see section 3.2.2.2). Making this assumption the current \(I_S\) becomes

\[
I_S = S A^* T^2 \exp \left(-\frac{q}{kT} (\Phi_B - \alpha E_S)\right)
\]

Where \(S\) is the area of the source, \(\Phi_B\) is the effective barrier height of the source barrier modified by the implant, \(E_S\) is the electric field in the a-Si:H induced by the gate (positive) and \(\alpha\) is a tunnelling constant. Calculations show that this approximation is reasonable over the field range 3–8x10^5 V/cm [37] but for higher fields the current against field curve rolls off (see Fig.5.4 and Fig.5.5). Furthermore if one used Eq.8.1 to obtain \(\Phi_B\) by extrapolating \(\log I_S\) to zero applied field then the current is underestimated and the barrier height is too high (as indicated by simulations in Fig.6.12).

The electric field in the a-Si:H above \(V_{SAT}\) is simply \(V_{SAT} / l_{a-Si}\). The saturation voltage can be expressed using the dielectric model [51] and Eq.4.2 where it is assumed that the a-Si:H is depleted in saturation.
Assuming uniform emission over the area of the source barrier, the tunnelling constant $\alpha$ and the effective barrier height, $\Phi_b$ of the source can be determined from the measured transistor characteristics as follows. From Eq.8.1 and Eq.4.2 the transconductance $g_m$ ($\partial I_S/\partial V_G$) is given by:

$$g_m = \alpha \frac{I_S}{\varepsilon_s \varepsilon_0} \frac{q}{kT} \frac{C_s C_G}{C_s + C_G}$$ (8.2)

The tunnelling constant can therefore be obtained by measuring the slope of the $g_m$ vs. $I_S$. (Eq.8.2). Furthermore the effective barrier height of the source following the implant can be obtained from Eq.8.3 using measured values of the $\alpha$ and $V_{SAT}$ since from above

$$\Phi_b = \frac{kT}{q} \ln \frac{SA'T^2}{I_S} + \alpha \frac{V_{SAT}}{t_{a-Si}}$$ (8.3)

The measured transistor characteristics of a SGT is shown in Fig.8.2 along with drain current and transconductance against gate voltage measured at $V_D = 5V$ (Fig.8.2b). The s-d separation was 2 microns and source width 12 microns. It is seen from Fig.8.2 that strong saturation is accompanied by a low saturation voltage.

The measured transistor characteristics of a SGT is shown in Fig. 8.2 along with drain current and transconductance against gate voltage measured at $V_D = 5V$ (Fig.8.2b). The s-d separation was 2 microns and source width 12 microns. It is seen from Fig.8.2 that strong saturation is accompanied by a low saturation voltage.
change from the FET off-current to the SGT limited on-current can be seen when plotting the transconductance $g_m$ as a function of gate voltage (Fig. 8.2b - blue curve). At high gate voltages $g_m$ increases steadily with voltage but at voltages close to threshold there is a hump in the curve. This occurs because close to its threshold voltage $V_{th}$ the parasitic FET continues to control the current and it increases with $(V_G - V_{th})^2$. Therefore $g_m$ increases linearly with gate voltage as indeed is seen in Fig.8.2b and it can be deduced that $V_{th} \approx 3$V and the field effect mobility in the parasitic FET is $\approx 0.2$cm$^2$/Vs. However as the gate voltage is increased further the current becomes controlled by the source barrier and the $g_m$ increases more slowly. It is seen that had there been an ohmic contact then $g_m$ at $V_G = 11$V would have been $\sim 3$ times greater. A plot of $g_m$ against drain current gives close to a linear dependence as predicted by Eq.8.3 and from the slope the effective tunnelling constant $\alpha$ was calculated to be 2.4nm (see Fig.8.3).

![Fig. 8.3 The plot of the transconductance ($g_m$) as a function of saturated drain current for a barrier lowering implant dose of 4x10$^{14}$ cm$^{-2}$ of P' at 10keV. The slope of the curve is directly proportional to the tunnelling constant $\alpha$.](image)

Using the barrier analysis above the effective barrier height of the source following the barrier modification by ion implantation and its dependence on gate voltage can be obtained. Examples are shown in Fig.8.4.

In Fig.8.4a the effective source barrier height is $\sim 0.62$eV. This is pulled down to a value of 0.54eV for $V_G = 20$V. The source barrier of the transistor shown in Fig.8.4b had a higher dose of phosphorous implanted into it. The barrier height in this case is $\sim 0.50$eV. A plot of effective barrier height as a function of implanted phosphorous is shown in Fig.8.5. The plot shows $\Phi'_{th}$ obtained from Eq. 8.3 and $\Phi_{th}$ when it has been pulled down using 10V on the gate. Clearly, as expected, the effective barrier height decreases with increasing phosphorous dose and gate voltage.
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Fig. 8.4 The values of $\Phi_b$ plotted as a function of gate voltage together with effective barrier height $\Phi'_b$ for two different barrier lowering implant doses of a) 5x10^{13} and b) 4x10^{14} cm^{-2} P^{31} at 10keV.

Fig. 8.5 The estimated barrier heights and their effective values $\Phi'_b$ at 10V on the gate are shown as a function of the barrier lowering implant (P^{31} 10keV).

Having obtained the effective barrier height against dose (Fig. 8.5) one can estimate the total electric field at the source barrier due to the implant together with the field induced by the gate voltage and the tunnelling constant obtained as a function of total electric field.

A plot of this dependence (Fig. 8.6) shows that the effective tunnelling constant decreases with increasing electric field. At the lowest electric fields and high source barriers (~8x10^4 V/cm) the value of $\alpha$ is similar to that measured in the past on reverse biased Schottky barriers in this field range [37, 38]. The decrease in effective tunnelling constant as the field increases is consistent with computer calculations that show a steady roll-off of the thermionic-field emission current at high fields [37].
Chapter 8. Characterisation of a Schottky source barrier

3.4
3.2
3.0
2.8
2.6
2.4
2.2

2.0x10^6 1.0x10^6 1.2x10^6 1.4x10^6

Total electric field [V/cm]

Fig. 8.6 Calculated values of tunnelling constant $\alpha$ based on equation (8.2) plotted as a function of total electric field. Thickness of SiN = 300nm.

When $\alpha$ is known, the change of effective barrier height with gate voltage can be determined as shown in Fig. 8.7. In Fig. 8.7 we show $\Phi'_{b}$ against gate voltage for two different samples one with a nitride thickness of 300nm the other 150nm. Also shown are activation energies ($E_a$) for current transport obtained from Arrhenius plots similar to that shown in Fig. 12.5

$$I_S = A \exp\left(-\frac{E_a}{kT}\right)$$  \hspace{1cm} (8.4)

Fig. 8.7 The comparison between calculated effective barrier height $\Phi'_{b}$ and measured activation energy of the reverse polarised source barrier as a function of the gate voltage. A barrier controlling implant of 5x10^{13} \text{ cm}^{-2} and 3x10^{14} \text{ cm}^{-2} was used with the thick and thin nitride respectively.

It is apparent that the activation energy is higher than the effective barrier height $\Phi'_{b}$ obtained from the analysis above whereas we would expect them to be similar since they both determine the barrier height of a thermally activated transport process. The reason for this discrepancy,
however, most probably arises because in calculating $\phi_b$ we assume that the current is emitted uniformly over the source barrier. In practice, computer simulations shown in chapter 7. [58, 59] indicate that the current peaks at the edge of the source barrier directly opposite the drain contact and there is a large reduction in the effective emitting area. Taking this effect into account will make a significant reduction to the effective barrier height $\phi_b$. However what is more important when considering just how the source works, is the change of the barrier height with gate voltage. Fig.8.7 shows that there is fair agreement between the slope of the barrier vs. gate voltage plots particularly for the high barrier, low current device. The slope of the activation energy plot for the low barrier (high current) device, however, gradually deviates further from that of the $\phi_b$ plot as $V_G$ and the current increases and the barrier height becomes lower. These results suggest that either the current is getting more and more concentrated at the edge of the source or that another mechanism apart from thermionic-field emission is limiting the current. Possible mechanisms that could limit the current at high currents include space charge effects and diffusion limited effects.

In the latter case the current could be no longer limited by how many carriers are emitted through the source barrier but by the rate at which carriers can diffuse towards the drain in the complicated two-dimensional field configuration under the source.

These results show conclusively that it is the change in the effective barrier height with the gate voltage that determines the transistor characteristics as proposed by Shannon and Gerstner [51] and not a series resistance as proposed by Ref. [57].

### 8.3 Chapter summary

Measurements on source-gated transistors in a-Si:H with a Schottky barrier source controlled by ion implantation have been analysed assuming the source current is limited by thermionic-field emission. From measurements of the mutual conductance ($g_m$) of the transistors the effective barrier height of the source was obtained as a function of the gate voltage together with a tunnelling constant characteristic of the thermionic-field emission process.

It was found that for high barriers and low currents the tunnelling constants were in good agreement with those measured previously in a-Si:H. Furthermore the change in effective barrier height with the gate voltage obtained from the thermionic-field emission model was in good agreement with measurements of changes in the activation energy for the current transport process. We therefore conclude that the current through these SGT's is determined by the field dependence of the thermionic-field emission process in the reverse biased source Schottky barrier.

For low barriers and high currents the thermionic-field emission analysis give lower tunnelling constants and the barrier heights were higher that those measured experimentally. This discrepancy is mostly explained by current crowding at the edge of the source. However it is also
likely that the current transport process became diffusion or space-charge limited. In this case, current is determined by the field dependence of transport through the bulk of the a-Si:H layer rather than the supply of carriers from the Schottky barrier.
Chapter 9

9 Stability of SGT devices

9.1 Introduction

Device stability is a very important issue for modern devices and is very closely related to device lifetime. This issue is more prominent with materials such as hydrogenated amorphous silicon where thin-film field-effect transistors (FET's) made in a-Si:H are notoriously unstable. The characteristics of these devices show large changes under prolonged application of gate voltage. These changes are usually characterized by a shift in the threshold voltage, with little change in mobility and a reduction in drain on-current during operation. This degradation of device performance severely limits their use in analogue circuits for displays and large area electronics, in general. The applications are limited to a pixel switch in AMLCD array (for more details see Chapter 2) and anything more demanding such as peripheral or driver circuitry is very difficult or impossible to achieve. In order to get around degradation, sophisticated correction circuits [60] are used which correct the on-current shift and extend the lifetime of devices but they are unable to stop the degradation mechanism and can only make corrections for small changes in current.

Two separate mechanisms have been found to contribute to this effect:

1) The first contribution comes from the changes in the DOS of the a-Si:H itself. Defects in the channel of the a-Si:H TFT device are created that trap charge carriers and change the threshold voltage. This mechanism was described in Chapter 2. (section 2.3.1), but briefly we can say that strained or weak Si – Si bonds break in the presence of band tail carriers (e.g. electron) and form two dangling bonds (DB). These broken (weak) Si – Si bonds are prevented from recombination by a hydrogen atom that moves in to passivate one of the DB. The result is a negligible increase in tail states but a larger increase in the density of defect states. This process depends on the electron concentration and the position of the electron quasi-Fermi level (discussed in section 2.3.1).
Therefore the higher the electron concentration the higher is the defect generation rate and trapping of electrons. Electrons trapped in these states act as fixed negative charge for positive gate voltage. The result is a reduction in band bending at the S-I interface giving a decrease in drain on-current. Because there is only a small decrease in field-effect mobility, this translates into a positive shift of $V_{TH}$. This process is dominant for lower fields and gate voltages (<25V) [61] and is temperature sensitive.

2) The second is the trapping of electrons that tunnel into the gate insulator. The charge trapping in the nitride gate insulator into which the electrons are transferred from a-Si:H builds up a negative charge. Any charge trapped in the insulator layer contributes to an increase in the threshold voltage $V_{TH}$ according to the following Eq.9.1 [62]

$$\Delta V_{TH} = \frac{q\Delta N_{trap}}{C_G}$$

(9.1)

where $\Delta V_{TH}$ is the threshold voltage drift, $\Delta N_{trap}$ is the number of trapped charges per unit area after gate stress and $C_G$ is the gate-insulator capacitance per unit area. This is a strongly field dependent process which requires high field and gate voltages (~50V) [12] but is not strongly dependent on the quality of the insulator.

The creation of DB leads to an increase in the $V_{TH}$ for both polarities (i.e for negative $V_G$ the $\Delta V_{TH}$ is negative). If the charge trapping in the insulator dominates then $\Delta V_{TH}$ is positive for both polarities of $V_G$. Defect kinetics is a complicated process, and a fuller description is given in Ref. [63].

9.2 Stability measurements

Stressing experiments were undertaken at voltages that would be used in typical circuit applications (<15V). Therefore electric fields were not abnormally high (i.e. the expected degradation mechanism is due to dangling bond creation). The FET and SGT devices were made using the same deposition conditions for the insulator (SiN) and a-Si:H. All experiments were carried out at elevated temperature of 30°C and under continuous DC stressing in order to accelerate the degradation of devices. The majority of experiments involved measurements of the device transfer characteristics (up to 30 measurements) over a period of 24 hours of continuous stressing. New software was developed (different than for I-V measurements above) in order to accommodate the experimental requirements needed to control the measurement equipment over 24 hours. This was quite important in order to avoid possible human errors influencing the experimental results. It was expected that most of the degradation occurs in the first hour and therefore measurements were made more frequently during this period.
An example of such an experiment can be seen in Fig.9.1 where the transfer characteristics of a FET and SGT following stress at 30°C, $V_G = 12V$ and $V_D = 10V$ for various stressing times are shown. The first and the last measurements are distinguished by a different line style (and colour).

![Fig. 9.1 Drift in the transfer characteristics of (a) a FET ($w = 50$ and $L = 10um$) and (b) SGT device ($w = 12$ and $d = 3um$) measured at $V_D = 10V$ for various stressing times over 24 hours.](image)

The stressing conditions are $V_G = 12$ and $V_D = 10V$ at 30°C.

The FET shows the classical $V_M$ shift, which affects the on-current right up to the maximum gate voltage of 15V. The value of $V_{TH}$ at the 1st measurement was $-2.3V$ and after 24 hours it changed to $-4.3V$, so $\Delta V_{TH} \approx 2V$. The SGT has some threshold shift $\Delta V_{TH} \approx 0.5V$ ($V_{TH}$ has changed from $-2.2V$ to $-2.7V$) when the current is determined by the parasitic FET. However in the on-state, when the current is controlled by the source barrier, the device is much more stable than the FET.

The instability in a-Si:H TFT is related to the position of the electron quasi-Fermi level in the device during operation and its deviation from the equilibrium level. Changes in the quasi-Fermi level lead to defect generation, electron trapping and the threshold voltage changes as described earlier (section 2.3.1). In general the greater the electron concentration the higher the defect generation rate. Therefore in the accumulated channel of a FET large numbers of defects are formed while in the depleted source region of a SGT the defect generation rate is small [6] because the quasi-Fermi level in the depleted source at the S-I interface is close to midgap and similar where it was when a-Si:H was grown. Therefore, the distribution of states in chemical equilibrium will be similar and the rate of defect generation at the S-I interface in the SGT device will be small. This explanation proposed by Shannon [65] is supported by simulations [59]. Computer simulations (Fig.9.2) indicate that depletion of the source region at the S-I interface gives rise to electron concentrations orders of magnitude lower in a SGT than it is in a FET but the amount depends on the effective barrier height of the source and the magnitude of the electron current.
Chapter 9. Device stability in a-Si:H

The electron concentration profiles were taken (at $V_G = 10\text{V}$) from a SGT where the cut-line was at the edge of the source (few nm inside of source), across the a-Si:H down to the S-I interface. In the case of the FET the source region was highly doped and therefore the cut-line was 100nm away from the source otherwise the electron concentration would be very close to that in the $n^+$ doped source region. The channel length of the simulated FET device was $L = 4\text{ um}$ and $d = 1\text{um}$ for the SGT ($s = 5\text{um}$). Calculations are shown for two SGT’s ($\phi_B = 0.4$ and 0.5eV) and a FET. Blue lines are when $V_D > V_{SAT}$ (depletion) and red lines when $V_D < V_{SAT}$ (accumulation). The simulations clearly show that depletion occurs at the source region at the S-I interface and the electron concentration is lower than it is in a FET. This feature is directly responsible for better device stability.

Fig. 9.3 shows the degradation of on-current with stressing time for a FET and SGT corresponding to devices shown in Fig.9.1 but on a linear scale. The on-currents were extracted from transfer characteristics for different gate voltage (6, 8, 10 and 12V). On the x-axis is therefore time and on the y-axis is the ratio of the actual current in time $t=x$ and the initial drain current (measured at $t = 0$). For example if we compare the on-current drop for $V_G = 12\text{V}$ the current in the FET device drops down to ~73% after 24 hours stress while in the SGT it is ~88%. But this situation gets worse for lower $V_G$ closer to the knee of the characteristics where the variation with $V_{TH}$ is much larger. It can be seen that for $V_G = 8\text{V}$ and 6V this drop is down to 52% and 28% respectively for the FET. On the other hand the drop in the SGT for the same gate voltage is much lower 87% and 78%.
Chapter 9. Device stability in a-Si:H

Fig. 9.3 Degradation of on-current with stressing time for a) FET and b) SGT device corresponding to Fig.9.1.

If we extrapolate the degradation in time we can get approximate values for the SGT to reach the same degradation of the on-current as the FET (Fig.9.4). For $V_G = 12\text{V}$ we get the same degradation after 695 days (more than 2 years) of continuous stressing and for $V_G = 8\text{V}$ extrapolation gives $\sim 1 \times 10^4$ years.

Fig. 9.4 The extrapolated values of on-current decay with current stress for $V_G = 12\text{V}$ and $8\text{V}$.

This value whilst very approximate underlines the superior stability of SGT devices against temperature / voltage / current stressing compared with a FET.

Further experiments and simulations showed that the SGT devices could be even more stable than those shown above. This is also due to their specific construction and different mode of operation. The experimental results for devices biased with $V_D > V_G - V_{TH}$ and two different s-d separation 3um (SiN = 300nm) and 2.5um (SiN = 150nm) is shown in Fig.9.5 after 24hours of stress at 30°C, $V_G = 8\text{V}$ and $V_D = 10\text{V}$ and 12V respectively.
Indeed both SGT devices show very little threshold voltage shift and literally no on-current shift. The proposed explanation of this excellent stability is presented in the next few paragraphs. The device in Fig. 9.5b has shorter s-d separation and width is only 1 micron but also higher leakage current ($7 \times 10^{-10}$ A). The higher leakage is most likely due to insufficient compensation of donors in the $d$ region between source and drain but this leakage has no effect on the stability of the device.

The potential and electron distribution profiles along the S-I interface under the source for 0.5eV barrier height also showing the region of the parasitic FET are plotted in Fig. 9.6.

Similar potential profiles have been shown previously but for a different barrier height. Simulated device had $d = 1$ um, $s = 4$ um, $t_{Si} = 100$ nm and $t_{SiN} = 300$ nm. With $V_D$ above the saturation
Chapter 9. Device stability in a-Si:H

Voltage (>2V) the source depletion layer extends into the channel of the parasitic FET. At low drain voltages (<7.5V) the potential drop across the FET is negligible while the source potential of the FET floats upwards to a value necessary to carry the saturation current supplied by the source barrier. However with \( V_D > V_G - V_{th} \), which is around 7V in this case, the device pinches off at the drain as well as the source (Fig.9.6b) and the parasitic FET is also being depleted and then for values of \( V_D > V_G - V_{th} \) the parasitic channel is fully depleted of carriers resulting in smaller capacitances and charging time. This situation when the drain is biased higher than gate electrode leads to further improvement of device stability and as mentioned previously also to higher output impedance. Also what is very important is the s-d separation i.e. length of parasitic FET channel.

The situation for a s-d separation of 5um is seen in Fig.9.7 where potential and concentration profiles for SGT device with \( d = 5um \) (\( s = 4um \), \( t_{ox} = 100nm \) and \( t_{sw} = 300nm \)) and barrier 0.5eV is shown. Clearly for higher drain potential above \( V_D > 8.5V \) the excess of the potential is dropped within 1um from drain edge and the depletion at the edge of the source is similar to that for a 1um s-d separation. Then the resulting electron concentration (region between \( x = 5.5um \) to \( 8um \) Fig.9.7b) is \( \sim 10^{16} \text{ cm}^{-3} \) and much smaller than that at lower drain voltages. Therefore, although the electron concentration is not as low as for the short channel device shown in Fig.9.6 (or Fig.9.5), there is still a major reduction with drain voltage that will decrease defect generation.

![Fig. 9.7 a) Potential and b) electron distribution profile along the semiconductor-insulator interface under the source for 0.5eV barrier height also showing the region of the parasitic FET.](image)

A more detailed plot of degradation of on-current with device stressing for the SGT corresponding to devices shown in Fig.9.5 is shown in Fig.9.8. The on-currents were extracted from transfer characteristics for different gate voltage (6, 8, 10, 12V and 15V). Obviously these devices have better stability than those shown in Fig.9.3. In the case of the device with 3um s-d
separation the on-current decay for all measured \( V_G \) is less than 4\% and for \( d = 2.5 \) micron it is even better; less than 2.5\%.

\[
\text{Fig. 9.8 Degradation of the on-current over time for SGT with a) } d = 3 \text{ and b) } d = 2.5 \text{um corresponding to Fig.9.5.}
\]

This situation with \( V_D > V_G - V_{th} \) brought us a much deeper understanding of how to improve the stability of the SGT and therefore other experiments were carried out to investigate the influence of \( V_D \) on device stability and on-current degradation. In figure 9.9 the on-current degradation is plotted for various \( V_D \) over 24 hours. Note that the plot shows five different devices of the same geometry and stressed at 30°C, \( V_G = 10V \). The transfer characteristics were measured at \( V_D = 10V \) (stressing \( V_D \) was variable). The values of drain current taken for this comparison were measured at \( V_G = 10V \).

It is clearly seen that an undepleted source (\( V_D = 0.1V < V_{sat} \)) degrades rapidly while applying a drain voltage above the saturation voltage (2.5V) provides us with a much stable mode of operation. Improvement for higher \( V_D \) is also significant and is due to depletion of the parasitic channel.

\[
\text{Fig. 9.9 Degradation of the on-current in time for SGT with } d = 3\text{um measured for different } V_D.
\]
Therefore to conclude this section about stability the decision was made to stress the same SGT device \((w = 2.5\, \text{um} \text{ and } d = 2.2\, \text{um})\) for a much longer period of time (i.e. 5 days) \(V_D\) will be changed while \(V_G\) is at a constant value (15V). In this case a higher \(V_G\) than \(V_D\) was chosen to enhance the degradation process (maximum value of \(V_D = 12\, \text{V}\)). The result is seen in Fig.9.10.

In the 1\textsuperscript{st} phase \((V_D = 12\, \text{V})\) the on-current has dropped by 7.6\% to 92.4\% of its initial value \((I_{D0})\). The same stressing was used also for 2\textsuperscript{nd} phase and on-current dropped another 2.7\% to 89.7\% of \(I_{D0}\). The \(V_D\) was changed in the 3\textsuperscript{rd} phase to 6V and the 4.9\% change in current was recorded giving subtotal drop 84.8\% of \(I_{D0}\). For the 4\textsuperscript{th} phase \(V_D\) was decreased further to 0.1V resulting in rapid decay of current down to 36.3\% of \(I_{D0}\). Between the 4\textsuperscript{th} and 5\textsuperscript{th} phase there was one-day break in measurement. The device was slowly cooled down to room temperature and stored in an airtight container. Then the 5\textsuperscript{th} phase was executed with \(V_D = 12\, \text{V}\). The relative on-current dropped during the 5\textsuperscript{th} phase was only 2.7\% which is exactly the same as during the 2\textsuperscript{nd} phase but what is more interesting is a recovery of the current between the 4\textsuperscript{th} and 5\textsuperscript{th} phase. The recovery was from a value of 36.3\% to 54.6\% of \(I_{D0}\) presumably due to some annealing of dangling bond defects during the one day interval.

One may argue that SGT transistors are more stable than FET’s due to a smaller on-current through the device caused by the source barrier. Therefore we decided to do another set of experiments where all results are plotted as a function of stressing current measured as the 1\textsuperscript{st} point of the stressing experiment. Then varying the stressing conditions for different SGT and FET devices we should be able to properly compare these devices. The comparison is shown in Fig.9.11 for SGT devices with s-d separation of 2-3um and a FET with \(L = 10\, \text{um}\).
It is seen that SGT devices biased with $V_D > V_{sat}$ are much more stable than the FET for the same value of the stressing current. Also we can say that for the same device stability the SGT is able to operate at a much higher current than the FET. One way of “improving” the performance of a FET is to decrease the channel length to 2um. The red curve shows the measured values of $I_D/I_{D0}$ for $L = 10$um but recalculated for current at $L = 2$um. Even though now the current is higher, it is still much less stable than a SGT for the same current. The interesting situation is when $V_D > V_G - V_{th}$. Then, as discussed above, the parasitic FET in the SGT is partly depleted, it pinches off at the drain and the stability is even better.

9.3 Chapter summary

A very interesting property of the SGT occurs because the electron concentration in the active source region is much lower than it is in the active channel of a FET. Computer simulations shown that the electron concentration in the source region at the semiconductor-insulator interface can be orders of magnitude lower than it is in a FET but the amount depends on the effective barrier height of the source and the magnitude of the electron current.

This feature has important implications for the stability of the device because changes of the electron concentration and therefore the electron quasi-Fermi level give rise to defect formation in amorphous silicon as it strives to reach a different chemical equilibrium. If changes between the electron concentration in the off and on states can be reduced then the device will be more stable to voltage / temperature / current stressing. It has been shown that SGT devices operating at low currents are almost completely stable [64, 65]. Furthermore it is found that a SGT is always more stable than a FET operating at the same current. Alternatively one can say that a SGT can be operated at a higher current than FET for the same stability (Fig.9.11).
Chapter 10

10 Transient response

10.1 Introduction

Switching circuits are very important part of digital electronics. If we consider large area electronics and thin film technology then the most common application of thin-film transistors is a pixel driver (switch) in AMLCD displays where each transistor controls one pixel of the display.

In general row drivers in active matrix displays require devices that operate in the kHz regime and require high currents with good stability. For column drivers however, we need devices that operate in the MHz region. At the present time the common solution to this requirements is to make the drive IC using crystalline silicon or lately with poly-Si and bond them to the substrate TFT back-plane. This solution has disadvantages such as less reliability and higher production cost compared with fully integrated drivers. Therefore there is strong pressure and need for fully integrated displays where row and column drivers are deposited at the same time as TFT back-plane. The first examples of integrated row drivers in a-Si:H were introduced recently [66].

As outlined above, the SGT can be operated with high internal fields and low carrier concentrations throughout by using a high drain voltage. We therefore expect low capacitance and short transit time particular if devices have small lateral dimensions. As described above, reduction in short-channel effects in the SGT enables narrow devices with good characteristics to be obtained. Therefore we believe that by using SGT devices fully integrated displays in amorphous silicon can be achieved that are stable and fast enough.

The simplest circuit is the transistor switch where the input is the gate electrode. The gate is capacitively controlling the output of the transistor. The circuit capacitance and resistance through which the transistor is charged and discharged constitute the predominant limitation factor on switching speed. In CMOS technology the charge transit time in the transistor is negligible in
comparison with TFT devices in a-Si:H where the mobility is significantly lower. Also the value of transconductance $g_m$ will determine how fast the device capacitances are able to charge and discharge.

The transient response $\tau$ of a FET can be determined by the gate charging time or the carrier transit time depending on various geometrical factors [67]. For the SGT however, the smaller $g_m$ and larger gate capacitance means that the gate charging time $\tau$ dominates and

$$\tau = \frac{C_g}{g_m}$$

where $C_g$ is the gate capacitance [68]. The charging time or switching time can be described in more exact terms in a practical situation using values of 10% and 90% of the output signal amplitude $I_{SAT}$. Usually in the textbooks the output values are related to the output voltage but here we are concerned with drain current therefore definitions of the parameters were modified as shown in Fig.10.1. The 10% and 90% figures were introduced to give a precise instant at which to measure these times. The turn-on time ($\tau_{ON}$) is the time from the instant that the input voltage goes positive to the moment when the output current of transistor reaches 90% of $I_{SAT}$ [67]. The turn-on time is divided into a delay time $\tau_D$ and a rise time $\tau_R$ as indicated in Fig.10.1. Similarly the turn-off time $\tau_{OFF}$ is the time from the moment that the input voltage returns to zero to the instant when the output current has fallen to 10% of $I_{SAT}$. The turn-off time is subdivided into the saturation time $\tau_S$ and the fall time $\tau_F$.

![Fig. 10.1 Showing a square-wave voltage input waveform and resulting output current waveform.](image-url)
10.2 Measured transient response

10.2.1 Experimental setup

The measurement setup used for transient response experiments is shown in Fig. 10.2. A square wave signal was applied to the gate input from the pulse generator (Agilent 81110A). The amplitude of the signal was 10V and frequency varied from 1kHz to 1MHz. The duty cycle was 50%. The drain of the SGT device was biased with a DC signal of 10V. There are two resistances in the circuit $R_s$ and $R_r$. If the transistor is switched on then the current passing through the SGT and the $R_s$ (91 Ohm) in series creates a voltage drop over $R_s$; this voltage drop is shown on the Digital Oscilloscope (Philips PM3392).

![Fig. 10.2 The measurement setup used for transient response experiments.](image)

The second resistance in the circuit ($R_r$) is necessary to suppress ringing in the response and should be as small as possible because it influences the rise time of the transient. Its optimal value in the circuit above was about 150 Ohms. The experimental data from the Oscilloscope are collected by PC using GPIB interface and Labview software (v7.0). All connections between the equipment and DUT (device under test) were made using coaxial cables. The cables were made as short as possible but they still influenced the experiment due to parasitic capacitance.

10.2.2 Experimental results

We soon realised that in order to obtain a good transient response we had to optimise the source circuit. The first thing was to optimise the $R_r$ resistance value. This was found to be 150Ω. There was a trade-off between the ringing in the response and the rise time. For higher $R_r$ values (470Ω and 1kΩ) the ringing was minimised but the turn-on and -off time were significantly increased. In Fig. 10.3 a sharp transient is shown with $R_r$ connected and disconnected to the circuit (Fig. 10.2). Clearly the ringing (presented as oscillations) is suppressed sufficiently with $R_r = 150\Omega$ in the circuit.
Chapter 10. Transient response

Fig. 10.3 Showing the sharp transient when the $R_r$ is connected (red) and disconnected (blue).

The next step was to optimise the resistance $R_s$. It was found that in order to minimise the duration of the sharp peak at the beginning of the transient caused by $R_s$, and the parasitic capacitance of the coaxial cable (connecting $R_s$ and Oscilloscope) in parallel with the input capacitance of the Oscilloscope (25pF), the value of $R_s$, needed to be as small as possible.

The down side is that the voltage drop across $R_s$ reduces with the $R_s$ but needs to be higher than the resolution of the Oscilloscope (2mV/div) otherwise the response is very noisy even with the averaging function (32 samples per one data point). Also to maximise the voltage drop the devices with the longest width (600 microns) and highest current were used. Unfortunately these devices were designed only for one s-d separation ~6 microns and we were unable to use devices with shorter s-d separation. In Fig.10.4a the response is shown ($V_D = 0V$) for different values of $R_s$. It can be seen that with decreasing $R_s$ value down to 91Ω the duration of the first sharp transient

Fig. 10.4 a) Transient at $V_D = 0V$ for different values of $R_s$ b) equivalent circuit explaining the second feature in the transient ($V_D = 0V$).
gets smaller and the response is noisier. The second feature in the transient is almost unchanged and is associated with SGT device and can be better understood in connection with equivalent circuit Fig.10.4b.

In the first instant when the pulse $V_g \rightarrow 10V$ is applied, the source barrier will be reverse biased and deplete the a-Si:H to the interface. Therefore the barrier will be pulled down and the current charging the $C_g$ will be high. However with increasing time $C_g$ charges and the reverse voltage on the barrier falls so the depletion layer withdraws towards its equilibrium value, the effective barrier height rises and the gate charges more slowly until $C_g$ is fully charged to 10V and there is no voltage across the barrier. This situation results in the second feature in the transient response when $V_d = 0V$ where the first sharp transient and second slow (due to the SGT) superimpose on each other resulting in the “bump”. Fortunately in most transistor circuit situations there is a drain voltage across the transistor when it is switched off so this situation is rather academic.

The SGT transient response for frequencies of 1kHz, 10kHz, 100kHz and 200kHz is shown in

![Fig. 10.5 SGT transient response for frequencies a) 1kHz, b) 10kHz, c) 100kHz and d) 200kHz](image)

$(d = 6\mu m, s = 5\mu m, w = 600\mu m$ and Phosphorus dose $4 \times 10^{14}$ cm$^{-2}$).
Fig. 10.5 measured with $R_s = 91\Omega$ ($V_G = 10\text{V}$ and $V_D = 10\text{V}$). Also the transients for $V_D = 0\text{V}$ are shown. Transient responses measured in Fig. 10.5 clearly show that these SGT devices are able to operate well in excess of 200kHz. Obviously if the duration of the initial sharp transient was too long then it would be impossible to estimate the turn-on time. The extracted turn-on time $\tau_{ON}$ ($V_D = 10\text{V}$) was for this device $\sim 3.7 \times 10^{-7} \text{s}$ (see Fig. 10.6). However the estimation of turn-off time ($\tau_{OFF}$) is more difficult due to the sharp transient during the discharge of the device and the parasitic capacitances. But one might guess that this value will be surely shorter than $\tau_{ON}$ because now ($V_G \rightarrow 0\text{V}$) electrons can rapidly diffuse from the S-I interface to the source Schottky barrier which will be forward biased. The delay and saturation time appeared to be very short (<5ns).

The comparison of the transient response for SGT and FET device with the same dimensions ($w = 600$, $d = L = 6\mu\text{m}$, $s = 5\mu\text{m}$) is shown in Fig. 10.7 for the frequency of 500kHz. Clearly both responses are experiencing the sharp transient caused by the circuit arrangement. However in the FET case the second “bump” ($V_D = 0\text{V}$) is not present and first sharp transient is therefore wider. Both devices are able to operate at 500kHz but the SGT has a higher $\tau_{ON}$ estimated above. For FET it is difficult to estimate the $\tau_{ON}$ because that region is overshadowed by the initial transient but one might expect shorter $\tau_{ON}$ (factor of 2) due a higher $g_m$ and lower drain capacitance.
Chapter 10. Transient response

(a) SGT
(b) FET

Fig. 10.7 a) SGT and b) FET device transient response for 500kHz also showing the case for \( V_n = 0V \).

10.2.3 Calculated turn-on and turn-off time

For the SGT device shown above it is possible very simply to calculate the turn-on and -off time from the measured transfer characteristics and SGT device geometry using Eq.10.1 above. One can assume that the \( t_{ON} \) and \( t_{OFF} \) time are similar as charging and discharging time \( t \). The transconductance \( g_m \) was derived from the transfer characteristics for \( V_D = 10V \) (and \( V_D = 10V \)). The value of \( g_m \) was measured to be \( 1.8 \times 10^{-6} \text{ S} \) (for 600um width). The total capacitance \( C \) was calculated to be \( 1.4 \text{ pF} \) which gives us the value of \( t \approx 7.6 \times 10^{-7} \text{ s} \). However if we consider only the source gate overlap we would get \( t \approx 3.8 \times 10^{-7} \text{ s} \). The values \( C \) and \( g_m \) used in these calculations as well as results are shown following Table 10.1. Further the calculated values of \( t \) for the FET device are shown. It might be seen that the charging times for the FET are approximately 4 times faster (for the same device geometry \( d = L \)). This is mainly due to the higher transconductance and drain current of the FET in comparison with the SGT.

Table 10.1 Calculated values of charging times for SGT and FET.

<table>
<thead>
<tr>
<th>Device</th>
<th>( g_m ) [S]</th>
<th>( C ) [pF]</th>
<th>( t ) [s]</th>
</tr>
</thead>
<tbody>
<tr>
<td>SGT ( w = 600\mu m ) ( d = 6\mu m ) ( s = 5\mu m )</td>
<td>( 1.8 \times 10^{-6} )</td>
<td>( 0.7 ) (area 600 x 5( \mu m ))</td>
<td>( 3.8 \times 10^{-7} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 1.4 ) (area 600 x 11( \mu m ))</td>
<td>( 7.6 \times 10^{-7} )</td>
</tr>
<tr>
<td>FET ( w = 600\mu m ) ( L = 6\mu m )</td>
<td>( 7.7 \times 10^{-6} )</td>
<td>( 0.7 ) (area 600 x 5( \mu m ))</td>
<td>( 1 \times 10^{-7} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( 1.4 ) (area 600 x 11( \mu m ))</td>
<td>( 1.8 \times 10^{-7} )</td>
</tr>
</tbody>
</table>
Chapter 10. Transient response

Another way of estimating the charging time for SGT is to use its model and Eq.8.2 for $g_m$ and assuming that the main contribution to the $\tau$ is from the capacitance underneath the source $C_g$ ($C_g = C_G S$ where $C_G$ is the gate capacitance per unit area) and neglecting the parasitic FET for short s-d separation. Then the small signal charging time $\tau$ will be as follows

$$\tau = \frac{C_g}{g_m} = \frac{\varepsilon_0 \varepsilon_r k T (C_g + C_G) C_g S}{q I_s \alpha C_g C_g} = \frac{\varepsilon_0 \varepsilon_r k T (C_g + C_G)}{q I_s \alpha C_g}$$

(10.2)

where $J_S$ is the current density across the source. Next assuming that $C_S >> C_G$ one can write Eq.10.2 as follows

$$\tau = \frac{\varepsilon_0 \varepsilon_r k T}{q J_S \alpha \alpha}$$

(10.3)

Using Eq.10.3 and values for the SGT device measured above ($J_S = 2.5 \times 10^9$ A/um$^2$, for $V_G = 10$V) we get the charging time $\tau \sim 2.6 \times 10^{-7}$s. In the case of Eq.10.2 when one has to also consider $C_G$ the charging time is higher $\tau \sim 3.1 \times 10^{-7}$s. In view of the fact that we are using a small signal charging time approximation to a large signal transient, these results of $\tau$ are in good agreement with the value of $\tau$ measured experimentally (Fig.10.6).

10.3 Simulated transient response

Silvaco ATLAS device simulator enables us to perform a simulation of transient response. The simulation of the transient response of a SGT device with the same geometry and barrier as used in experimental part above ($t_{SiN} = 300$nm, $w_{Si} = 100$nm, $s = 5$um, $d = 6$um) is shown in Fig.10.8.

Fig. 10.8 The simulated transient response for a SGT (200kHz square wave) with $\Phi_a = 0.5$eV (black) and 0.49eV (red), $d = 6$um and $s = 5$um.
Chapter 10. Transient response

The simulated transient response is plotted for two different barrier 0.5eV and 0.49eV which give source current densities similar to that measured in Fig.10.6. The value of drain current density $J_s$ in saturation was $\sim 2.6 \times 10^9 A/\mu m^2$ and $\sim 3.1 \times 10^9 A/\mu m^2$ for 0.5eV and 0.49eV, respectively. The simulated response is for a 200kHz square waveform on the input (gate) with amplitude of 10V and no DC offset. The drain electrode bias was 10V.

Extracted turn-on and -off times are shown in Table 10.2. The estimated $\tau_{ON}$ was $\sim 7.7 \times 10^7 s$ and $\sim 6 \times 10^7 s$ for 0.5eV and 0.49eV barrier height respectively. On the other hand the turn-off time $\tau_{OFF}$ was very similar for both devices $\sim 1.5 \times 10^7 s$ and $1.8 \times 10^7 s$. The turn-off time is significantly faster, as mentioned above, the electrons now diffuse very fast from the S-I interface to the source barrier which becomes forward biased and due the fact that in saturation the electron concentration underneath the source barrier as well as in the parasitic FET is very low. Therefore it is seen that to switch the SGT device off takes significantly ($\sim 4$ times) less time than to turn it on.

**Table 10.2 The switching times extracted from simulation shown in Fig.10.3.**

<table>
<thead>
<tr>
<th>barrier</th>
<th>$\tau_{ON} [s]$</th>
<th>$\tau_{OFF} [s]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.49eV</td>
<td>$6 \times 10^7 s$</td>
<td>$1.5 \times 10^7 s$</td>
</tr>
<tr>
<td>0.5eV</td>
<td>$7.7 \times 10^7 s$</td>
<td>$1.8 \times 10^7 s$</td>
</tr>
</tbody>
</table>

The values for turn-on time are very similar to those calculated above (calculated was $\sim 7.6 \times 10^7 s$ for area 600x11um Table 10.1) and a factor of two higher than experimentally measured ($\sim 3.7 \times 10^7 s$). This suggests that there is fair agreement between the calculated, simulated as well as experimental results. The various values of $\tau$ are shown in Table 10.3.

**Table 10.3 Estimation values of the transient response charging time for device shown in Fig.10.6.**

<table>
<thead>
<tr>
<th>Calculated $\tau [s]$ using</th>
<th>Simulated $\tau [s]$ by ATLAS</th>
<th>Experiment $\tau [s]$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$s = 5 \mu m$</td>
<td>$d = 6 \mu m$</td>
<td>$C_s &gt;&gt; C_o$</td>
</tr>
<tr>
<td>$3.8 \times 10^7 s$</td>
<td>$7.6 \times 10^7 s$</td>
<td>$4.1 \times 10^7 s$</td>
</tr>
</tbody>
</table>

Pleased by the good agreement between the various methods we were spurred on to use ATLAS simulations to predict conditions that would give response times sufficiently low for MHz operation. The simulation of the transient response of a SGT device for different s-d separation
and 0.4eV barrier height can be seen in Fig.10.9. The simulated response is for 1MHz square waveform on the input (gate) with an amplitude of 10V and no DC offset.

The drain electrode bias was 10V. The device had the $s = 5$ microns and s-d separation was varied (0.5, 2 and 4 microns). The layer thickness of a-Si:H and SiN was 100nm and 300nm respectively. With decreasing s-d separation the transit time gets shorter as expected. The extracted turn-on time for the SGT device ($d = 0.5um$) is only $\sim 4.5 \times 10^{-8}s$ on the other hand for longer device ($d = 4um$) this increases to $\sim 7 \times 10^{-8}s$. The $\tau_{on}$ for $d = 6um$ and barrier of 0.4eV was $\sim 1 \times 10^{-7}s$ (not shown here). It is seen that for all of these devices a digital circuit would operate well above 1MHz.

![Fig. 10.9 Simulations showing transient response of SGT device for various s-d separations ($V_D = 10V$).](image)

Another way to increase the drain current and transconductance is to use thinner layers of a-Si:H and SiN. As shown in chapter 7, decreasing the thickness either of a-Si:H or SiN leads to an increase of drain current in the SGT device. In Fig.10.10 the simulated transient response is shown for two different source barriers (0.45eV and 0.5eV) and two frequencies of input signal (200kHz and 1MHz). The amplitude of the input square waveform signal was again 10V and $V_D = 10V$. The device had a source length $s = 5$ microns and s-d separation of 1 micron. The layer thickness of a-Si:H and SiN was 40nm and 120nm respectively. The value of drain current density $J_s$ reached in saturation was $\sim 3.9 \times 10^{-8}A/\mu m^2$ and $\sim 7.6 \times 10^{-9}A/\mu m^2$ for the 0.45eV and 0.5eV barrier, respectively. The transient response at 200kHz is shown in Fig.10.10a. It is seen that both devices easily to operate at 200kHz with turn-on time $\tau_{on} \sim 1.4 \times 10^{-7}s$ (0.45eV) and $\sim 4.5 \times 10^{-7}s$ (0.5eV). The turn-off time is the same for both cases $\tau_{off} \sim 1 \times 10^{-8}s$. These results show that it is the barrier height and the current density that controls the speed of response as indeed is indicated by Eq.10.3.
Chapter 10. Transient response

Fig. 10.10 Simulated transient response for two different source barriers of 0.45eV (red) and 0.5eV (black) and two frequencies of input signal a) 200kHz and b) 1MHz.

Computer simulations indicate that it should be possible to operate SGT devices in a-Si:H above 1MHz but the source barrier height needs to be < 0.45eV.

10.4 Chapter summary

This chapter focuses on the transient response of the SGT and FET devices. Due to the source barrier the current through the SGT is always lower than that of a FET with the same s-d separation and layer thicknesses. The transient response of the FET is therefore faster. Measurement of the transient response of a SGT is found to be in good agreement with values calculated using various approaches and also with simulation using ATLAS. It is shown that the transient response of a SGT can be sufficiently fast for a circuit to operate well above 1MHz but the source barrier needs to be <0.45eV.

Interestingly, it might be possible to create a SGT with faster transient response than a FET. This is because to obtain the highest frequencies the device dimensions have to be reduced and the SGT shows very much smaller short channel effects. Therefore smaller SGT devices operating at higher frequencies whilst retaining good output characteristics should be achievable (see section 7.3).
Chapter 11

11 Small signal response of the SGT

11.1 Introduction

The frequency limitations of transistor devices are dependent on device geometry and material properties. Throughout this work we are concerned with SGT’s prepared in a-Si:H where the mobility is very low. The potential to deposit a-Si:H over a large area creates a very interesting application area because analogue circuits could be prepared on a large scale. The reason why analogue electronics has not been developed in a-Si:H so far is due to the rapid degradation in performance of FET devices. The stability issues (on-current and $\Delta V_{TH}$ shift) are discussed in chapter 9, where it was shown that SGT devices are very much more stable than the FET. We believe that there are many possibilities to successfully develop this field of large area analogue electronics using SGT devices in a-Si:H instead of conventional thin-film FET’s.

Useful oscillators and amplifiers in a-Si:H requires that transistor performance will not significantly change during operation thus giving a stable and reliable circuit function. Also applications such as on-pixel amplifier could be realized that play an important role in X-ray scanners and imagers. The ongoing issue in the X-ray imagers is that there is strong need to amplify the small signal coming from a X-ray detector before this signal is read-out by scanning electronics [69] so as to increase the signal-to-noise ratio. Consequently the image quality (higher contrast and better resolution) should be better than arrays without pre-amplification of the signal. Also flat panel X-ray imagers using amorphous silicon technology applied in digital radiography of the skeleton might replace conventional skeletal radiography without loss of image quality even at a dose reduction of up to 50% [70].

In this chapter, the possibility of using SGT device in analogue electronics is examined through the discussion of the simulated small signal frequency response. An equivalent circuit of the SGT device is proposed in order to obtain an indication of which circuit elements are important. Next the influence of SGT device parameters and geometry on device RF performance is simulated using ATLAS to obtain $f_T$ and $f_{MAX}$. We will be mainly interested in SGT transistor with grounded source or common-source arrangement, which is the circuit most frequently used with field-effect devices in connection with amplifier circuits.

11.2 SGT device equivalent circuit

Before the SGT device RF capability can be discussed the SGT device equivalent circuit should be decided upon. Generally one might expect this equivalent circuit to be similar to a FET (MOSFET) considering the fact that the mutual conductance is controlled by an insulated gate. The equivalent circuit is shown in Fig.11.1.

![Fig. 11.1 Small signal equivalent circuit for a SGT device in saturation.](image)

The circuit elements in the intrinsic SGT model are capacitances of the insulator $C_g$ and voltage dependent $C_t$ of the semiconductor under the source and the source barrier resistance $1/g_m$. The $C_{GD}$ represents the feedback capacitance which is mainly due to the overlap of the gate with the extrinsic drain region of length $d$ that forms the parasitic FET (see Fig.6.4) and $R_{DS}$ the dynamic output impedance of the gated source. The $R_{DS}$ is parallel with the voltage controlled current source $g_m V_i$. The parasitic FET channel resistance of the FET is $R_{dp}$ ($\sim 1/g_{dp}$) and $V_i$ is the input signal voltage.

An important figure of merit to describe transistor RF performance is the cut-off frequency $f_T$. The $f_T$ is defined as the frequency at which the current through $C_g$ is equal to that of the current source $g_m V_i$ in the intrinsic device (i.e. without parasitic series resistances). In other words it is equal to the frequency at zero current gain [71]. For this equivalent circuit $f_T$ can be approximated by

$$f_T = \frac{g_m}{2\pi(C_g + \frac{1}{g_m})} = \frac{1}{2\pi\tau}$$

(11.1)
Where \( g_m/C_e \) is the small signal response time similar to Eq.10.1.

The maximum oscillation frequency \( f_{\text{MAX}} \) is a characteristic of the “extrinsic” device. The \( f_{\text{MAX}} \) is defined as the frequency at which the unilateral power gain (UPG) of the transistor is equal to unity under optimum matching conditions for the input and output impedances [42].

\[
UPG(f) = \frac{1}{f = f_{\text{MAX}}} \tag{11.2}
\]

where UPG is defined using \( y \) (admittance) parameters [72] as

\[
UPG = \frac{|y_{12} - y_{21}|^2}{4(\text{Re}[y_{11}]\text{Re}[y_{22}] - \text{Re}[y_{12}]\text{Re}[y_{21}])} \tag{11.3}
\]

11.3 Simulated small signal response

Note that all simulations of small signal response performed using ATLAS Silvaco were done for ideal matching conditions where both input impedance and load impedance were 50\( \Omega \) (without any reactance part). This allowed us to determine the optimum possible SGT and FET device operation.

In the Fig.11.2 the simulated small signal response is shown for two different source barriers (0.45eV and 0.5eV) and the same device geometry. This device geometry was the same as in the previous chapter 10, concerned with transient response (Fig.10.10). The device had \( s = 5 \) microns and a s-d separation of 1 micron. The layer thicknesses of the a-Si:H and SiN was 40nm and 120nm respectively. The DC bias point was \( V_D = 10V \) and \( V_G = 10V \).

![Fig. 11.2 Small signal response for a SGT device with a barrier height of a) 0.45eV and b) 0.5eV.](image)

It can be seen that the frequency \( f_r \) is \( \approx 1.49\text{MHz} \) and \( \approx 290\text{kHz} \) for barrier heights of 0.45eV and 0.5eV, respectively. If we try to calculate the \( f_r \) from the charging time (\( \tau_{\text{OV}} \) extracted in previous
chapter) and using Eq.11.1 we get similar results of 1.14MHz and 354kHz showing good agreement and link between the transient and small signal response simulations. This gives us more confidence in the SGT device small signal response simulations where we can try more ambitious device geometries. In the case of $f_{\text{MAX}}$ the expected values increase from 6.2MHz to 25MHz as the barrier height is decreased from 0.5eV to 0.45eV.

It might be seen that the $f_T$ is mainly dependent (Eq.11.1) on transconductance $g_m$ and the situation is similar to that in previous chapter where there was the need to maximize the current in order to get a fast transient response. Obvious ways to increase the current are to modify the source barrier height and source length. Improvement in current handling is also possible to achieve by reducing the semiconductor thickness (shown in chapter 7.). There should also be an improvement in RF response if the capacitance of the parasitic FET is reduced by reducing s-d separation or increasing drain voltages. These possibilities will be explored in the following section. It is also very important to mention that all these simulations were done in the context of the unique SGT features of low saturation voltage and high output impedance.

Note that in chapter 9. the potential and electron concentration profiles were shown for s-d separation less than 2um (Fig.9.6). There, a suggestion was made that when $V_D > V_G - V_T$ we achieve the situation where the parasitic FET channel is depleted resulting in smaller capacitances and shorter transit time [58]. This situation is simulated in figure 11.3 where the frequency $f_T$ is extracted from simulations and plotted as a function of drain voltage. There are four curves each is for a SGT device of different geometry and the same barrier height 0.4eV. The source length was 2 or 4 microns and s-d separation 1 or 2 microns. The layer thickness of the a-Si:H and SiN was 100nm and 300nm respectively.

![Fig. 11.3 $f_T$ plotted as a function of drain voltage for different SGT device geometry ($\Phi_b = 0.4eV$).](image)

Above $V_{\text{SAT}} (-2.5V)$ $f_T$ rises with drain voltage in all cases (Fig.11.3) presumably due to a decrease in the parasitic FET capacitance as suggested above. There is also a small increase in $f_T$ as $d$
decreases from 2 to 1 micron. The small change suggests that it is the charging time of the source capacitance that mainly controls $f_T$. Surprisingly the $f_T$ reduces with increasing source length and increasing current. However this effect arises because there is a current crowding at the edge of the source as shown in Fig.11.4 and in the simulations Fig.7.4. Therefore the $g_m$ at the edge ($X_2$) of the source is much higher than it is further away from the edge and response time is much shorter. Therefore reducing the source length increases $f_T$ by removing the slower regions of the source.

![Fig. 11.4 Schematic diagram of SGT device showing the origin of slow small signal response and transient for longer sources.](image)

Using various combinations of geometric parameters of SGT devices and barrier heights one can optimise small signal response in order to achieve the optimal $f_T$ (and also transient response). The results of these simulations are shown in Table 11.1.

From the Table 11.1 one can get the relationships between the geometric parameters, barrier heights and cut-off frequency as follows:

a) $\Phi_B \downarrow \rightarrow J_S \uparrow \rightarrow f_T \uparrow$ (for lower $\Phi_B$, the $J_S$ will be higher resulting in higher $f_T$)

b) $t_{a-Si} \downarrow \rightarrow J_S \uparrow \rightarrow f_T \uparrow$

c) $t_{SiN} \downarrow \rightarrow J_S \uparrow \rightarrow f_T \uparrow$

d) $V_D \uparrow \rightarrow C_{FET} \downarrow \rightarrow f_T \uparrow$ ($C_{FET}$ is the capacitance of the parasitic FET)

e) $d \downarrow \rightarrow C_{FET} \downarrow \rightarrow f_T \uparrow$

Knowing the relationships between the parameters of SGT devices and $f_T$ gives the possibility to design SGT device capable of fast operation. The $f_T$ of devices with sub-micron s-d separation and low barrier heights are shown in Table 11.2 ($V_G = 10V$).
Table 11.1 $f_T$ extracted from simulations for different SGT geometries and barrier heights ($V_G=10V$).

<table>
<thead>
<tr>
<th>Barrier height [eV]</th>
<th>Source length [um]</th>
<th>$d$ [um]</th>
<th>a-Si/SiN thickness [nm]</th>
<th>$f_T$ [MHz] @ $V_D=1V$</th>
<th>$f_T$ [MHz] @ $V_D=5V$</th>
<th>$f_T$ [MHz] @ $V_D=10V$</th>
<th>$f_T$ [MHz] @ $V_D=15V$</th>
<th>$f_T$ [MHz] @ $V_D=20V$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.4</td>
<td>2</td>
<td>1</td>
<td>100/300</td>
<td>0.8</td>
<td>3.4</td>
<td>4.32</td>
<td>4.52</td>
<td>4.58</td>
</tr>
<tr>
<td>0.4</td>
<td>2</td>
<td>2</td>
<td>100/300</td>
<td>0.51</td>
<td>2.9</td>
<td>3.9</td>
<td>4.23</td>
<td>4.35</td>
</tr>
<tr>
<td>0.4</td>
<td>4</td>
<td>1</td>
<td>100/300</td>
<td>1</td>
<td>2.73</td>
<td>3.3</td>
<td>3.4</td>
<td>3.42</td>
</tr>
<tr>
<td>0.4</td>
<td>4</td>
<td>2</td>
<td>100/300</td>
<td>0.9</td>
<td>2.05</td>
<td>2.92</td>
<td>3.1</td>
<td>3.15</td>
</tr>
<tr>
<td>0.4</td>
<td>2</td>
<td>2</td>
<td>25/100</td>
<td>3.7</td>
<td>7.6</td>
<td>9.9</td>
<td>10.95</td>
<td>11.1</td>
</tr>
<tr>
<td>0.4</td>
<td>4</td>
<td>2</td>
<td>25/100</td>
<td>3.4</td>
<td>6.2</td>
<td>7.05</td>
<td>7.3</td>
<td>7.4</td>
</tr>
<tr>
<td>0.45</td>
<td>2</td>
<td>2</td>
<td>25/100</td>
<td>0.95</td>
<td>1.42</td>
<td>1.84</td>
<td>1.96</td>
<td>1.97</td>
</tr>
<tr>
<td>0.45</td>
<td>4</td>
<td>2</td>
<td>25/100</td>
<td>0.96</td>
<td>1.46</td>
<td>1.72</td>
<td>1.79</td>
<td>1.8</td>
</tr>
<tr>
<td>0.45</td>
<td>5</td>
<td>1</td>
<td>40/120</td>
<td>0.72</td>
<td>1.34</td>
<td>1.49</td>
<td>1.52</td>
<td>1.53</td>
</tr>
<tr>
<td>0.5</td>
<td>5</td>
<td>1</td>
<td>40/120</td>
<td>0.125</td>
<td>0.25</td>
<td>0.29</td>
<td>0.295</td>
<td>0.296</td>
</tr>
</tbody>
</table>

Table 11.2 $f_T$ extracted from simulations for sub-micron SGT geometries and low barrier height.

<table>
<thead>
<tr>
<th>Barrier height [eV]</th>
<th>Source length [um]</th>
<th>$d$ [um]</th>
<th>a-Si/SiN thickness [nm]</th>
<th>$f_T$ [MHz] @ $V_D=1V$</th>
<th>$f_T$ [MHz] @ $V_D=5V$</th>
<th>$f_T$ [MHz] @ $V_D=10V$</th>
<th>$f_T$ [MHz] @ $V_D=15V$</th>
<th>$f_T$ [MHz] @ $V_D=20V$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.4</td>
<td>2</td>
<td>0.5</td>
<td>40/120</td>
<td>3.77</td>
<td>8.36</td>
<td>9.84</td>
<td>10.5</td>
<td>10.8</td>
</tr>
<tr>
<td>0.4</td>
<td>2</td>
<td>0.5</td>
<td>25/100</td>
<td>7.4</td>
<td>9.42</td>
<td>10.65</td>
<td>10.94</td>
<td>10.97</td>
</tr>
<tr>
<td>0.4</td>
<td>1</td>
<td>0.25</td>
<td>25/100</td>
<td>9.7</td>
<td>11.96</td>
<td>12.92</td>
<td>13.0</td>
<td>13.05</td>
</tr>
<tr>
<td>0.35</td>
<td>1</td>
<td>0.25</td>
<td>25/100</td>
<td>33.2</td>
<td>55.7</td>
<td>60.5</td>
<td>61.0</td>
<td>61.1</td>
</tr>
</tbody>
</table>

From Table 11.2 can be seen that it is possible to operate SGT device of sub-micron dimensions with cut-off frequencies above 10MHz and for the lowest barrier of 0.35eV the $f_T$ is even as high as 60MHz. These results are even more attractive considering the fact that the SGT output characteristics for these sub-micron dimensions (s-d separation is only 250nm, s = 1um) are good.
with low saturation voltage and high output impedance (see Fig.7.10a). Obviously the saturation is less well defined and the output impedance is not as high as for high barrier devices (Fig.6.3) but it very much better than that of a FET (Fig.7.10b). The FET characteristics for a channel length \( L = 250\text{nm} \) show rapid deterioration of device performance and lack of saturation due to short channel effects. These results showing great potential for the SGT but it requires sub-micron technology and control of low source barriers.

Another factor influencing the small signal performance is gate voltage. Increasing the gate voltage increases the electric field, the barrier is pulled down further and the higher number of electrons crosses the barrier. This increases the device current and the transconductance as well. As we know that transconductance is directly proportional to the cut-off frequency (Eq.11.1) Therefore we expect a higher \( f_r \) for higher \( V_G \). This relationship is indeed shown in the next figure (Fig.11.5) where cut-off frequency is plotted as a function of gate voltage for two different drain voltages (5V and 10V). These curves correspond to SGT device shown in Fig.7.10a. The curves shown in Fig.11.5 have remarkably similar features to transconductance curves plotted against gate voltage shown previously (see Fig.8.2b).

![Cut-off frequency plotted as a function of gate voltage for two different drain voltages 5V and 10V.](image.png)

Here we can apply the same analysis as for the transconductance and the same explanation for the bump in the curves, caused by the parasitic FET in series with the gated source. For voltages around the threshold voltage of the parasitic FET, the FET controls the current and the transconductance and cut-off frequency increase linearly. However as a gate voltage is increased further the current becomes controlled by the source barrier. Then the \( g_m \) and cut-off frequency increase slowly with the gate voltage. Hypothetically had there been an ohmic source contact the cut-off frequency would follow the green line in the plot for the FET but as shown in Fig.7.10 the output characteristics of the FET are very poor and probably of little use.
11.4 Chapter summary

In this chapter simulations of the small signal response of a SGT using ATLAS Silvaco were presented. Even though all simulations were performed under the ideal matching conditions i.e. both input impedance and load impedance were 50Ω the SGT devices show great potential for practical applications. Simulations showed that one might expect SGT operation as high as 60MHz. The dependence of cut-off frequency was discussed showing that it strongly depends on device geometry and barrier height. Also the complex relationship between $f_T$ and source length of the SGT was discussed. The close link between the transient response and small signal response was presented comparing the calculated values of $f_T$ using the turn-on time from transient response and extracted values of $f_T$ from simulated small signal performance. This underlines the fact that one might optimise the SGT device in both areas at once. Finally the dependence of cutoff frequency on the gate voltage was demonstrated which has a very similar behaviour as device transconductance vs. gate voltage.

In a real situation, however, the circuit operation frequency will be worse. Similarly as for the transient response extrinsic and parasitic circuit elements (resistances, capacitances) will seriously affect the optimum performance even if we achieve a good impedance match between the input and output of the device and circuit.

Furthermore we have tried to perform small signal analysis on our existing SGT devices but these attempts were not successful for a couple reasons. The first was that SGT devices have very high input and output impedance resulting in impedance mismatch with the network analyser, which has 50Ω input and output impedance. This situation results in measurement where the reflection coefficients are too high giving negligible current gain. The solution will be to design impedance matching circuits for input and output and then perform the small signal analysis. The second issue was that measurements were done using a standard probe kit without low capacitance probes which were not available.
12 Comparison between SGT and FET in a-Si:H

12.1 Introduction

In this chapter the properties of a SGT device are summarized and compared with a FET for the same semiconductor and insulator layer thickness. To some extent the proper comparison is quite difficult to make especially because short-channel effects are much reduced in a SGT so very small structures can be made whilst preserving good output characteristics. The SGT is superior to the FET in many regards, but on the other hand from the previous two chapters one can guess that the FET has some advantages over the SGT in some cases.

12.2 Properties of SGT and FET devices

SGT devices have a different geometry and principle of the operation than the FET and therefore their electrical characteristics are very different from those of a standard FET prepared by thin-film technology in a-Si:H.

12.2.1 Saturation voltage

The direct consequence of the different device construction is the lower saturation voltage for SGT's. The major difference is that the current saturation in the FET occurs when the drain end of the channel is depleted while in a SGT saturation occurs when the source is depleted by the reverse biased source barrier. If the semiconductor layer is thin and lightly doped then the saturation voltage is very small and its change with gate voltage can be more than ten times lower than that of an equivalent FET (i.e. see Fig.6.13 or Fig.7.7). Under these conditions when the
semiconductor is depleted the structure behaves as two dielectrics in series with the electric field at the source barrier controlled by the gate voltage.

12.2.2 Output impedance

The physical processes that determine the output impedance of a SGT are very different from those in a FET. In the SGT the impedance is controlled by field penetration from the drain towards the source barrier when a drain voltage is applied. In the FET there is an effective shortening of the channel with drain voltage, which increases the conductivity of the channel. In the SGT, however, the source is screened by the close proximity of the gate (see Fig.6.16). Therefore the SGT is much less sensitive to the drain field than the FET, which is manifested as a much better output impedance (Fig.6.15). This comes about because of the change in geometry compared to the FET [2].

As previously said the saturation voltage can be very much smaller and current after the saturation is very flat (Fig.6.9) therefore the device can be operated in saturation due to its very high output impedance at lower drain voltages giving less power dissipation than a conventional FET (Fig.4.3). The power dissipation is an important issue in some applications such as OLED active matrix displays where up to 50% of the total power dissipation occurs in the drive FET transistors [73].

12.2.3 Saturated drain current

Source-Gated Transistors are devices in which the on-current is determined by a reverse biased source barrier located opposite a gate electrode [1]. Changing the gate potential affects the magnitude of the electric field at the source barrier and thereby the magnitude of the current flowing through the reverse biased barrier. Therefore the magnitude of the current in SGT devices will always be affected by the source barrier and will be smaller than for conventional FET having the same layer thickness and dimensions. However using ion implantation it is possible to modify the effective barrier height and increase the drain current close to the FET limit (shown in chapter 6., Fig.6.10). Furthermore due to less short channel effects the SGT can operate with smaller s-d separations.

12.2.4 Short channel effects

On the other hand the magnitude of the drain current does not depend on s-d separation due to SGT geometry and concept (Fig.7.1). This leads to improved characteristics and immunity to short channel effects at sub-micron s-d separations as shown by simulations in the chapter 7. (see
Chapter 12. Comparison between SGT and FET in a-Si:H

Fig. 7.10. Here the examples of the SGT devices with the shortest s-d separations prepared in a-Si:H and barrier modification implant of $2\times10^{14}$ cm$^{-2}$ are shown in Fig. 12.1.

(a) (b)

Fig. 12.1 Photographs of “short channel” SGT devices with a) $d = 1.1$ and $w = 3.6$ microns (dry etched) b) $d = 1.2$ and $w = 1.4$ microns (wet etched).

The layer thickness of a-Si:H and SiN was 100 nm and 300 nm respectively. In Fig. 12.1a the SGT device has the $w \sim 3.6$ microns, $s \sim 5.5$ microns and s-d separation of $\sim 1.1$ micron. The definition of the source and drain electrodes was done by reactive ion dry etching (RIE). This device was prepared as a symmetrical device where the source length and gate-drain overlap should be of similar length. This is due to fact that in this case the mask set for the conventional FET devices was used. The device in Fig. 12.1b has the $w \sim 1.4$ microns, $s \sim 6.5$ microns and s-d separation of $\sim 1.2$ micron. The definition of the source and drain electrodes (Al, Cr) was wet etched. The second device shows asymmetry of the contacts due to lithography alignment offset in some cases done intentionally in order to investigate the influence of the source length on the device current (shown in chapter 7., Fig. 7.3).

The corresponding SGT transistor characteristics for devices shown above are plotted in Fig. 12.2. It is seen that both devices show low saturation voltage $\sim 1.8$V which is in good agreement with dielectric model [1] and a high output impedance.
Chapter 12. Comparison between SGT and FET in a-Si:H

Fig. 12.2 SGT output characteristics of the SGT devices with (a) $d = 1.1$ and $w = 3.6$ microns (dry etched) (b) $d = 1.2$ and $w = 1.4$ microns (wet etched) corresponding to Fig. 12.1.

The output impedance in these devices is not as high as in previous cases (see Fig. 6.9). The reason can be seen in the next figure (Fig. 12.3) where the transfer characteristic of the SGT device is shown (Fig. 12.3a).

Fig. 12.3 a) SGT transfer characteristics $d = 1.2$ and $w = 1.4$ microns (wet etched) corresponding to Fig. 12.1b and b) leakage current plotted as a function of drain voltage showing problems with compensating BF$_2$ implant.

It can be seen that with increasing of the drain voltage for negative $V_G$ the leakage current is increasing as well. This situations leads to drain current increase beyond its normal saturated value and decreasing of the output impedance with $V_D$. The reason for the higher leakage current lies within the problem with the compensating implant where in this case the ion dose was too low or the activation of the acceptors was not sufficient and there are still uncompensated phosphorous donors remaining. Therefore the region near the semiconductor surface behaves as
an additional resistance, parallel to the “channel”, through which the additional current flows. This is depicted in Fig.12.3b where the leakage current is linearly increasing with drain field (voltage) and the leakage conductance of the compensated region is $4 \times 10^{-11}$ S. The total conductance (parallel configuration) of the parasitic channel and leakage was estimated from the transistor characteristics to be $\sim 1.55 \times 10^{-10}$ S for ($V_G = 10$V) resulting in a parasitic channel conductance of $\sim 1.15 \times 10^{-10}$ S.

### 12.2.5 Voltage gain

The mutual conductance or transconductance $g_m$ depends mainly on drain current through the device. Therefore the transconductance is smaller in the SGT than in the FET due to barrier which constricts the current at the source. On the other hand the SGT channel conductance $g_d$ which is inversely proportional to the output impedance is much lower than that of FET due to the specific construction of the SGT device (Fig.6.15). Hence the voltage gain which is defined (Ref. [68]) as:

$$A_v = \frac{g_m}{g_d}$$

will be much higher for the SGT than FET.

In Fig.12.4a the voltage gain of the simulated SGT device for different gate voltages plotted as a function of drain voltage is shown. The layer thickness of a-Si:H and SiN was 40 nm and 120 nm respectively. The device has the barrier height of 0.45eV, $s = 5$ microns and $s-d$ separation of 1 micron.

![Fig. 12.4 a) Voltage gain of the simulated SGT device for different gate voltages and plotted as a function of $V_m$. b) Experimental results of the voltage gain for devices with a barrier height modified by ion implantation (phosphorous dose) also plotted as a function of $V_D$ ($V_G = 10$V).](image)
Chapter 12. Comparison between SGT and FET in a-Si:H

It is seen that voltage gain is higher for higher values of \( V_d \) due to depletion of the parasitic FET and pinch-off at the drain as well as the source. Interestingly but not unexpectedly the voltage gain is decreasing with \( V_d \) despite higher transconductance. This is caused by the increase in the current and a decrease in the output impedance. We see that for the highest current devices where the current is similar to the FET the voltage gain is approximately a factor of 5 higher for the SGT compared to the FET.

12.2.6 Dynamic range

Another feature of these SGT devices is the small dynamic range over which they operate. For example in Fig.12.2 changing the gate voltage from 4V to 10V increases the current by only a factor ~3. Whilst a small dynamic range is not important in some circuits, in others it is prohibitive. An obvious way of increasing both the dynamic range and the current at low gate voltages is to increase the capacitance of the gate dielectric. It is possible by reducing the insulator thickness or increasing the dielectric constant of the insulator (Eq.4.3).

The simplest, least expensive possibility is to vary the insulator thickness. By doing this we increase the magnitude of the electric field and amount by which it changes at the source barrier. The effect of reducing the nitride thickness by a factor of two was shown in Fig.7.13 for the lowest phosphorus implant (1x10^{14} cm^{-2}). These transfer characteristics show the dynamic range for \( V_G \) up to 20V has increased from ~40 (\( t_{SiN} = 300 \text{nm} \)) to ~150 (\( t_{SiN} = 150 \text{nm} \)) and the current at 10V has increased by a factor of 3. This shows that even though the SGT’s have smaller dynamic range in comparison with the FET’s there are ways around this problem.

12.2.7 Stability to stress

A very interesting property of the SGT occurs because the electron concentration in the active source region is much lower than it is in the active channel of a FET. Computer simulations shown in Fig.9.2 indicate that the concentration of electrons in the source region at the semiconductor-insulator interface can be orders of magnitude lower than it is in a FET but the amount depends on the effective barrier height of the source and the magnitude of the electron current.

This feature has important implications for the stability of the device because changes of the electron concentration and therefore the electron quasi-Fermi level give rise to defect formation in amorphous silicon as it strives to reach a different chemical equilibrium. If changes between the electron concentration in the off and on states can be reduced then the device will be more stable to voltage / temperature / current stressing. It has been shown that SGT devices operating at low currents are almost completely stable [64]. Furthermore it is found that a SGT is always more
stable than a FET operating at the same current (chapter 9., Fig.9.11). Alternatively one can say that a SGT can be operated at a higher current than a FET for the same stability.

12.2.8 Temperature dependence

The source barrier used in all our studies was a metal-semiconductor Schottky barrier. Current transport across the reverse polarized Schottky barrier is based on thermionic and thermionic-field emission as discussed earlier. Therefore as one might expect this carrier transport is thermally activated which is a disadvantage of the SGT device compared with a FET. However this temperature dependence is low for small barrier heights and higher currents. In figure (Fig. 12.5) the measurement of activation energy is shown. The transistor characteristics were measured from room temperature up to 80°C and using the gate voltage from 4V to 24V with step of 2V. The SGT device has 100 nm of a-Si:H and 150 nm of SiN. The s-d separation was 1.5 micron, w = 2 microns and barrier modification implant dose of 3x10¹⁴ cm⁻².

![Fig. 12.5 Activation energy measurement for the SGT device.](image)

The activation energy was estimated as a linear fit of the \( \ln(I_{SGT}) \) plotted as a function of \( 1/kT \) using Eq.8.4. It is seen that the activation energy decreases with gate voltage as the barrier is pulled down. Also the fact that the source barrier can be pulled down (in the on-state) to 0.17eV with sufficiently high fields \( (V_c = 24V) \) is interesting because it is within the factor of 2 of the activation energy measured on FET's (0.08eV).

Alternatively temperature dependence can be totally minimised using a different type of the barrier (e.g. barriers where the current transport is governed by field-emission processes).
12.3 Chapter summary

The advantages (+) and disadvantages (-) of the SGT device with a Schottky source in comparison with the conventional thin-film FET having the same semiconductor and insulator layers are summarised in following table (Table 12.1).

<table>
<thead>
<tr>
<th>SGT / FET</th>
<th>Low currents</th>
<th>High currents</th>
</tr>
</thead>
<tbody>
<tr>
<td>Saturation Voltage</td>
<td>+++</td>
<td>+++</td>
</tr>
<tr>
<td>Output Impedance</td>
<td>+++</td>
<td>+</td>
</tr>
<tr>
<td>Short channel effects</td>
<td>+++</td>
<td>+++</td>
</tr>
<tr>
<td>Voltage gain</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Stability to stress</td>
<td>+++</td>
<td>+++</td>
</tr>
<tr>
<td>Temperature dependence</td>
<td>--</td>
<td>--</td>
</tr>
</tbody>
</table>

Briefly one can say that the improvement in saturation voltage, output impedance and stability are fundamental to the operation of a SGT and should apply in all cases (i.e. high current and low current SGT devices). Likewise the FET will always have a higher value of saturation current and larger dynamic range for the same layer thickness and dimensions. On the other hand due to the source barrier and device geometry the SGT is much more immune to short channel effects with the possibility of SGT device fabrication at sub-micron level. The voltage gain despite the lower transconductance will be higher than that of a FET due to its high output impedance. SGT devices have a much better device stability than a FET prepared in a-Si:H for the same current driven through the transistor. Also it was found that for the same stability we could drive the transistor with higher current than the FET. The temperature dependence, however, is governed by the exact nature of current transport through the reverse biased source barrier which in our case was via thermionic-field emission. This temperature dependence can be corrected for electronically but also it should be possible to minimise temperature effects using a different form of source barrier.
Chapter 13

13 Conclusions and Future work

13.1 Conclusions

This thesis is concerned with new transistor devices named Source-Gated Transistors prepared in hydrogenated amorphous silicon. Amorphous silicon has become a widely used semiconductor in electronic circuits particularly for display applications. The most significant benefit of a-Si:H is its large area deposition capability at low cost on inexpensive substrates and despite low carrier mobility it provides applications that are otherwise unavailable in crystalline semiconductors (displays, solar cells, X-ray imagers) [6].

To the authors knowledge, there is only one relevant reference [57] to date from the other group concerning the properties of SGT devices. This paper reaches conclusions that are rather negative and are very different from our findings. This paper [57] is purely based on simulations and where the lack of the deeper understanding is obvious.

The construction and principle of SGT operation differs from a conventional thin-film FET. The operation of all FET's is based on the same principle, the gate voltage controls the channel conductance and current saturates when the drain end of the semiconductor is depleted of charge carriers. The on-current in the SGT is determined by a reverse biased source barrier located opposite a gate electrode [46]. Changing the gate potential affects the magnitude of the electric field at the source barrier and thereby the magnitude of the current flowing through the reverse biased barrier. The electrical characteristics of the SGT are very different from those of standard FET. In the first place the saturation voltage can be very much smaller [74] and therefore the device can be operated in saturation at lower drain voltages giving less power dissipation. Secondly, the SGT is much less sensitive to the drain field than a FET which is manifested as
much better output impedance. These features come about because of the change in geometry compared to a FET [51].

The SGT structure for low mobility semiconductors slightly differs from its general form [46]. In a-Si:H the extrinsic drain resistance is prohibitive without using conductivity modulation at the semiconductor-insulator interface as in a FET. Therefore the gate does not lie only underneath the gate but it was extended towards the drain edge (Fig.7.6). Consequently the modified structure has more parasitic capacitance but a low drain resistance. Effectively we have a SGT in series with a FET of length $d$. Then the off-state is determined by the threshold characteristics of the FET whilst the on-state was determined by the effect of the gate on the source barrier of the SGT.

There is one well known feature of thin-film FET's (TFT) prepared in a-Si:H; they are notoriously unstable showing large threshold voltage and on-current shift under voltage bias stress. It is shown that SGT's prepared in amorphous silicon have another important advantage over conventional TFT's; they are much more stable [65, 64] so the correction circuits in displays are possibly not required or significantly simplified and the life-time of the SGT devices can be extended beyond the margin of the conventionally used TFT devices. However this advantage of stable devices could be extended to all disordered materials such plastic and polymers where the defect generation rate and trapping of electrons depends on position of quasi-Fermi level. This feature could have as we believe important implications for future OLED and PLED based displays.

Also it was shown, that due to specific device construction, the SGT can be operated with lower carrier concentration, higher internal fields [75] and reduction in short channel effects [56] enabling the possibility of devices at sub-micron or nanometres scale to be prepared with superior characteristics [75].

As well as high fields and low electron concentration in the source it is also possible to obtain high fields and low electron concentrations in the parasitic FET. If the drain voltage is increased above $V_{STR}$ to $V_G - V_{TH}$ then as in a conventional FET the parasitic FET will pinch-off at the drain. It was shown that increasing $V_D$ above $V_G - V_{TH}$ can cause the whole of the parasitic FET channel to be depleted resulting in low electron concentrations and high fields throughout the device [59]. This feature reduces parasitic capacitance, charging times and carrier transport times. Also this feature with biasing the gate above $V_G - V_{TH}$ improves the stability of the device for short s-d separation.

The good agreement between experimental and simulated SGT transistor characteristics with Schottky barrier sources was presented (Fig.6.11) allowing us to use Silvaco ATLAS modelling to obtain much deeper insight into SGT device physics. Where it was possible, experimental results were supported by modelling and vice versa. The influence of device geometry parameters such
as source length, s-d separation, source barrier height, thickness of a-Si:H and SiN on the SGT properties was shown. It was seen that these parameters are very closely linked together. In later stages of this work these findings were used to explain some aspects of the SGT device behaviour and improve transient and small signal response.

The current through the SGT is determined by the effective barrier height of the Schottky barrier and its mutual conductance (transconductance) is determined by the change of the effective barrier height with the gate voltage. Assuming the uniform emission over the barrier the effective barrier height of the source was obtained as a function of the gate voltage (Fig.8.4, Fig.8.5) from transconductance measurements together with a tunnelling constant characteristic of the thermionic-field emission process.

In the case of high barriers it was found that the tunnelling constants were in good agreement with those measured previously in a-Si:H [37]. Next the dependence of effective barrier height on the gate voltage obtained from the thermionic-field emission model was in good agreement with measurements of changes in the activation energy for the current transport process (Fig.8.7). It was concluded that the current through these SGT’s is determined by the field dependence of the thermionic-field emission process in the reverse biased source Schottky barrier.

For low barriers and high currents the thermionic-field emission analysis gives lower tunnelling constants (Fig.8.6) and the barrier heights were higher than those measured experimentally. It is therefore likely that the current transport process became diffusion or space-charge limited. In this case, current is determined by the field dependence of transport through the bulk of the a-Si:H layer rather than the supply of carriers from the Schottky barrier.

In the experimentally prepared samples the barrier height was controlled by shallow phosphorous ion implantation. Using the model for SGT and barrier analysis based on thermionic-field emission theory the effective barrier heights were estimated and employed in ATLAS simulations of SGT transistor characteristics. The good agreement between the experiments and simulations was seen (Fig.6.12) but we found that ATLAS model underestimates the current for lower barrier heights.

The simulations also show that assumption of uniform emission is only true for higher barriers. In the case of lower barriers the current emission is concentrated towards the edge of the source opposite the drain contact (Fig.7.4). Interestingly this feature allows us to optimise the SGT device better in terms of transient response and small signal response. The average g_{s} in the source increases as the source becomes shorter resulting in the faster source charging time (Table.11.2).

The experimental results of transient response also showed good agreement between simulated and calculated results (Table 10.3). The fact is that the charging time for the SGT is longer than...
for a FET with the same device dimensions and layer thickness. Consequently the transient response is better for a FET than a SGT with the same geometry and calculated values of charging time (for quite large device $s = 5$, $d = 6$ and $w = 600$ microns) show that it is approximately a factor of 4 faster.

However, it should be possible to create a SGT with similar (or even faster) transient and small signal response compared to a FET for the same value of the output impedance. As we know, for very short s-d separation and low source barriers the SGT device still has good transistor characteristics as shown in Fig.7.10. Furthermore the whole of the parasitic channel can be depleted (Fig.9.6) at sufficiently high drain voltage, decreasing the resistance of the channel, and the device charging time (Fig.11.3).

The close link between the transient response and small signal response was presented comparing the calculated values of $f_r$ using the turn-on time from transient response and extracted values of $f_r$ from simulated small signal performance (Fig.11.2). This underlines the fact that one might optimize the SGT device in both areas at once. Simulations showed that one might expect the maximum SGT operation to be possibly around 60MHz. The dependence of cut-off frequency was discussed showing that it strongly depends on device geometry and barrier height (Table.11.1). Also the relationship between the $f_r$ and source length of the SGT which has a much more complex character was discussed. Finally the dependence of cut-off frequency on the gate voltage was demonstrated (Fig.11.5) and shown to have a very similar behaviour as the device transconductance vs. gate voltage (Fig.8.2b).

As such these devices are well suited to current driven matrix displays. We have shown that SGT devices in a-Si:H can be operated in the current region needed to drive OLED arrays (Fig.7.14) with improved stability (Fig.9.11) and output impedance (Fig.6.15) compared with a FET. They should enable LED pixel drivers to be operated with much lower power dissipation. The SGT is also a promising device for operation in the MHz region with possible application in row and column drivers. SGT allows us to bring the vision of fully integrated display and drivers much closer to a reality.

Another application area for SGT devices is in analogue electronics. The major reason and big drawback as to why this area has not been explored so far is the instability of thin-film FET devices in materials such as a-Si:H. Analogue electronics requires very good and stable device performance where transistor characteristics remain unchanged to within a few percent over the lifetime of the circuit and the SGT is able to handle such a demanding task.

In general the results show that stable, high performance electronics featuring SGT devices in amorphous silicon is a real possibility.
13.2 Future work

SGT devices are relatively easy to make using thin film technology. The widely used material in thin-film technology and large area electronics is a-Si:H due to its satisfactory semiconductor properties, large area deposition capability and very low material cost. These factors are very significant for the industry. Therefore the presented work was focused on SGT devices in a-Si:H. But the SGT concept should well suit to other disordered and defective materials. Hence the proposed future work could be divided into following areas:

13.2.1 Work on a-Si:H

1) More detailed analysis of transient and small signal response should be undertaken.

   i) Regarding the transient response measurements, the use of the operational amplifier in a different circuit arrangement should help to get rid of the fast initial transient and obtain better results.

   ii) In the case of small signal response where the measurements could not be performed more changes are needed. First the SGT devices should be properly designed with layout necessary to perform RF measurements. Next the low capacitance (Cascade) probes have to be used in order to minimise the parasitic elements in the measurement circuit. Thirdly the design of the matching circuits will be necessary otherwise the RF measurements will be pointless due to high reflection coefficients.

2) Another issue is the temperature dependence of SGT devices with a Schottky source barrier. As was previously suggested, use of a thin insulator barrier layer instead of Schottky source could result in current transport no longer being dependent on the temperature because the dominant transport mechanism would be field emission at the Fermi level. A great deal of attention has to be paid to the preparation of the right shape of barrier. In other words this barrier should have a high field dependence and should be easily pulled down with the gate voltage.

3) Other possibilities for the source include the use of a low work function materials and then using ion implantation to raise the barrier height to a sufficient level.

4) High k-materials – It was shown how the capacitance of the insulating layer influences the device performance particularly the saturated drain current and saturation voltage. In our presented work only the thickness of SiN was varied. However there are other materials with higher dielectric constant than SiN (e.g. oxides of Ta, Ti and Hf) which should allow improved SGT device performance.
5) Sub-micron or nanometer scale SGT devices - The concept of the SGT offers the prospect of devices working at very small dimensions where well-known short channel effects are minimised. The presented experimental results and simulations undoubtedly support this possibility. For example using focused ion beam (FIB) technique we should be capable to prove this point and create really sub-micron devices. Furthermore this concept, in principle, should work on the nanometer and molecular level. The first reference to investigate this point can be found on the internet where Prof. J. Kanicki (University of Michigan, USA) is leading a project to investigate such possibilities in gated source structures [76].

13.2.2 SGT and other semiconductor materials

The SGT concept should work also in the other materials:

1) Poly-Si is the very close material to a-Si:H with more ordered morphology and improved semiconductor properties (namely mobility). As mentioned previously, in order to achieve faster operation one needs materials with higher carrier mobility. We have been simultaneously exploring this possibility. First results are promising and published in Ref. [77].

2) Organic electronics on plastic – in my opinion this is the future of electronics on a large area scale. The research in organic and polymer materials is booming with more than 60 research groups and companies interested in this area worldwide which could produce a cheap and disposable electronic on inexpensive substrates or highly efficient displays with better parameters. With rapid improvements of organic materials the OLED and PLED are becoming more efficient and requirements on driving current are being reduced. Therefore SGT devices with higher stability and better characteristics prepared in organic materials should help to improve this application area. The fact that metals in connection with polymers usually form Schottky barriers should make it easy for SGT devices to be made.
References


Appendix

# Title: SGT device simulation source code

go devedit

load infile=SGT_13X_SD025_S025_A025_I10.de

# Definition of parameters for amorphous silicon and SiN

material material=silicon mun=15 mup=0.5 nc300=2.5e20 \ 
    nv300=2.5e20 eg300=1.0 taun0=1e-8 taup0=1e-8

material material=Nitride PERMITTIVITY=6.5

defects nta=1.12e21 ntd=4.e20 wta=0.025 wtd=0.05 \ 
    nga=1.0e16 ngd=1.0e16 ega=0.4 egd=0.4 wga=0.1 wgd=0.1 \ 
    sigtae=1.e-16 sigtah=1.e-14 sigtde=1.e-14 sigtdh=1.e-16 \ 
    siggae=1.e-16 sigghb=1.e-14 siggd=1.e-14 siggdh=1.e-16

DFILE=donors2.dat AFILE=acceptors2.dat

# interface and interface traps
interface charge=1e11

# define source workfunction
contact NEW.SCHOT name=source workfunction=4.52 TUN.LOW SURF.REC \ 
    BARRIER ALPHA=4e-7

# define models
Appendix

```plaintext
models srh temp=300 print

# define numerical method
method newton trap

# method for transient analysis
# method 2ND TAUTO AUTONR trap

solve init

output E.FIELD BAND.PARAM E.MOBILITY E.VELOCITY CON.BAND VAL.BAND QYN

save outf=tft.str
log outf=tft.log

log outf=transient.log

# Simulation of transient response

solve vgate=10.0 ramptime=1e-8 tstop=5e-6 TSTEP=1e-9 CYCLES=3 \ CYCLIC.BIAS SQPULSE TDELAY=2e-7 TRISE=1e-8 TFALL=1e-8 PULSE.WIDTH=5e-7 \ REQ=1e6 outf=sgt_trans1.str onefileonly master

tonyplot transient.log

# Simulation of Id/Vd characteristics

solve init
solve vgate=0 outf=solve_Otmp
solve vgate=2.0 outf=solve_tmp0
solve vgate=4.0 outf=solve_tmp1
solve vgate=6.0 outf=solve_tmp2
solve vgate=8.0 outf=solve_tmp3
solve vgate=10.0 outf=solve_tmp4
solve vgate=15.0 outf=solve_tmp5
solve vgate=20.0 outf=solve_tmp6

# load in temporary files and ramp Vds

load infile=solve_Otmp
log outf=idvdnl_0V.log
```

135
solve name=drain vdrain=0 vfinal=10.0 vstep=0.1 outf=tft_b0V.str \
    onefileonly master

load infile=solve_tmp0
log outf=idvdnl_0.log
solve name=drain vdrain=0 vfinal=10.0 vstep=0.1 outf=tft_b1.str \
    onefileonly master

load infile=solve_tmp1
log outf=idvdnl_1.log
solve name=drain vdrain=0 vfinal=10.0 vstep=0.1 outf=tft_b2.str \
    onefileonly master

load infile=solve_tmp2
log outf=idvdnl_2.log
solve name=drain vdrain=0 vfinal=10.0 vstep=0.1 outf=tft_b3.str \
    onefileonly master

load infile=solve_tmp3
log outf=idvdnl_3.log
solve name=drain vdrain=0 vfinal=10.0 vstep=0.1 outf=tft_b4.str \
    onefileonly master

load infile=solve_tmp4
log outf=idvdnl_4.log
solve name=drain vdrain=0 vfinal=10.0 vstep=0.1 outf=tft_b5.str \
    onefileonly master

load infile=solve_tmp5
log outf=idvdnl_5.log
solve name=drain vdrain=0 vfinal=10.0 vstep=0.1 outf=tft_b6.str \
    onefileonly master

load infile=solve_tmp6
log outf=idvdnl_6.log
solve name=drain vdrain=0 vfinal=10.0 vstep=0.1 outf=tft_b7.str \
    onefileonly master

# display IdVd characteristics
Appendix

tonyplot -overlay -st idvdnl_0V.log idvdnl_0.log idvdnl_1.log 
    idvdnl_2.log idvdnl_3.log idvdnl_4.log idvdnl_5.log idvdnl_6.log 
    tonyplot tft_te.str tft_b1.str tft_b2.str tft_b3.str tft_b4.str 
    tft_b5.str

# RF analysis

solve init
solve vgate=0 outf=solve_0tmp
solve name=gate vgate=0 vfinal=10 vstep=0.5 outf=solve_tmpx 
    onefileonly master
solve vgate=10.0 vdrain=1.0 outf=solve_tmp4
solve vgate=10.0 vdrain=5.0 outf=solve_tmp5
solve vgate=10.0 vdrain=10.0 outf=solve_tmp6
solve vgate=10.0 vdrain=15.0 outf=solve_tmp7
solve vgate=10.0 vdrain=20.0 outf=solve_tmp8

load infile=solve_tmp4
log s.param gains outf=ac_d1.log IMPORT=gate OUTPORT=source width=100 RIN=50 impedance=50
solve vdrain=1 name=gate vgate=10.0 AC FREQ=1E3 FSTEP=2 MULT.F NFSTEPS=18 onefileonly master

load infile=solve_tmp5
log s.param gains outf=ac_d5.log IMPORT=gate OUTPORT=source width=100 RIN=50 impedance=50
solve vdrain=5.0 name=gate vgate=10.0 AC FREQ=1E3 FSTEP=2 MULT.F NFSTEPS=18 onefileonly master

load infile=solve_tmp6
log s.param gains outf=ac_d10.log IMPORT=gate OUTPORT=source width=100 RIN=50 impedance=50
solve vdrain=10.0 name=gate vgate=10.0 AC FREQ=1E3 FSTEP=2 MULT.F NFSTEPS=18 onefileonly master

load infile=solve_tmp7
log s.param gains outf=ac_d15.log IMPORT=gate OUTPORT=source width=100 RIN=50 impedance=50
solve vdrain=15.0 name=gate vgate=10.0 AC FREQ=1E3 FSTEP=2 MULT.F NFSTEPS=18 onefileonly master
Appendix

```plaintext
load infile=solve_tmp8
log s.param gains outf=ac_d20.log INPORT=gate OUTPORT=drain \ 
IN2PORT=source OUT2PORT=source width=100 RIN=50 impedance=50
solve vdrain=20.0 name=gate vgate=10.0 AC FREQ=1E3 FSTEP=2 MULT.F \ 
NFSTEPS=18 onefileonly master

# Simulation of Id/Vg characteristics

solve init
solve vdrain=0.1 outf=solve_d_tmp0
solve vdrain=1 outf=solve_d_tmp1
solve vdrain=2.5 outf=solve_d_tmp2
solve vdrain=5.0 outf=solve_d_tmp3
solve vdrain=7.5 outf=solve_d_tmp4
solve vdrain=10 outf=solve_d_tmp5
solve vdrain=12.5 outf=solve_d_tmp6
solve vdrain=15.0 outf=solve_d_tmp7

# Load in temporary files and ramp Vgs

load infile=solve_d_tmp0
log outf=idvgnl_0.log
solve name=gate vgate=-10.0 vfinal=10.0 vstep=0.2 outf=tft_t1.str \ 
onefileonly master

load infile=solve_d_tmp1
log outf=idvgnl_1.log
solve name=gate vgate=-10.0 vfinal=10.0 vstep=0.2 outf=tft_t2.str \ 
onefileonly master

load infile=solve_d_tmp2
log outf=idvgnl_2.log
solve name=gate vgate=-10.0 vfinal=10.0 vstep=0.2 outf=tft_t3.str \ 
onefileonly master

load infile=solve_d_tmp3
log outf=idvgnl_3.log
solve name=gate vgate=-10.0 vfinal=10.0 vstep=0.2 outf=tft_t4.str \ 
onefileonly master
```

load infile=solve_d_tmp4
log outf=idvgnl_4.log
solve name=gate vgate=-10.0 vfinal=10.0 vstep=0.2 outf=tft_t5.str \
    onefileonly master

load infile=solve_d_tmp5
log outf=idvgnl_5.log
solve name=gate vgate=-10.0 vfinal=10.0 vstep=0.2 outf=tft_t6.str \
    onefileonly master

load infile=solve_d_tmp6
log outf=idvgnl_6.log
solve name=gate vgate=-10.0 vfinal=10.0 vstep=0.2 outf=tft_t7.str \
    onefileonly master

load infile=solve_d_tmp7
log outf=idvgnl_7.log
solve name=gate vgate=-10.0 vfinal=10.0 vstep=0.2 outf=tft_t8.str \
    onefileonly master

# display IdVg char
tonyplot -overlay -st idvgnl_0.log idvgnl_1.log idvgnl_2.log \
    idvgnl_3.log idvgnl_4.log idvgnl_5.log idvgnl_6.log idvgnl_7.log

tonyplot tft_te.str tft_t1.str tft_t2.str tft_t3.str tft_t4.str \
    tft_t5.str tft_t6.str tft_t7.str tft_t8.str

quit