Ion implantation techniques for the fabrication of gallium arsenide multilayer microwave devices

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Abstract

This thesis presents a study of the potential for ion implantation to play a more significant role in the manufacture and fabrication of commercially available multilayer microwave devices. Two different applications for ion implantation in device manufacture are investigated.

Firstly, implant isolation as an alternative to wet chemical etching for the planar doped barrier diode, and low and high power versions of the graded gap Gunn diode are attempted. It is demonstrated that the technique is an excellent method of lateral device isolation for the current generation of these devices, having little or no effect on the performance of the planar doped barrier diode, but with significant improvements in across wafer uniformity of device area, and hence, improvements in uniformity of device characteristics. Implant isolation of the graded gap Gunn diode has been met with mixed success. It has been shown that implant isolation has no detrimental effect on the ability of the device to emit microwaves at 77GHz, despite encapsulation of the active regions of the device in ion implanted GaAs. Problems have, however, been encountered with the geometry of the integral heat sink device (high power version), resulting in parasitic capacitance to the extent that the device experiences a shift in output frequency and power.

Secondly, doping of GaAs by ion implantation of the dopants magnesium and zinc, for the production of p-type layers relevant to GaAs multilayer microwave device manufacture is studied. Attempts are made to emulate the MBE grown planar doped barrier buried p-type spike using ion implantation of magnesium through a n-type contact region, and into a 'n-i-n' MBE grown structure. The result is a working bulk unipolar diode, with barrier height dependent on magnesium implanted energy and dose. A p-type dopant diffusion control experiment is also conducted whereby the depth of the diffusion-controlling phosphorus co-implant is varied to yield different p-type doping profiles. It is demonstrated that using this method it is possible to achieve a p-n junction with a gradually decaying p-type surface region, or an extremely abrupt junction. This technique is then used to produce and study varactor diodes, focusing on their rest capacitances, and their capacitance ratios. SIMS analysis and differential Hall effect measurements are also performed.
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1. Introduction

The current generation of multilayer microwave devices are grown by MBE or MOCVD. Whilst both techniques are outstanding in the results they achieve, and the technology they employ, problems have been encountered by industry endeavouring to use the techniques for large scale manufacture. Paramount are the difficulties encountered with non-uniformity of layers across-wafer, and with reproducibility from one growth run to another. In addition, some of the semiconductor etching techniques commonly used in, say, transistor manufacture, have not proved suitable for the production of discrete microwave components due to the poor across-wafer uniformity of the device area they achieve.

Industry has been slow to apply ion implantation techniques to the manufacture of discrete high-performance microwave devices fabricated by MBE and MOCVD, and this is a subject of major concern in this thesis. Ion implantation is capable of introducing dopants into semiconductor materials, and/or damaging them into a state of high resistivity in place of the mesa etching process - known as implant isolation - and has enjoyed outstanding success in the silicon integrated circuit, and GaAs MESFET industries. The techniques are discussed further in sections 4.1 - 4.3, and the literature review in chapter 2. Following ion implantation, lattice damage is present in the semiconductor, which is desirable for implant isolation, but not for dopant introduction. In order to activate implanted dopants onto a lattice site, and to repair the implantation-induced damage, an annealing cycle is required. Thermal annealing causes degradation of
the GaAs surface as arsenic vaporizes. To prevent this an encapsulant is needed on the GaAs surface, such as Si$_3$N$_4$, which can be chemically removed after annealing.

Implanted acceptors activate readily at temperatures in excess of $700^\circ$C, but diffuse during annealing, which may be controlled with the use of certain co-implanted ion species. Implanted donors do not activate so efficiently, and do not diffuse readily during annealing.

In this thesis we examine how the area definition of high-performance microwave devices may be achieved using implant isolation, and how some of the epitaxy may be replaced, or improved upon, using ion implantation of dopants. We also expand upon the current knowledge of diffusion-controlling co-implants of phosphorus, and apply the results to the fabrication and assessment of p-n junction varactor diodes.

Chapter 2 is a review of the literature on the subjects of semiconductor layer growth techniques, microwave devices, implant isolation, doping by ion implantation, and control of the diffusion of p-type dopants during annealing. It also serves as a further introduction to the background of this work.

The basic theory and operational principles of the microwave devices concerned with the project are described in chapter 3. These are the bulk unipolar diode, the Gunn oscillator diode, and the varactor diode. This is followed by a description of the methods employed during the project in chapter 4. Some theory is included in this chapter where appropriate.

The chapter is split into two areas; firstly ‘fabrication’, covering the routines and techniques employed to fabricate the devices, and secondly, ‘measurement’, covering the material and device assessment methods.
Chapter 5 is the experimental chapter, describing the implementation of the techniques covered in chapter 4. Every experimental result in chapter 6 is presented in the same order as its corresponding experiment in chapter 5, which is organised device by device, so that all the experiments performed on the bulk unipolar diode precede those on the Gunn diode, and those on the Gunn diode precede those on the varactor.

All the new results given in this thesis are contained within one major chapter, chapter 6, with appropriate discussions. Other information relating to these results is to be found in chapters 3, 5, and 7. This is followed by conclusions (chapter 7), as a summary of the results and achievements, and references in chapter 8. Following chapter 8 is the publication list of the author.
2. Literature Review

Since the 1950s, semiconductor mesa diodes have been extensively used as mixer/detectors, and voltage-variable capacitances (varactors) [8,9,10,11], in high frequency communications.

2.1 Doping methods

Exploitation of novel ion implantation techniques [1,2,3] has been relatively slow in the discrete microwave technologies. To date, the most accurate ways of constructing a semiconductor multilayer structure suitable for fabrication of microwave devices have been Molecular Beam Epitaxy (MBE) or Metal Organic Chemical Vapour Deposition (MOCVD) [4,5,6].

2.1.1 MBE, MOCVD, and VPE

MBE has been used experimentally since the early 1960s, and MOCVD since the 1970s, but neither have been a competing technology to Vapour Phase Epitaxy (VPE) for the growth of thick layer structures (>~1μm) until recent years [7]. This was due to the deposition rate limitations of early machines, which have since been overcome. VPE is no longer a competing technology to modern growth methods for the fabrication of high performance microwave devices. The advantages of MBE and MOCVD over VPE are numerous. The most important is that the time constants associated with VPE i.e. the time for the system to cease deposition after an 'off' switch is thrown are far less significant with MBE or MOCVD [7], facilitating the possibility of complex grown layer structures [4,5,6,12,13,14,15]. This is due to the minimization of redundant gas transfer line in MOCVD, and the use of instantaneous shutters with the MBE technique [15].
In general, MBE is a less complicated process than MOCVD as there are no additional chemical reactions to consider. An MBE reactor is fundamentally an evaporator. An MOCVD reactor is a low chamber-pressure, chemical reaction controller. The advantages mentioned above indicate the compatibility of MBE in particular, with the production of the current generation of discrete microwave components. Devices with microwave applications produced in GaAs using MBE growth include the planar doped barrier diode (PDB) [13], varactor diode [16], asymmetric spacer layer tunnel (ASPAT) diode, resonant tunnelling diode [17], Gunn diode [18,19], High Electron Mobility Transistor (HEMT) [82], and others.

Claims from growers that they can grow accurately doped, atomic-monolayer precision structures has led industry to attempt to exploit growth techniques for the fabrication of multilayer microwave devices [51,14]. Although the growers' claims are undeniable, consistent production of such tight-tolerance structures requires considerable focus from a grower, many repeated growth runs, and extensive customer collaboration, followed by material assessment, before the desired structure is achieved. Approaching a new grower to produce the same structure will necessitate expensive repetition of the same development exercise. It is therefore likely that a facility wishing to manufacture devices from such structures will need its own growth equipment, dedicated to the manufacture of a particular device or reproducibility problems will persist.

2.1.2 Ion implantation

One alternative to doping during epitaxy is the introduction of dopants from an accelerated beam of charged particles - ion implantation [21-49].
Ion implantation is an inherently controllable and reproducible technique, both in terms of impurity density, and dopant distribution, and is widely used in the semiconductor industry. Implanted impurity profiles approximate to a Gaussian distribution, but often have some small asymmetry associated with them, as shown in the SIMS profile in figure 6.18 of chapter 6, and discussed further in chapter 4, section 4.1.2. It is well known that acceptors implanted into GaAs diffuse readily upon annealing. This diffusion, and the electrical activation of acceptors in GaAs is well documented [29,31-34, 36,37,39-43, 45-49], and control of diffusion has also received much interest.

Electrical activation of dopants involves annealing in order that the introduced dopant has sufficient thermal energy to migrate onto a substitutional lattice site. The simplest method of diffusion control is rapid thermal annealing (RTA) where the semiconductor is heated to elevated temperatures for short periods of time [3,21,23,26,33,37,42,45,46,49,52], in order that the implanted dopant may activate without significant diffusion, since the diffusion distance is controlled by both the temperature and time during an anneal.

The diffusion depth of an implanted dopant is proportional to $(Dt)^{1/2}$ where $t$ is the time at the annealing temperature, and $D$, the diffusion coefficient, which is proportional to $\exp(-E_d/kT)$. $E_d$ is the energy of diffusion, $k$ is the Boltzmann constant, and $T$ the annealing temperature. The diffusion depth can be controlled therefore by shortening the annealing time or reducing the annealing temperature. Since sufficient thermal energy must enter the system for activation to occur, the anneal time is shortened to a few seconds or less, for activation without excessive diffusion. Some diffusion always occurs however, the aim of RTA being to limit the effect in comparison to furnace annealing for
several minutes. The problems with this method are associated with difficulties in
maintaining uniformity of temperature over the wafer, generating large thermal stresses
and wafer dislocations.

If an implant is to be electrically activated without significant diffusion, a co-implantation
technique is necessary. This involves the implantation of an element which, upon
annealing, occupies an arsenic lattice site. Although GaAs is unlikely to be in
equilibrium, an approximate, or pseudo equilibrium prevails during annealing, and from
simple thermodynamic arguments [75], the density of gallium vacancies is expected to
increase dramatically around the phosphorus co-implant peak. An increase in the gallium
vacancy density results in enhanced electrical activation of the p-type dopant due to the
increase in opportunities to occupy a substitutional site a potential acceptor sees during
annealing, and hence, less diffusion of the implanted p-type dopant [22,30,33,34,46,48].
In practice this has been achieved by superposition of the two implants. Hence, resultant
doping profiles approximate to their as-implanted shape. This is sometimes a desirable
feature, and sometimes an undesirable one. In some cases diffusion is required, maybe in
order to give a good electrical surface contact, but may need to be controlled to the extent
that the profile does not penetrate too far into the substrate.

2.2 Bulk Unipolar Diodes (BUDs)

Bulk unipolar diodes in the form of planar doped barriers are traditionally fabricated
using MBE or MOCVD [51,52].
2.2.1 BUDs formed using ion implantation

In silicon, devices similar to PDBs have been fabricated in the form of camel diodes using ion implantation as a method of introducing the n-type contact region, and the p-type spike, at very low energy [53-55], depicted in figure 3.1 of chapter 3. In GaAs, the contact technology is inhibited by the necessity for a diffused contact region, as 'n'-type doping levels high enough for a non-alloyed, evaporated top contact are not achievable. This precludes the low-energy implant approach to fabricating the device, as dopants would have to be implanted through the contact region. This thesis examines the formation of bulk unipolar diodes by implantation of the p-type dopant into a MBE grown n-i-n structure, and utilization of the tail of the implant to form a p-type region within the structure. New contact technologies are emerging for GaAs, and the potential use of these will be discussed in the further work section.

2.2.2 Mesa etching and Implant isolation

In addition to the problems encountered with reproducibility due to inconsistent layer growth, are problems associated with device area definition. A device engineer is interested in the I-V characteristics of a device, often the applied voltage at a particular operating current, and often the output power of the device at a particular applied voltage. In order to predict these operating parameters for devices made from a known layer structure, the engineer needs to be able to rely on a consistent device isolation technique. The common choices available are wet chemical etching and plasma etching, to produce a mesa structure, or the more exotic method of implant isolation, which enables retention of the planar nature of the wafer [13,14,56-74].
Carrier removal in GaAs occurs when ion implantation is performed. This is due to the generation of damage-related mid-gap states within the forbidden gap that is normally present in the ‘perfect’ crystal structure. Implant isolation is a method that involves the selective-area removal of carriers from a semiconductor due to damage caused by the implanted ions. Fundamentally, incorporation of the implanted ion species into the sample is of little importance to the process, although it is suggested that implanted ion incorporation has a relatively subtle effect on achievable levels of isolation [73,75]. This is a little understood phenomenon. It is also suggested that the isolation level is a function of electronic states formed due to a property of the introduced impurity [75,76], and that the original dopant species in the semiconductor target can affect achievable isolation levels, when using an oxygen implant [73,75].

The nature of the implant damaged region is dependent on a number of different parameters. The carrier removal rate depends primarily on the ion species. Boron and oxygen remove carriers at a rate of up to 120 per implanted ion at room temperature [57], whereas for protons the rate is of the order unity. It is also assumed [57] that approximately one in ten lattice atom displacements result in a removed carrier.

Two stopping processes occur when an energetic ion impinges on a target. At high energy the dominant mechanism is electronic stopping due to electrostatic forces between the target valence electrons and the charge on the impinging ion. As the ion decelerates in the target, a second mechanism, nuclear stopping, begins to have an increased effect. This is the collision of the nuclei of the target atoms and the energetic ion. At low energies this mechanism is dominant, and is responsible for the majority of target lattice displacements.
upon which we rely for the carrier traps that effect isolation. Isolating damage occurs, therefore, near the end of ion range [57]. This means that the damage level near the end of ion range has little dependency on the initial energy of the ion.

Greater ion doses inflict greater extents of lattice damage. Large ion doses therefore produce more resistive layers than small doses, up to a limit [57], where the shallow defect density is so great that hopping conduction occurs [56]. At this point, further increasing the ion dose results in an increase in electrical conductivity. Increasing the dose further (10^{17} \text{cm}^{-2} in the case of protons [77]) results in void formation after annealing, which raises the GaAs resistivity due to surface states on the inner walls of the voids. Void formation has not been exploited in this project due to uncertainties about the effect of lattice strain on the device characteristics, [78], despite the great thermal stability of the voids formed [79]. Overdoses of implanted ions in a semiconductor result in relatively low resistivity, due to the high density of hopping states generated (shallow levels within the forbidden gap), along with the desired deep levels. Electrons 'hop' from one of these states to another, and are regularly thermally energized into the semiconductor conduction band. The sample can be annealed towards an optimally resistive state [57], as the hopping states are less temperature stable than the deep levels. These anneals are often commensurate with contact alloying cycles[13]. Samples which receive too low an implanted dose will degrade with annealing towards their pre-implanted resistivity [56], due to the low density of deep levels generated. It is therefore likely that buried damage regions are possible, with negligible post-anneal surface damage,
due to the near-gaussian implanted damage profile [17]. Time related degradation of the isolation characteristics is also reported at semi-elevated temperatures [62].

Implant isolation has been demonstrated by the author and collaborators to be a viable technique for the production of graded-gap Gunn diodes [14], and planar doped barrier diodes [13].

The use of heavier ions such as boron or oxygen for implant isolation in recent years is a result of availability of high energy (several MeV) ion implanters, producing viable beam currents able to achieve ion ranges comparable to those reached by protons on conventional (100 or 200 keV) implanters. When lateral current confinement is required in a conducting epitaxial layer grown on a semi-insulating substrate, it has been shown that 5MeV oxygen implantation produces sufficient damage to isolate devices [72], with an approximately flat surface damage profile in the thin electrically active device layers. The peak of the implanted ion damage profile lies deep in the substrate, where it is ineffective. It is also shown that implanting MeV oxygen ions in a channelling direction results in double the ion penetration depth [72]. The commonly used isolation species are hydrogen [56], boron [65], and oxygen [62]. It is suggested that the use of implant isolation as an alternative to mesa etching can result in enhanced device performance [13,66].
3. Microwave Devices and their Mode of Operation

Sections 3.1 - 3.5 in this chapter are intended to give the reader an understanding of the principles of operation of the devices described. It is by the means of ion implantation (either for doping or isolation purposes) that we seek to improve the device characteristics, or at least maintain their state of operation and performance, with improvements in device yield or ease of manufacture. The first of these is the Planar Doped Barrier diode (PDB). Figure 3.1 depicts a PDB mesa structure.

3.1 The planar doped barrier diode (mixer/detector)

Fig. 3.1. PDB mesa structure.

The most interesting aspect of this device from the point of view of its usefulness as a mixer/detector within a circuit is the control the crystal grower has over its barrier height, represented in figure 3.2. The potential range of barrier heights available varies from a
short circuit, to within a few kT of the band gap of the semiconductor within which it is grown.

Figure 3.2 shows the electrostatic potential profile of a planar doped barrier structure, related to approximate doping levels within it. In essence the device is an ‘n-i-n’ structure with a fully depleted p-type spike within the ‘intrinsic’ region. In practice, the intrinsic region is doped to about $5 \times 10^{15}$ cm$^{-3}$ n-type, the p-type spike is of the order 40nm wide, and doped at $10^{18}$ cm$^{-3}$ and the n$^+$ encasement is also doped to a level of $10^{18}$ cm$^{-3}$.

Figure 3.2 Electrostatic potential profile of the planar doped barrier.

It is usual to grow the structure on an n$^+$ substrate of around $3 \times 10^{18}$ cm$^{-3}$ doping density, with a top contact region doped at the same level. This has the effect of slightly reducing the series resistance of the device.
The depleted structure within the intrinsic region creates an energy barrier proportional in height to its doping-width product. Additionally, the relative lengths 1₁ and 1₂ determine the symmetry of the barrier, and hence, the symmetry of the I-V characteristic. It is, therefore, possible to approximate the shape of the barrier from just these two sets of parameters. A greater extent of asymmetry of structure due to 1₁ and 1₂, will result in a more asymmetric I-V characteristic. If 1₁ = 1₂, the resultant device will be a diode with a symmetric I-V characteristic. PDB diodes are inherently leaky devices, and in practice a forward:reverse breakdown voltage ratio of 1:10 is sought by device engineers. The analysis using symmetry and sheet doping concentration is however a little simplistic, and is completed by the addition of two regions, one at either end of the intrinsic layer. Spill-over charge from the contact region exists in the intrinsic layer, and a depletion region occurs in the substrate buffer, due to depletion of the p-spike and the need to maintain overall space-charge neutrality.

The barrier height of a PDB diode can be estimated from Kearney et al [51] if we know the doping-width product in the p-spike, and the two lengths 1₁ and 1₂ by the relationship:

$$\phi_0 = q \frac{N_a t}{\varepsilon} \left( 1 + \frac{N_a}{N_d^2} \right) + kT/q + \zeta_2,$$

where

- \( q \) is the electronic charge
- \( N_a \) is the acceptor layer doping density
- \( N_d^2 \) is the doping density in contact nearest p-spike
- \( k \) is the Boltzmann constant
- \( t \) is the thickness of the p-spike
- \( \varepsilon \) is the relative permittivity of GaAs
\[ \zeta_2 \] is the Fermi level with respect to conduction band in Nd\(_2\).

\[ I_1 \] is the long intrinsic region

\[ I_2 \] is the short intrinsic region

assuming that \( I_1 \gg I_2 \).

The principal process of current conduction over the barrier is that of thermionic emission, and is essentially the same as that in the bulk unipolar diode described in section 3.2, where conduction processes are dealt with in detail.

3.2 The Camel Diode (mixer/detector)

Both the PDB diode and the camel diode are members of the bulk unipolar diode (BUD) family, the fundamental difference between the two being the existence of an intrinsic (or low-doped n-type) layer, in the PDB, between the contact region and the p-spike. The camel is effectively a PDB with \( I_2 = 0 \), resulting in the simpler \( n^+ - p^+ - i - n^+ \) structure depicted in figure 3.3. Again, in the camel diode, the p-type spike is fully depleted.
3.2.1. The forward bias case, and the Bethe criterion

In forward bias it has been shown [54] that the application of Bethe’s criterion and thermionic emission theory (as in the case of the Schottky barrier) is appropriate despite the difference in electrostatic potential profile shapes. The Bethe criterion states that the condition

\[ E_s \lambda \gg kT/q \]

must be satisfied, where \( E_s \) is the field at the junction, and \( \lambda \) is the mean free path of electrons around the potential maximum. With this condition satisfied, the number of electrons at the potential maximum increases exponentially with applied bias, and the
current is a maximum, limited only by the mean velocity of carriers crossing the top of the barrier.

\[ i.e. \ J_F = qvn_s \]

where \( n_s \) is the concentration of electrons at the top of the barrier, and \( v \) is their average velocity at a normal to the plane of the barrier. Since when thermionic emission prevails in a Schottky barrier, the current across the barrier is a maximum, and the forward voltage drop across it is a minimum, ideally we would like to see these factors as inherent in the BUD. The maximum electric field occurs either side of the potential maximum [53,54]. The barrier gradient in a BUD is less than in a Schottky diode, and the field around the potential maximum is small. Current could, therefore, be limited by diffusion over the barrier. Hence, one important design consideration is to endeavour to make the potential maximum narrow compared to the electron mean free path. Thermionic emission is then expected to prevail, and current conduction is governed by the equation:

\[ I = I_n \exp \left( \frac{qV}{n_kT} \right), \]

where \( I_0 = A_e A^{* *} T^2 \exp \left( -q\phi_v / kT \right) \)

and \( V \) is the voltage drop across the diode

\( n \) is the ideality factor of the diode

\( I_0 \) is forward current extrapolated to zero bias on log scale

\( A^{* *} \) is the Richardson constant modified to account for electron backscattering by phonons
\( A_e \) is the device electrically active area

\( \phi_e \) is the device effective barrier height

\( A'^* \) is not expected to be modified by the occurrence of quantum mechanical reflection of electrons from the barrier as BUDs are made in one material, and the potential profile is symmetrical around the top [54]. Phonon backscattering is, however, expected to occur, and to minimize this effect the designer may maximize the electric field on the \( n^+ \) side of the barrier to ensure that electrons gain the necessary energy over a short distance beyond the potential maximum. The field dependence of the barrier height in a BUD is due to image force lowering of the barrier, i.e. the equal and opposite charge induced on the other side of the barrier by an approaching electron. Fortunately, the image plane for an electron approaching the barrier of a BUD with a narrow and uniform \( p \)-type spike is in the \( n^+ \) layer, and, hence, image force lowering is much less significant than in a Schottky barrier.

3.2.2 The reverse bias case

Whereas the reverse breakdown mechanism in a Schottky diode consists of an image force lowering of the barrier at low bias, followed by an increase in the quantum mechanical tunnelling current at higher reverse voltages, the mechanism in a BUD is governed by electrostatic pull-down of the barrier. Image force lowering is not a significant contributor to reverse current because the image plane to an approaching electron is not in the barrier region, but in the \( n^+ \) contact region. Tunnelling is not as significant in a BUD due to the width of the barrier region.
Blocking characteristics can be of similar quality to those of Schottky diodes, if the thickness $t$ of the p-type spike is small—say of the order 50 Å, as electrostatic pull-down of the barrier is not then so significant, due to the concentration of charge in one small region. The rate of change of barrier height with applied reverse bias is approximated by the expression:

$$\frac{d\phi}{dV} = -t \left(\frac{qN_D}{2\varepsilon\varepsilon_0}\right)^{1/2} V^{1/2}$$

### 3.3 The Punch-Through Diode

The punch-through diode structure is the same as that of the camel diode. The difference lies in the doping-thickness product in the 'p'-type spike, which is too great for the structure to fully deplete. Figures 3.4, 3.5, and 3.6 show the band structure of such a device in the unbiased, reverse biased, and forward biased cases respectively.

**Figure 3.4. Unbiased Punch-through diode energy band diagram**
3.3.1 Forward bias

When the ‘n’-type layer is biased negatively with respect to the n' contact layer, the p'-n junction is in the forward bias condition, and the n'-p' junction is in reverse bias. The asymmetry of the structure dictates that hole emission from the base will predominate, occurring by the following mechanism, considering the structure as the equivalent transistor. Generation of holes in the reverse biased n'-p' region causes a flow of holes into the base, where charge is stored until the p'-n junction is sufficiently forward biased for the holes to flow into the ‘n’-type layer. More bias applied across the structure will be shared between the two junctions such that the hole flow into the substrate will be equal to the hole emission into the base from the p'-n' region. This will occur to a greater and greater extent until the punch-through condition occurs. Hole generation does not directly affect the barrier height to electrons or holes, but affects the division of applied bias between the two junctions. The charge storage mechanisms described here cause an inevitable hysteresis in the I-V characteristic as bias levels change.

**Figure 3.5 Energy band diagram of a Punch-through Diode in Forward Bias**
3.3.2 Punch-through diode in Reverse bias

The punch-through condition occurs when the low-doped ‘n’-type layer is biased positive with respect to the contact region, and so the p'-n junction becomes reverse biased, and the ‘p’-type region begins to deplete. As reverse bias is further increased, the generated depletion region extends to the depletion region at the n'+p' interface, until they touch. This is the punch-through condition.

A net flow of holes will enter the p^+ region under these conditions, which will produce a forward bias of the n^+ - p^+ junction. The charge build up is limited by emission of holes into the n^+ region, and/or recombination with electrons injected from the n^+ region. If the doping concentration in the n^+ region is large compared to that in the p^+ layer, the ratio of electron/hole current may be approximated by the ratio of their conductivities, \( \alpha_n/\alpha_p \).

Normally the current gain \( \beta \) of the equivalent transistor would be \( << \alpha_n/\alpha_p \) so recombination is the dominant hole removal process, and the hole leakage current \( I_h \) is amplified. The reverse leakage current \( I_R \) of the device is hence given by:

\[
I_R = I_h \left( 1 + \beta \right)
\]
3.4 The Gunn diode (Gunn oscillator, microwave source)

3.4.1. Negative differential resistance

The Gunn diode in its most basic useable form is an n-type GaAs (or InP) region, sandwiched between two n⁺ contact regions, also of GaAs (or InP). It is the first of a generation of devices known to exhibit negative differential resistance (NDR), a principle of its operation as a DC-microwave power converter. The radiated power is associated with negative differential resistance caused by the intervalley transfer of electrons from the lower to the upper valley in the conduction band, depicted in fig 3.7(a).
Figure 3.7(a) Two valley model of electron energy versus wave number for n-type GaAs

Upper Valley
m_{ev} = 1.2
\mu_{ev} = 180 \text{ cm}^2/\text{V.s}

Lower Valley
m_{lu} = 0.068
\mu_{lu} = 8000 \text{ cm}^2/\text{V.s}

\Delta E = 0.36 \text{ eV}

\text{Conduction Band}

E_g = 1.43 \text{ eV}

\text{Forbidden Gap}

\langle 100 \rangle

\text{Valence Band}

Figure 3.7(b) below shows the effect of the intervalley electron transfer on the I-V characteristic, which clearly exhibits negative differential resistance. The actual diode is a 60\mu m diameter integral heat sink device.
At low fields most electrons are in the lower energy, high mobility valley, i.e. in the lower valley. As the electric field in the GaAs increases beyond the threshold field $E_r$, (about 3200 Vcm$^{-1}$) electrons are scattered to the upper valley (0.36 eV above the bottom of the lower conduction band valley) labelled with its corresponding low mobility state for electrons. Hence, increasing bias results in decreasing current, and NDR.

3.4.2 Modes of operation

The scattered electrons are near the cathode of the device, a region of major inhomogeneity, where this mechanism occurs just before electrons in the rest of the device can respond to the rising field. Just ahead of them the field is low, and the electrons have a high drift velocity. These fast electrons leave a region depleted of electrons behind them, which, together with the accumulated layer of slow electrons, create an electrostatic
The dipole, across which the field is high. This high field grows at the expense of the field in the rest of the device, and the device is operating at constant current. On arrival at the anode the discharge of the dipole causes a momentary rise in current and the process begins to occur again. The spike like shape of the current rise is indicative of the high harmonic content of the resultant waveform, and hence, its low fundamental efficiency.

The frequency of operation of the device is given by

\[ f_T = \frac{1}{T_t} = \frac{V}{L} \]  

(3.1)

where \( T_t \) is the transit time of the dipole, \( L \) is the length of the transit region, and \( V \) is the velocity of the dipole across the transit region. This mode of operation is known as the Transit Time Mode, and was the mode first observed by J. B. Gunn in 1963 [20].

Several other modes of operation for the Gunn diode exist, the most commercially important being the Delayed Domain Mode (the most common mode of operation in commercial devices). In this mode, the device is operated so that for part of the cycle of the device (just when the dipole region reaches the anode), the total field across the device falls below the critical field, and no fresh dipole can nucleate. This delay in nucleation of a new domain adds a new term to \( T_t \) in equation 3.1 so the new frequency is given by

\[ f_0 = \frac{1}{(T_t + T_d)} \]

where \( T_d \) is the delay time before the critical field at the cathode is reached again.

Fundamentally speaking, the frequency of operation with no domain delay (which is present only for the purposes of stability of operation) is dependent on the doping density
in, and length of, the transit region. The use of a drift region in the n-i-n structure to accelerate electrons (often of the order 0.25μm width, compared with 1.5μm transit region width) causes reduced efficiency due to series resistance. For high power applications a hot electron injector is required. In our case this is a graded Al (0-33% Al) AlGaAs layer, shown in fig 3.8, which utilizes the difference in band structures between GaAs and AlGaAs.

**Figure 3.8. Schematic Doping profile of a Gunn diode showing graded AlGaAs hot electron injector**

The n⁺ region adjacent to the graded AlGaAs layer gives the necessary control over the field at the cathode, in order for critical field to occur at the cathode.
3.5 The varactor diode

The varactor diode is essentially a voltage dependent variable capacitor. The two most common types are the Schottky varactor, and the p-n junction varactor. The principle of operation depends on the variability of the depletion region depth at the metal-semiconductor interface, or the p-n junction, with changes in applied bias. The rest capacitance, $C_0$, is governed by the equation

$$C_0 = \varepsilon A/D$$

where $\varepsilon$ is the semiconductor permittivity, $A$ the junction area and $D$ the total depletion depth in the semiconductor. In the case of the p-n junction varactor, the focus of this project, the construction of the device consists of an activated p-type implant on a low-doped 'n'-type epilayer, grown on an n$^+$ substrate, depicted in figure 3.9.

Figure 3.9 Varactor diode mesa structure
It is customary to make these devices as p⁺-n structures, with a thin (= 0.2 μm) p⁺ surface region, for easy ohmic contact formation, and the lowest possible series resistance.

Basic DC C-V characteristics of varactor diodes are governed by conventional p-n or Schottky diode theory, described by Sze [80]. Whether the device is a p-n junction varactor, or a Schottky varactor, both of which are used in high frequency communications, two types of device are of importance in the marketplace. Firstly, the abrupt junction varactor. This is a device in which the interface (whether p-n or metal-semiconductor) width is narrow compared with the epitaxial layer thicknesses, shown below in figure 3.10 (a).

**Figure 3.10. Doping profile of (a) abrupt, and (b) hyperabrupt junction tuning varactor.**
This type of device yields a capacitance variation which is roughly proportional to the inverse square root of the applied reverse-bias voltage. The capacitance as a function of voltage is given by [12],

\[ C(V) = K \cdot A \cdot (V + \phi)^{-\sigma} \]

where:

- \( C(V) \) = capacitance of diode at voltage \( V \)
- \( K \) = constant
- \( A \) = area of the diode
- \( V \) = voltage applied to the diode
- \( \phi \) = built-in potential of the diode
- \( \sigma \) = the capacitance - voltage slope exponent (\( n \approx 0.5 \) for an abrupt diode)

The second (and slightly more complex) type of device is the hyperabrupt junction varactor diode, shown in figure 3.10 (b). This type of device is used when an approximately linear variation of frequency with applied voltage is required. The inverse square root dependence of the abrupt junction capacitance provides an inverse fourth root frequency dependence on applied reverse bias [12]. A hyperabrupt varactor is designed to give an inverse square capacitance law, resulting in narrow band linear frequency dependence on voltage.

The hyperabrupt varactor profile has a higher n-type doping level at the interface, resulting in a narrower depletion region (hence hyperabrupt), and higher capacitance at zero bias. Since the doping level falls as the depletion region extends further into the epilayer with increasing reverse bias, the rate of change of capacitance with applied bias is greater than...
in the case of the abrupt varactor. The capacitance-voltage relationship is described by the equation:

\[ C(V) = C(0) \cdot (1+V/\phi)^\gamma \]

where \( C(0) \) = mathematically extrapolated junction capacitance when \( V = 0 \)

\( \phi \) = built-in potential of the diode

\( \gamma \) = the capacitance-voltage slope exponent (gamma)

(gamma > 0.5 for a hyperabrupt diode).

In summary, the varactor diode is a voltage-variable capacitor. It exhibits a 'rest capacitance', due to its depletion width at zero bias, and decreasing capacitance with increasing values of reverse bias. The rate of change of the capacitance with applied potential is a function of the doping profile encountered by the depletion region as it extends into the semiconductor.
4. Techniques

This section contains brief descriptions of the methods employed to achieve the results presented in chapter 6. Some theory is included where appropriate.

The chapter is split into two subsections, one loosely called ‘fabrication’, describing the means used to produce materials and devices for assessment, and the second entitled ‘measurement’, covering assessment techniques employed and their basic principles.

4.1-4.4 Fabrication

4.1.1 Ion implantation

The implantation process: Ion implantation is a commonly used means of introducing impurities into a target material, or modifying its properties. A block diagram of an ion implanter is shown below in fig. 4.1.
A plasma is generated in the ion source by a variety of methods such as a radio frequency source or a hot filament energising an injected gas or particles from a sputtered target into the plasma state. The injected gas may originate from a gas bottle, a liquid, or a heated...
solid. The entire interior of an ion implanter is under vacuum, ranging from $10^{-5}$ Torr in the source chamber to $10^{-7}$ Torr in the target chamber.

The source chamber is charged to a potential of about 20 kV, which forces positive ions out of the source chamber, through an electrically biased slit lens, and into a powerful magnetic field, generated through a chamber bent through an angle of between 60° and 90° as a means of mass selection. A second acceleration stage follows, the total acceleration potential experienced by the ions being the sum of the first and second acceleration potentials. Electrostatic bending of the beam is normally then employed to offset the beam from any neutral elements within it, before electrostatic focusing. Finally, the beam is scanned over the target, using alternating electric fields in the horizontal and vertical planes.

The ion dose received by the target is counted by means of a current integrator, which gives the total charge contribution to the target from the ion beam. The magnitude of the charge on a singly charged implanted species is that of the electronic charge. Twice as many counts are required if a doubly charged species is implanted, or half as many if a molecular ion containing two atoms is implanted.

A doubly charged ion is accelerated to twice the potential as a singly charged ion; hence, a 200 kV implanter may be used as a 400 kV machine if the doubly charged species is selected from the ion source. A 2-atom molecular ion will dissociate within the first few atomic layers on impact with a target, the energy split evenly between the constituent atoms (assuming that the two constituent atoms are the same type). In a system where the constituent atoms are not the same (e.g. BF$_2^+$), the resultant energy of a constituent ion
after splitting of the molecule is proportional to the ratio of its own mass to the total mass of the molecule. It is by selection of doubly charged and molecular ion species that we manipulate the energy range of operation of an implanter to suit our own needs.

Implantation is normally carried out with the incident rastered ion beam at an average 7° angle to the wafer surface normal. This is beyond the acceptance angle for incident ions to enter a channel, and this improves the conformity of the implant to the Gaussian profile model.

4.1.2 Implanted ion distribution

The ion range is governed by the rate of energy loss of the ion in the target due to collisions with the atoms and electrons in the target. It is given by

\[ R = \int_{E_0}^{E} \frac{1}{dE/dx} dE \]

Where \( E_0 \) is the initial ion energy. The normal distance from the surface for a single ion is called the projected range, \( R_p \). For many ions (the practical case), \( R_p \) refers to the mean projected range. Implanted ion profiles are often approximated by a Gaussian curve, or a skew Gaussian, with the range distribution given by

\[ N(x) = \exp \left( -\frac{1}{2} \left( \frac{x - R_p}{\Delta R_p} \right)^2 \right) \]

where \( \Delta R_p \) is the standard deviation of the range.
4.2 Implant isolation

As discussed in the literature review, implant isolation relies on the formation of deep levels within the semiconductor target, with the result that carriers become trapped in these levels, and the material resistivity increases by orders of magnitude, so that devices are electrically isolated from one another. In actual fact the ion implantation process results in deep and shallow levels within the bandgap, resulting in a relatively conductive material, due to carriers hopping from one shallow state to another. This 'hopping conduction' is eliminated by a furnace anneal, (the temperature of which is dependent on the ion species implanted), to remove the damage causing the shallow levels, which is less thermally stable than the damage causing the deep levels.

The damage profiles are usually simulated using TRIM, (Transport of Ions in Matter), a simulation package which performs Monte Carlo calculations to yield, among other data, final ion and damage distribution simulated profiles. The simulations at different energies are then summed to obtain the necessary profile to isolate the device concerned. The factors to be considered when choosing an ion species include the thermal stability required of the device, the available ion range given the energy capability of the implanter/accelerator, and available beam current (from an economic point of view).

Figure 4.2 shows the structure of an implant isolated planar doped barrier diode [13], produced using the self-aligned technique.
The advantages of the technique over wet chemical processing are listed in 2.2.2.

4.3 Doping and dopant activation

Two methods exist for doping of semiconductors when devices are not produced from layers grown by MBE, MOCVD, or other similar techniques, (i) diffusion from the surface, and (ii) ion implantation.

4.3.1 Dopant diffusion

The oldest, and perhaps most obvious, is diffusion of the dopant from the surface, and into the bulk. This is a difficult process to control, resulting in long and unpredictable diffusion tails, and problems associated with the cleanliness of the surface.
4.3.2 Implantation of dopants

Slightly more recent and now more common is the method of ion implantation, where the position and shape of the introduced dopant profile is known with greater accuracy, either from simulation or, better still, from past measurements. After implantation, the target is damaged, and the implanted dopants are not electrically active. The extent of the damage is dependent on the ion energy, ion species, sample temperature during ion implantation, and ion dose. Electrical activation of dopants is achieved using thermal annealing, where the implanted material is heated to temperatures usually in excess of 700°C, to energize the system sufficiently that dopants may be incorporated onto substitutional lattice sites, and in order that the implantation-induced damage may be ‘annealed out’. i.e. the material recrystallizes. In our case, we have, for the BUD and punch-through diode structures, used implants of magnesium as a ‘p’-type dopant, and for the varactor structures, zinc.

4.3.3 Rapid Thermal Annealing (RTA)

Diffusion of ‘p’-type dopants in III-V semiconductors during activation annealing is well known and can be problematic for the engineer trying to form a shallow ‘p’-type region at the semiconductor surface, or a well defined buried ‘p’-type region. One way of controlling this diffusion is Rapid Thermal Annealing (RTA), where a very short, high temperature cycle is used to activate dopants rapidly, and recrystallization still has time to take place, before diffusion can occur. This is a superior method to furnace annealing.
where diffusion control is difficult, although with RTA there are still some associated control problems, and diffusion is not insignificant.

4.3.4 Phosphorus co-implantation

A better method still is the co-implantation of a second ion species with the dopant, where the co-implanted species does not dope the material, but does occupy arsenic sites. During the course of this work phosphorus has been exclusively used for this purpose. In equilibrium this tends to increase the concentration of gallium vacancies within the material which act as substitutional lattice sites for activation of the ‘p’ type dopant. This method will be shown to be a reliable way of controlling diffusion of acceptor impurities in GaAs.

4.4 Fabrication routines

Listed here are four different diode fabrication processes. Since the basis of this work has been modification and improvement of the processes, their inclusion is important. Accompanying each process is a diagram showing the final chip orientation.

4.4.1 Planar Doped Barrier Diode Process

1) PECVD deposit 0.25 μm SiO₂ on wafer surface

2) Leave wafer in Hexamethyldisilasane (HMDS) vapour ambient for 7 minutes

3) Spin on Shipley S1828 photoresist 5000 rpm 30 seconds

4) 1 minute softbake-90°C hotplate

5) Expose under oxide window mask 15 seconds 400 nm Ultraviolet

6) Develop in microposit 351CD31 developer for 1 minute

7) Inspect
8) UV ozone clean 5 minutes
9) Pre-wet in fast DI water stream
10) SiO$_2$ etch by eye-10% HF
11) Isopoly resist strip-by eye
12) 3x3 solvent clean (Trichloroethylene, Acetone, Isopropanol) - Blow dry
13) GaAs etch (hexacyanoferrate III) - 2.5 μm by Dektak profiler
14) Rinse in DI water, blow dry
15) Strip oxide
16) Grow new oxide
17) repeat steps 3-4
18) Expose under negative of mask in step 5
19) Develop as in step 6
20) UV ozone clean
21) de-oxidise exposed contact windows
22) Contact etch
22) Place immediately into evaporator and evacuate
23) Evaporate Au/Ge/Ni contacts
24) Lift-off resist and metal in Isopoly phenol-based resist stripper
25) 3x3 solvent clean-start with 3x boiling Trichloroethylene
26) Inspect
27) Lap back substrate to 75 μm
28) Clean in DI water
29) Contact etch

30) Repeat steps 22 and 23 for back contact

31) 3 x 3 solvent clean - start with boiling trichloroethylene

32) Contact alloy in H₂ ambient 390°C 10 seconds.

Figure 4.3 Planar doped barrier diode structure.

4.4.2 Low-power Gunn Diode Process

1) 3x3 Solvent clean

2) PECVD deposit 0.5 μm Si₃N₄

3) Thin substrate to ~125μm using 5μm alumina paste
4) Prepare substrate surface for metallization using 3:1:1 H$_2$SO$_4$:H$_2$O$_2$:H$_2$O etch for 20 seconds

5) DI water rinse, blow dry, into evaporator and pump down.

6) Evaporate Au/Ge/Ni (83%:12%:5%) to 1000Å thickness.

7) Contact alloy 385°C 60 seconds in H$_2$ ambient

8) Remove Si$_3$N$_4$ in 5:1 NH$_4$F:48%HF

9) Place sample in HMDS vapour for 7 minutes

10) Spin on Shipley AZ4562 positive resist 5500 rpm for 30 s.

11) Soft bake 90°C 120 seconds

12) Photolithography to open contact windows

13) UV ozone clean 300 seconds

14) Contact etch

15) Evaporate Au/Ge/Ni as before

16) Lift off resist in acetone

17) 3x3 solvent clean

18) Repeat alloy cycle

19) Repeat photolithography using contact mask to achieve plating area.

20) UV ozone clean

21) Etch alloyed surface in 10:1 H$_2$O:HF

22) Plate for 30 minutes in Transtherm gold plating solution

23) Photolithography as above using larger contact mask
24) Mesa diodes in $K_3Fe(CN)_6$, continually probing until correct characteristic is achieved.

**Figure 4.4 Low-power Gunn diode structure**

Figure 4.4 above shows the final device structure, a microwave emitter with about 50 mW output power. If a higher power device is needed, then the following heat-sunk structure is used.

**4.4.3 Integral Heat Sink (IHS) Gunn Diode Process**

1) 3x3 solvent clean

2) HMDS ambient 7 minutes

3) Spin on AZ4562 photoresist 5500 rpm, 30s.

4) Soft bake 90°C 120 seconds

5) Expose to grid patterned mask

6) Develop in AZ400k developer
7) Post bake at 115°C for 120 s.

8) UV ozone clean

9) 210 seconds in 1:4:10 (H₂SO₄:H₂O₂:H₂O) to etch grid 14μm deep

10) Phenol based resist stripper

11) 3x3 solvent clean

12) Etch sample 15 seconds in 10:1 H₂O₂:40%HF

13) Evaporate ~1000Å Au/Ge/Ni

14) Alloy contact in H₂ ambient 385 °C 60s

15) Gold plate as in low power process, to thickness of 30μm

16) Thin substrate in bubble etch tank using 3:4:4 etch H₂O:H₂O₂:H₂SO₄. Etch is complete when grids appear

17) Back contacts are then formed by photolithography, then the mesa mask is applied

18) Gold plating as before

19) Substrate etched through to gold layer

20) Contact alloy as before

21) Plating to 5μm as before.

The resultant wafer now consists of a 30μm thick gold leaf, on which are mounted individual Gunn devices, epilayers down. Devices are separated using a scalpel. The 30μm gold layer is hence the ‘top’ contact and acts as the heat sink for the device. Junction temperatures can approach 300°C.
The following is the fabrication process for the varactor tuning diode.

4.4.4 Varactor diode

1) Grow 0.5μm PECVD oxide

2) Thin substrate using 5μm alumina paste and contact etch

3) Evaporate Au/Ge/Ni and alloy as before

4) Perform photolithography for mesa

5) Mesa etch as in other processes

6) Remove resist and oxide

7) Deposit new oxide
12) Etch unwanted gold (proprietary gold etch)

13) Strip resist

14) Photolithography to isolate areas for electroplating

15) Au plate as before

16) Strip resist and unwanted Ti 75:5:1 H₂O:H₂SO₄:40%HF

Figure 4.6 Varactor diode structure.
4.5 Measurement

4.5.1 I-V and barrier height assessment

As mentioned in section 3.2.1, it is appropriate to apply the ideal diode equation to the BUD family to yield barrier height and ideality factor.

We have \[ I = I_o \exp \left( \frac{qV}{nkT} \right) \]

Taking logs \[ \ln I = \frac{qV}{nkT} + \ln I_o \]

So plotting \( \ln I \) against \( V \) yields the classic straight line equation of the form \( y = mx + c \), where \( \ln I_0 \) is the y intercept and \( q/nkT \) is the gradient. The value of the ideality factor \( n \) may be obtained straight away as \( k, T, \) and \( q \) are known, and the value of \( \ln I_0 \) may be substituted, after taking further logs, into

\[ I_o = A_e A^{**} T^2 \exp \left( -q\phi_e / nkT \right) \]

which gives the value of the effective barrier height, \( \phi_e \), assuming a value of \( 10^6 \) for the Richardson constant \( A^{**} \).

4.5.2 Secondary Ion Mass Spectroscopy (SIMS)

A SIMS system has much in common with an ion implanter in that it employs an ion beam of energy generally < 20keV focused to a beam diameter = 60 \( \mu \)m. The beam is first
rastered over the sample surface to sputter away surface contaminants, and then concentrated on one area within the cleaned region. Because the beam is low energy, nuclear collisions dominate at the surface, and the target is sputtered away. Sputtered ions from the target are mass analyzed and detected and distinguished by atomic or molecular mass. Sometimes, in the case of a sample containing Zn$_{64}$, it may be convenient to use a caesium beam for sputtering the sample, and detect the zinc as the ZnCs$^+$ complex ion, as this will distinguish the zinc from, say, the S$_2^+$ molecular ion.

The system is calibrated by analysing a sample containing a known amount of the impurity concerned, and also, in the case of GaAs, by monitoring the levels of arsenic present. Depth resolution is calibrated by an optical measurement of the crater, and normalisation of the distribution curve.

The most common inaccuracy of the system is a phenomenon known as ion beam mixing, where analyzed impurities often seem to have originated from a depth greater than they actually exist. This is due to the impinging ion beam “pushing” the impurities further into the material. It is thought that this is a significant problem when measuring the distribution profile of a light implanted species such as hydrogen.

At the surface of the target (first few nm) inaccuracy occurs due to the gradual build-up of the implanted primary ion species. Secondary ion yields do not stabilize until the primary ion concentration reaches a steady state level at a depth dictated by the range of the primary species in the target.

It is also important to note that, unless 100% dopant activity is to be assumed, a SIMS profile is only a measure of atomic concentration, and not a doping profile.
4.53 Differential Hall Effect (DHE) measurement

In this technique thin layers are stripped in sequence from the semiconductor surface and the resistivity and Hall coefficient are measured by the Van der Pauw method. Ohmic contacts are made to the corners of a cloverleaf shaped sample by diffusion of an appropriate dopant. The carrier concentration and mobility profiles are calculated from the differential measurements. The Van der Pauw geometry is shown in figure 4.7.

![Figure 4.7 Cloverleaf Hall sample](image)

The sheet resistivity may be expressed as

\[ \rho_s = \frac{1}{\pi \ln 2} \cdot \frac{1}{(R_1 + R_2)/2} \cdot f(R_1/R_2) \]

Where, referring to figure 4.53,

\[ R_1 = \frac{V_{34}}{I_{12}} \quad , \quad R_2 = \frac{V_{41}}{I_{23}} \]
and \( f(R_1/R_2) \) is a correction factor which tends to 1 for a symmetrical sample.

The sheet Hall coefficient, \( R_s \), is determined by measuring the change in \( V_{13} \) normal to the current path \( I_{24} \), when a magnetic field \( B \) is applied perpendicular to the sample. \( R_s \) is given by

\[
R_s = 10^8 \left( \frac{\delta V_{13}}{BI_{24}} \right)
\]

The sheet Hall mobility is given by

\[
\mu_s = \frac{R_s}{\rho_s}
\]

and the sheet carrier concentration \( N_s \) is obtained from

\[
N_s = \frac{r}{eR_s}
\]

where \( r \) is the ratio of the Hall mobility \( \mu_s \) and the conductivity mobility \( \mu \). The value of \( r \) depends on the impurity scattering mechanism, which is assumed to be predominantly ionised impurity scattering. In this case \( r \) is normally assumed to be unity.

It is the changes in values, from one layer removal to another, that reveal the carrier concentration and mobility as a function of depth.

Layer removal is achieved by anodic oxidation of the sample up to a known potential, and then chemical etching. Hence the approximate thickness of the layer removed is known.

The profile may be normalised later to a depth measured on a profilometer.

4.5.4 Simple I-V assessment

It is often not necessary to perform the relatively complicated calculations to evaluate the performance of, say, a PDB. If, for example, we wish to know whether an implant isolation on a wafer has been successful, then on-wafer probing is a sufficient gauge.

Common measurements are the reverse and forward voltage at 100\( \mu \)A, (the latter often
being interpreted as the barrier height), and the device resistance determined by measuring
the slope of the I-V characteristic between 10 and 20 mA. These simple data may be
compared to a control mesa sample, to yield information about the success of the implant
and the electrically active area of the device. These basic measurements may be performed
using a simple probe station coupled to a curve tracer.

4.5.5 Microwave performance assessment

i) Planar doped barrier diode

Measurement of the performance of a PDB is normally concerned with the noise
characteristics of the device when operating in a circuit. Measurement of a packaged
device is considerably easier than measurement on-wafer, due to the complicated
fabrication routines and probing equipment required for on-wafer measurements. The
disadvantage of measuring a device within a package is the additional parasitic impedance
presented by the bond wires and package casing. This may, at least, be considered
constant. The two parameters examined in this project are intermediate frequency noise
figure (IFNF) with the device operating as a mixer at 9.375 GHz, and the tangential
sensitivity of the device to a 1kHz-modulated 9.375 GHz signal. This second measurement
indicates the ability of the device to detect the 1kHz signal above the superimposed 'noise'
of the 9.375 GHz signal, and is expressed as the attenuation it is possible to impose on a
signal of fixed amplitude before the 1kHz signal becomes undetectable. The measurements
are performed with high and low frequency signal generators, microwave power meters
and an oscilloscope.

ii) Gunn oscillator
Again, devices are assessed already packaged. One advantage to the method of making measurements of pre-packaged devices, in contrast to the disadvantage described earlier, is that the information obtained about the device is relevant to the final product, and predicts the performance of the device in-circuit.

The relevant measures of performance in this case are the DC-microwave conversion efficiency of the device at fundamental frequency, and the spectral noise voltage density measured at 100kHz off-carrier frequency. This is an attenuation value calculated from the noise voltage 100kHz away from the peak amplitude of the fundamental frequency of the device, and is expressed in dBc/Hz, and is performed with a power supply operating the diode, and a spectrum analyzer.

4.5.6 C-V assessment

These measurements were carried out on p-n junction varactor diodes. The equipment consists of an automatic Hewlett Packard C-V measurement system connected to a jig in which the packaged device is mounted, and external parasitic capacitances are calibrated out of the measurement.
5. Experimental

This chapter describes the implementation of the techniques outlined previously. It is divided into sections describing the experiments performed on the devices detailed in Chapter 4. The same format is adopted in the Results and Discussion section, for easy reference purposes.

5.1 The Planar Doped Barrier Diode.

This section on the PDB diode includes the BUD and punch-through diode, as they are a result of the investigation into the PDB.

5.1.1 Isolation

One important area of research in this thesis has been process reproducibility. Current methods of manufacture of the PDB inflict unacceptable levels of variability on final device performance from wafer to wafer, and even from die to die. The first experiment outlined here was designed to address the element of process that directly affects the device area, i.e. the etch.

Typical PDB layer structures were grown by MBE, with the intention of fabricating implant isolated diodes with an effective ‘mesa’ diameter of 10 - 25μm (the mask plate contained several dot diameters) and total grown layer depth of 1.3μm respectively. For fabrication of the implant isolated devices, process steps 1-15 in section 4.4.1 are eliminated. The rest of the PDB diode fabrication process was followed to the end, with the addition of 2 further steps, as follows:

(a) Mount wafer face-up on an insulating plate using wax
(b) Electro-plate top contacts with 5 µm gold.

This process was designed by the author to result in a self-aligned implant isolation, using the electro-plated top contact as the implantation mask for the active layers. The resultant SiO₂ layer from the initial contact formation process was of thickness 0.81 µm. Isolating ions must, therefore, penetrate this layer before entering the GaAs. The oxide was in fact grown to a greater thickness than normal, as it allows us to place the peak of the lowest energy damage profile at the semiconductor surface. This was necessary as the available ion implanters do not have very low energy capability.

5.1.2 Implanter modification

A Lintott II ion implanter was then modified for the implantation of protons. The implanter is normally used only for implantation of ions derived from solid sources with the aid of a plasma support argon gas source. The configuration of gas lines and sources used is shown in figure 5.1.
The implanter was later shown to be capable of beam current densities well in excess of $10 \mu A \text{ cm}^{-2}$ scanned over a square inch aperture.

Samples were implanted with protons to a dose and energy shown in table 5.1.

**Table 5.1 Implanted proton doses and energies.**

<table>
<thead>
<tr>
<th>Sample ID</th>
<th>Implanted dose at each energy (cm$^{-2}$)</th>
<th>Implantation Energies (keV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDB1</td>
<td>$10^{14}$</td>
<td>185,220,280,350</td>
</tr>
<tr>
<td>PDB2</td>
<td>$10^{14}$</td>
<td>185,220,280,350</td>
</tr>
<tr>
<td>PDB3</td>
<td>$10^{15}$</td>
<td>185,220,280,350</td>
</tr>
</tbody>
</table>

The I-V characteristics of the implanted samples were assessed on a curve tracer, dividing the sample into four areas for measurement. A single die was chosen in each area and the
largest and second largest devices on the die were assessed. Measurements taken were forward voltage at 100 μA, reverse voltage at 100 μA, and forward resistance between 10 and 20 mA. Wafers were then subjected to annealing at 290°C as recommended by Pearton [60] to eliminate hopping conduction. Complementary devices were fabricated using the standard PDB process and were labelled PDB4. All devices were subjected to DC test on-wafer, and were then diced into single devices and packaged into leadless inverted device (LID) structures for RF assessment. Intermediate frequency noise figure (IFNF) and tangential sensitivity were measured, each at a frequency of 9.375 GHz.

The thermal stability of the devices became a concern, as demonstrated in the results and discussion section, identifying the need for more thermally stable implantation induced damage. Boron was chosen as the isolating ion, as it induces damage thermally stable to around 400°C, a temperature commensurate with the contact alloying process. The use of this ion species could mean that the contact alloying stage and the damage anneal can be performed in one step.

5.1.3 Boron implants for isolation

The proton implantation experiment was replicated using boron ions, except of course for the implantation schedule given in table 5.2. Annealing was performed at 400°C for 15 minutes in H₂ ambient, an identical anneal schedule to the contact alloy cycle.
The results given in sections 6.1.1 - 6.1.5 encouraged the industrial collaborators to treat the system developed with some seriousness. Up until then experiments had been performed on sub-standard material (of relatively high barrier height). DC results still varied to a small extent from sample to sample by ten per cent or less, although not to the same extent as results from samples which were wet chemical-etched. One possibility for the variability was in the area of the electroplated contacts, hence, the following experiment was devised.

A blanket layer of AZ4500 resist was spun-on to a sacrificial GaAs wafer, and soft baked. It was then implanted with $10^{14}$ B$^+$ ions cm$^{-2}$ at a beam current density of 0.2 μA cm$^{-2}$ at an energy of 2 MeV. The wafer was then stripped of resist, and SIMS was performed, analyzing the sample for boron contamination. No boron was found. Hence, the resist layer contained all of the implanted ions, and the resist thickness was sufficient for an implantation mask.

Process steps 16-26 in section 4.4.1 were performed on new low-barrier height device compatible material, followed by:
HMDS vapour ambient 7 minutes
Spin on AZ4500 resist 200 rpm 30 seconds
Develop
UV ozone clean
Ion implant according to PDB6 in table 5.2
Resist strip
Then steps 27-32

After the AZ4500 resist has been spun-on, the resultant wafer is patterned with Au/Ge/Ni contacts, on top of which are photoresist plateaux, of slightly larger diameter, and 7μm thickness. These plateaux serve as the implantation mask. The self-aligned process is hence dispensed with in this case.

5.1.4 Doping

Experiments on the PDB diode described so far focus on control of the electrically active area of the device. The other problem addressed here is the doping control of the thin p-type region within the n-i-n sandwich. The approaches taken do not achieve the goals in full, but go some way to the development of an entirely new process. The total elimination of epitaxy in the device manufacture was not an aim, and is not seen by the author as a realistic goal. Rather, the potential advantage of precision doping by ion implantation is being investigated.
The need for a relatively thick (>0.3 μm) region in GaAs for the formation of evaporated and sintered ohmic contacts is a major factor in defining the operating window of ion dose, energy and species.

5.1.5 Si, Mg, and P co-implants

An investigation was firstly undertaken to assess the possibility of co-implantation of a 'p'-type and an 'n'-type species for flexibility and control of the device barrier height. A wafer was grown by MBE with the doping profile shown in figure 5.2.

**Figure 5.2. n-i-n doping profile**

Substrate $3 \times 10^{18}$ cm$^{-3}$ 'n'-type

Low-doped region $5 \times 10^{16}$ cm$^{-3}$ 'n'-type, 1 μm thickness

Contact region $3 \times 10^{18}$ cm$^{-3}$ 'n'-type, 0.5 μm thickness
Silicon\textsuperscript{29}, phosphorus\textsuperscript{31} and magnesium\textsuperscript{24} were co-implanted according to the conditions given in table 5.3.

Table 5.3 Co-implanted doses and energies for P\textsuperscript{31}, Si\textsuperscript{29} and Mg\textsuperscript{24}.

<table>
<thead>
<tr>
<th>Sample</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>P\textsuperscript{+} dose (x10\textsuperscript{13} cm\textsuperscript{-2})</td>
<td>1.5</td>
<td>3</td>
<td>1.5</td>
<td>3</td>
<td>1.5</td>
<td>3</td>
</tr>
<tr>
<td>P\textsuperscript{+} energy keV</td>
<td>600</td>
<td>600</td>
<td>600</td>
<td>600</td>
<td>600</td>
<td>600</td>
</tr>
<tr>
<td>Mg\textsuperscript{+} dose (x10\textsuperscript{13} cm\textsuperscript{-2})</td>
<td>1.5</td>
<td>3</td>
<td>1.5</td>
<td>3</td>
<td>1.5</td>
<td>3</td>
</tr>
<tr>
<td>Mg\textsuperscript{+} energy keV</td>
<td>420</td>
<td>420</td>
<td>420</td>
<td>420</td>
<td>420</td>
<td>420</td>
</tr>
<tr>
<td>Si\textsuperscript{+} dose (x10\textsuperscript{13} cm\textsuperscript{-2})</td>
<td>4.8</td>
<td>4.8</td>
<td>4.8</td>
<td>4.8</td>
<td>4.8</td>
<td>4.8</td>
</tr>
<tr>
<td>Si\textsuperscript{+} energy keV</td>
<td>410</td>
<td>410</td>
<td>430</td>
<td>430</td>
<td>450</td>
<td>450</td>
</tr>
</tbody>
</table>

Prior to annealing in a double graphite strip heater [81], samples were encapsulated with 500\textgreek{A} of PECVD Si\textsubscript{3}N\textsubscript{4}. For each sample the anneal temperature/time was 900\textdegree C for 10s. Encapsulant removal was achieved by immersion of the samples in concentrated HF.

SIMS was performed on samples before and after annealing, and PDB diode structures were fabricated from 15x15mm samples.

The results yielded by the SIMS dictated a change in direction, as discussed in chapter 6, section 6.1.8. The conclusion was that a simpler implantation procedure was required, so three GaAs wafers were grown by MBE with the structure shown in figure 5.3.
Substrate $3 \times 10^{18}$ cm$^{-3}$ 'n'-type

Low doped region $5 \times 10^{16}$ 'n'-type, 1.65$\mu$m thickness

Contact region $3 \times 10^{18}$ cm$^{-3}$, 0.3$\mu$m thickness

5.1.6 Mg and P co-implants

The aim this time was to achieve the 'p'-type spike in the low-doped region using the tail of the Mg$^+$ implant, spilling over from the contact region where most of the Mg profile resided. This type of n-p-i-n structure is a bulk unipolar diode, or a PDB with the narrow intrinsic region of zero thickness, a camel diode. This maximized layer asymmetry also maximizes asymmetry of the I-V characteristic. Phosphorus and magnesium were implanted according to the energies and doses shown in table 5.4.
Table 5.4 Implanted Mg and P doses and energies.

<table>
<thead>
<tr>
<th>Sample</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>P⁺ dose (cm⁻²)</td>
<td>1x10¹⁴</td>
<td>1x10¹⁴</td>
<td>1x10¹⁴</td>
<td>1x10¹⁴</td>
</tr>
<tr>
<td>P⁺ energy (keV)</td>
<td>280</td>
<td>280</td>
<td>280</td>
<td>280</td>
</tr>
<tr>
<td>Mg⁺ dose (cm⁻²)</td>
<td>1x10¹⁴</td>
<td>1x10¹⁴</td>
<td>1x10¹⁴</td>
<td>1x10¹⁴</td>
</tr>
<tr>
<td>Mg⁺ energy (keV)</td>
<td>140</td>
<td>160</td>
<td>180</td>
<td>200</td>
</tr>
</tbody>
</table>

Confidence in the ability of a phosphorus co-implant to eliminate diffusional broadening of the magnesium implant during annealing was by now so complete that it was only seen necessary to take SIMS profiles of post-anneal samples. Samples were annealed in a double graphite strip heater at 800°C for 10s. Resultant SIMS profiles are given in section 6.1.8 of chapter 6. It is known that a doping-width product (DWP) in the thin ‘p’-type region of 3x10¹¹ cm⁻² corresponds to a diode barrier height of ~ 0.5eV. The SIMS profiles showed that even in the lowest energy case, the dose would have to be reduced to ~10% of the dose used, ie. around 10¹³ ions cm⁻². Another parameter governing the ion dose is of course the amount of compensation in the contact region due to the implanted ‘p’-type dopant. Levels would be unacceptably high unless the implanted dopant dose was kept to around 2x10¹³ cm⁻² or less.

On the basis of these results further implants into the 2nd and 3rd wafers were carried out for the purpose of device fabrication. Doses and energies are given in Table 5.5.
Samples 5-8 were implanted to a dose and energy expected to yield a BUD barrier height around 0.5V. Samples 1-4 were implanted to a dose and energy more likely to be correct if the SIMS measurements in section 6.1.8 of chapter 6 were incorrect to the extent that the silicon profile were actually 20% higher, and the magnesium profile were 20% lower-the worst case error.

All the samples were then encapsulated with 500Å Si₃N₄, and annealed at 800°C for 10s. The encapsulant was removed in concentrated HF, and samples were rinsed in de-ionized water. The samples then underwent the whole PDB diode fabrication process using wet chemical etching as the isolation technique, due to time constraints. DC I-V testing followed.

### 5.2 The Graded-Gap Gunn Diode

The Gunn diode is also a device that suffers from mesa etch non-uniformity. Variations in effective junction area have a direct effect on device resistance and capacitance, leading to variable output power, and poor impedance matching to microwave circuits. Typical
Mesa diameters of these devices vary between 50\(\mu m\) for a low power device, to 100\(\mu m\) for an Integral Heat Sink structure. Thermal stability of an isolating implant is a serious issue, due to the operating temperatures of the active layers in the high power devices, which can be in excess of 300\(^\circ\)C.

One point of contention with our industrial collaborators during the project was the potential of implant isolation for the manufacture of Gunn diodes. Concerns ranged from whether the encapsulation of the device in GaAs would affect its power output, to whether noise generated by conduction through the lateral straggle of the implant would affect the characteristics of the device at microwave frequencies.

5.2.1 Gunn diode proton isolation

The simplest way to address the questions asked was to create a structure compatible with a self-aligned proton implant. A simple low-power graded-gap Gunn diode structure was fabricated identical to that shown in figure 5.4.
The 5μm-thick gold top contact is a normal feature of the device, as is the SiO₂ layer. Coincidentally, the top contact is of sufficient thickness to act as an implantation mask, and the SiO₂ layer easily facilitates ion stopping at the semiconductor surface at low to medium energy. The low-doped transit region is sufficiently thick and well defined to allow adjustment of the implantation doses on the basis of simulation only, with a significant saving of beam time. Beam current density was <2μA cm⁻². The proton doses
and energies are listed in Table 5.5. The process steps eliminated are those associated with
the wet chemical etch.

Table 5.5 Proton doses and energies for the isolation of a graded-gap Gunn diode.

<table>
<thead>
<tr>
<th>Proton Energy (keV)</th>
<th>Proton Dose (cm$^{-2}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>80</td>
<td>$5 \times 10^{14}$</td>
</tr>
<tr>
<td>130</td>
<td>$5.1 \times 10^{14}$</td>
</tr>
<tr>
<td>180</td>
<td>$5.24 \times 10^{14}$</td>
</tr>
<tr>
<td>230</td>
<td>$5.39 \times 10^{14}$</td>
</tr>
<tr>
<td>280</td>
<td>$5.55 \times 10^{14}$</td>
</tr>
<tr>
<td>330</td>
<td>$5 \times 10^{12}$</td>
</tr>
<tr>
<td>380</td>
<td>$5.4 \times 10^{12}$</td>
</tr>
</tbody>
</table>

A second sample was also implanted in the same way, with the two highest energy doses
a factor of 10 greater. The resultant wafers were then assessed for DC isolation, diced,
and packaged. Testing at microwave frequencies was performed as described in section
4.5.5.

5.2.2 IHS Gunn diode

The success of these preliminary trials gave justification for serious modification of the
IHS Gunn diode fabrication routine which included the design of a new mask set, to
compensate for the lack of 'undercut' caused by the implant isolation, and the lack of
process variation. This mask consisted of a simple 3x3 matrix of 80μm diameter dots,
which were aligned in between the deep etched grids, over a positive resist layer of 7µm thickness. After developing, the result was a sample covered with 7 µm thick dots of resist, of 80µm diameter. These served as the implantation mask. An oxygen implantation scheme was chosen, due to the thermal stability of the resultant damage. Layer thicknesses were the same as in the case of the low power Gunn diode structure described in section 4.4.2 of chapter 4. Table 5.6 gives the ion energies and doses used.

Table 5.6 Oxygen ion implant isolation scheme.

<table>
<thead>
<tr>
<th>Oxygen ion energy (MeV)</th>
<th>Ion dose (x10^{13} cm^{-2})</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.3</td>
<td>0.6</td>
</tr>
<tr>
<td>1</td>
<td>0.7</td>
</tr>
<tr>
<td>2</td>
<td>0.8</td>
</tr>
<tr>
<td>3</td>
<td>0.9</td>
</tr>
<tr>
<td>4</td>
<td>1</td>
</tr>
</tbody>
</table>

Although implant isolation had been achieved, the devices were still mesa etched, in order that the resultant die fitted into the package, i.e. process step 17 in section 4.4.3 was performed.

5.3 The Varactor diode

This section encompasses experiments performed with the diffusion of an implanted ‘p’-type dopant in GaAs-namely zinc, although it is thought to be valid for and applicable to other ‘p’-type dopants in GaAs. The object of the exercise is to compare the diffusion,
up upon annealing, of the implanted zinc with a superimposed phosphorus co-implant, with the diffusion when the phosphorus is implanted into the tail of the zinc profile. The carrier profiles measured using the differential Hall effect technique are correlated to the C-V behaviour of the resultant varactor diodes, and their breakdown voltages. SIMS profiles were also obtained, yielding differences between atomic distribution profiles and carrier profiles.

Two GaAs wafers were grown by Vapour Phase Epitaxy (VPE) at GEC-Plessey Semiconductors, Lincoln to the following specification:

<table>
<thead>
<tr>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate</td>
</tr>
<tr>
<td>Low-doped layer</td>
</tr>
</tbody>
</table>

3 x 10^{18} cm^{-3} n-type sulphur doped
1 x 10^{16} cm^{-3} n-type sulphur doped 2.6μm thickness

5.3.1 Zinc and phosphorus co-implants

The wafers were then labelled V1 and V2 and co-implanted with zinc and phosphorus ions to the dose and energy given in table 5.7. Two semi-insulating GaAs wafers were also implanted, one (VR1) identically to V1, and the other (VR2) identically to V2. In each case the P⁺ ions were implanted first, so that the channelling tail of the zinc would be reduced. One small piece of identical n-n⁺ material was also implanted to the same dose and energy of zinc, but with no phosphorus co-implant.
Table 5.7 Implanted doses and energies of Zn\(^+\) and P\(^+\) for diffusion control experiment.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>V1 (VR1)</th>
<th>V2 (VR2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>P(^+) Dose (cm(^{-2}))</td>
<td>(7 \times 10^{14})</td>
<td>(7 \times 10^{14})</td>
</tr>
<tr>
<td>P(^+) Energy (keV)</td>
<td>72</td>
<td>330</td>
</tr>
<tr>
<td>Zn(^+) Dose (cm(^{-2}))</td>
<td>(7 \times 10^{14})</td>
<td>(7 \times 10^{14})</td>
</tr>
<tr>
<td>Zn(^+) Energy (keV)</td>
<td>140</td>
<td>140</td>
</tr>
</tbody>
</table>

After implantation a Si\(_3\)N\(_4\) encapsulant of 500Å thickness was grown by PECVD on each wafer. The semi-insulating wafers were then divided into 6mm squares, and V1 and V2 were divided into 15mm squares which were then processed according to the varactor diode fabrication process given in the techniques section. Reverse and forward breakdown voltages were assessed, along with C-V characteristics.

Two 6mm square samples from each of VR1 and VR2 were then annealed under vacuum (<10\(^{-1}\) Torr) in a double graphite strip heater. Anneal temperatures and times are given in Table 5.8.

Table 5.8 Anneal temperatures and durations

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>700</th>
<th>750</th>
<th>800</th>
<th>850</th>
<th>900</th>
<th>950</th>
<th>1000</th>
<th>700</th>
</tr>
</thead>
<tbody>
<tr>
<td>Time (s)</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>900</td>
</tr>
</tbody>
</table>

Encapsulant removal was achieved by immersion of samples in concentrated HF (48%) until de-wetting occurred.
5.3.2 Profile assessment

Samples were then prepared into the Van Der Pauw geometry for Differential Hall effect measurements in order to ascertain the carrier and mobility distribution profiles, and sheet resistivities.

SIMS analysis was carried out at Loughborough university on corresponding samples to reveal the atomic zinc distribution profiles in a Cameca system (model number ims3f), using a Cs\(^+\) primary ion beam. Zn was detected as the CsZn\(^+\) molecular ion, and phosphorus was detected as P\(^+\). The impact energy of the Cs\(^+\) beam was 5.5 keV and 14.5 keV for the zinc and phosphorus analysis respectively. The analyzed area for both conditions was 60µm diameter.
6. Results and Discussion

This chapter describes the outcome of the experiments and includes discussion, interpretation and comparisons with published data where available. The order of presentation in the experimental section is retained.

6.1 The planar doped barrier diode, bulk unipolar diode, and the punch-through diode

6.1.1 DC measurement on proton implanted structures

The I-V characteristic of diode structures on PDB1 indicated that there was little isolation between devices i.e. the device was short-circuit. PDB2 and PDB3 gave an I-V characteristic showing little deviation from that of the mesa isolated sample. However, following annealing at 290°C for 20 minutes (close to the contact alloying conditions) in an H₂ ambient, DC I-V measurements revealed that the isolation achieved in PDB2 had been annealed out, but that the I-V characteristic of PDB3 remained essentially unchanged. These results are an excellent demonstration of, and in general agreement with those previously published by Ascherton, and Pearton et al, in terms of ion dose [56], thermal stability of implant-induced damage [67], and doping density of pre-implanted material [76].
Table 6.1 below summarises the results of I-V measurements on the largest and second-largest device from each die, taken from PDB3 and PDB2, pre and post-anneal in the case of PDB3, and just pre-anneal in the case of PDB2, due to its failure after annealing. Also included are results for PDB4, the wet chemical etched sample. The cost and difficulty of manually processing these devices to the packaging stage meant that only a limited quantity were produced, precluding detailed statistical analysis. However more measurements were performed on-wafer, revealing that greater uniformity had been achieved than in the case of the wet chemically-etched mesa devices.

6.1.2 Proton isolation assessment

The reader should refer to table 5.1 for proton implant parameters of PDB1, 2, and 3. One immediately obvious point to note from the results presented in table 6.1 is the smaller spread in the device resistances of the implant isolated diodes, in comparison to the mesa structures. This suggests that the uniformity of the total device area improved from device to device. Variations in $V_F$ and $V_R$ (forward and reverse voltages at 100μA current) are not explicable in terms of variations in device area and are more likely to be due to variations in barrier height from one part of the wafer to another, i.e. growth non-uniformity, probably in the p$^+$ spike region. There is the second possibility that the mesa devices suffered partial contact failure, in which case no conclusions regarding improvements in the uniformity of the area may be drawn. Other interesting points to note are the consistently higher resistances associated with pre-annealed devices on PDB3, compared to those on PDB2, suggesting partial conduction in the material surrounding PDB2. Evidence for this interpretation is furthered by the post-anneal failure of PDB2.
The forward resistance of PDB3 was seen to increase after annealing, which is likely to be due to elimination of hopping states at the periphery of the devices, which constitutes further evidence that the anneal has improved the isolation. The post-annealed PDB3 samples exhibited 19% variation in device resistance, in comparison to 39% variation for the mesa etched (PDB4) samples.

The lower resistance values seen in the implant isolated samples is interpreted as evidence that the 'undercut' effect of the isolating implant is reduced compared with that obtained after wet chemical etching, which is isotropic. This result is supported by simulations performed using the TRIM code, which indicates an undercut of approximately 0.4μm for 350 keV protons.

Slight variations from one side of the wafer to the other could be attributed to non-uniformity arising from the implanter scanning system. Figure 6.1 represents an ion beam current profile, in the horizontal direction as an illustration of how ion dose can potentially vary across a wafer. Although the scanning profile shown is in the x-direction (horizontal), it may be similar in the vertical direction. The variation in beam current across the target is of the order a few per cent.
### Table 6.1 I-V characteristics of proton implant isolated and mesa etched PDB diodes

<table>
<thead>
<tr>
<th>Wafer</th>
<th>( V_F ) @ 100( \mu )A (V)</th>
<th>( V_R ) @ 100( \mu )A (25( \mu )m device)</th>
<th>( R_D ) 10-20 mA (Ω)</th>
<th>( V_F ) @ 100( \mu )A (21( \mu )m device)</th>
<th>( V_R ) @ 100( \mu )A (21( \mu )m device)</th>
<th>( R_D ) 10-20 mA (21( \mu )m device)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDB2 pre-anneal</td>
<td>.27</td>
<td>2.9</td>
<td>12</td>
<td>.28</td>
<td>3.1</td>
<td>14</td>
</tr>
<tr>
<td>PDB3 pre-anneal</td>
<td>.29</td>
<td>3.1</td>
<td>15.5</td>
<td>.31</td>
<td>3.2</td>
<td>19.2</td>
</tr>
<tr>
<td>PDB3 post-anneal</td>
<td>.28</td>
<td>3</td>
<td>17.8</td>
<td>.29</td>
<td>3</td>
<td>19.5</td>
</tr>
<tr>
<td>PDB4</td>
<td>.31</td>
<td>3.3</td>
<td>27.2</td>
<td>.33</td>
<td>3.5</td>
<td>26.8</td>
</tr>
<tr>
<td>PDB2 pre-anneal</td>
<td>.28</td>
<td>2.9</td>
<td>12</td>
<td>.27</td>
<td>2.9</td>
<td>13.5</td>
</tr>
<tr>
<td>PDB3 pre-anneal</td>
<td>.27</td>
<td>2.9</td>
<td>13</td>
<td>.28</td>
<td>3.1</td>
<td>16</td>
</tr>
<tr>
<td>PDB3 post-anneal</td>
<td>.27</td>
<td>2.9</td>
<td>15.6</td>
<td>.28</td>
<td>2.9</td>
<td>18.1</td>
</tr>
<tr>
<td>PDB4</td>
<td>.31</td>
<td>3.2</td>
<td>19.8</td>
<td>.34</td>
<td>3.5</td>
<td>29</td>
</tr>
<tr>
<td>PDB2 pre-anneal</td>
<td>.27</td>
<td>2.8</td>
<td>12</td>
<td>.28</td>
<td>3</td>
<td>14</td>
</tr>
<tr>
<td>PDB3 pre-anneal</td>
<td>.27</td>
<td>2.9</td>
<td>14</td>
<td>.29</td>
<td>3.1</td>
<td>17</td>
</tr>
<tr>
<td>PDB3 post-anneal</td>
<td>.3</td>
<td>3.1</td>
<td>19.6</td>
<td>.3</td>
<td>3.2</td>
<td>20.7</td>
</tr>
<tr>
<td>PDB4</td>
<td>.29</td>
<td>3.1</td>
<td>17.1</td>
<td>.33</td>
<td>3.5</td>
<td>26.1</td>
</tr>
<tr>
<td>PDB2 pre-anneal</td>
<td>.28</td>
<td>3</td>
<td>13</td>
<td>3.1</td>
<td>2.2</td>
<td>16</td>
</tr>
<tr>
<td>PDB3 pre-anneal</td>
<td>.3</td>
<td>3.2</td>
<td>17</td>
<td>.32</td>
<td>3.4</td>
<td>22</td>
</tr>
<tr>
<td>PDB3 post-anneal</td>
<td>.29</td>
<td>3</td>
<td>18.6</td>
<td>.3</td>
<td>3.2</td>
<td>20.3</td>
</tr>
<tr>
<td>PDB4</td>
<td>.3</td>
<td>3.2</td>
<td>19.9</td>
<td>.32</td>
<td>3.4</td>
<td>40.2</td>
</tr>
</tbody>
</table>
Figure 6.1. A nominal ion beam current profile as a function of distance scanned across a target.

Under normal operating conditions the scanned beam would pass through an aperture in the sample chamber, so the extremities of the above profile could be removed, to give a closer representation to the ideal profile.

6.1.4 RF Measurements

The post-anneal PDB3 wafer and the mesa isolated sample were diced into single devices and packaged into Leadless Inverted Device (LID) structures for assessment at microwave frequency. The intermediate frequency noise figure (IFNF) was measured with the diodes operating as mixers at 9.375 GHz, each carrying a rectified current of 1.5 mA. Mesa isolated devices gave an IFNF of between 7 and 7.4 dB, with proton implant isolated devices giving consistently lower IFNFs of between 6.4 and 7 dB. Tangential sensitivity to a 1kHz-modulated signal revealed a value of -54dBm for the implant isolated samples,
compared to a slightly worse value of -51dBm for the wet chemical etched samples. Differences observed in the performance of mesa and implant isolated samples could possibly be attributed to variances in impedance matching to the measurement circuit. The greater undercutting of the wet etch compared to the lateral straggle of the isolating implant is certain to result in greater device impedances. Confidence in the isolation system led to the development of the boron isolation scheme described in the experimental section.

6.1.5 Boron implant isolation assessment

The reader should refer to table 5.2 for boron implantation parameters of PDB 5, 6, and 7.

Table 6.2 shows the measured DC parameters of the boron implant isolated samples.

Table 6.2 Boron implant isolated PDBs. DC I-V parameters.

<table>
<thead>
<tr>
<th>Wafer</th>
<th>$V_F$ @ 100µA</th>
<th>$V_R$ @ 100µA</th>
<th>$R_D$ 10-20</th>
<th>$V_F$ @ 100µA</th>
<th>$V_R$ @ 100µA</th>
<th>$R_D$ 10-20</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(V)</td>
<td>(V)</td>
<td>(mA (Ω))</td>
<td>(V)</td>
<td>(V)</td>
<td>(mA (Ω))</td>
</tr>
<tr>
<td></td>
<td>(25µm device)</td>
<td>(25µm device)</td>
<td>(25µm device)</td>
<td>(21µm device)</td>
<td>(21µm device)</td>
<td>(21µm device)</td>
</tr>
<tr>
<td>PDB6 pre-anneal</td>
<td>.28</td>
<td>2.9</td>
<td>12</td>
<td>.28</td>
<td>3.1</td>
<td>14</td>
</tr>
<tr>
<td>PDB7 pre-anneal</td>
<td>.28</td>
<td>3</td>
<td>12</td>
<td>.29</td>
<td>3.2</td>
<td>14</td>
</tr>
<tr>
<td>PDB8 pre-anneal</td>
<td>.28</td>
<td>3</td>
<td>12</td>
<td>.29</td>
<td>3.2</td>
<td>14</td>
</tr>
<tr>
<td>PDB6 post-anneal</td>
<td>.28</td>
<td>3</td>
<td>12</td>
<td>.28</td>
<td>3.2</td>
<td>13</td>
</tr>
<tr>
<td>PDB7 post-anneal</td>
<td>.28</td>
<td>3</td>
<td>12</td>
<td>.29</td>
<td>3.2</td>
<td>13</td>
</tr>
<tr>
<td></td>
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<td>---</td>
</tr>
<tr>
<td>PDB8 post-anneal</td>
<td>.28</td>
<td>3</td>
<td>12</td>
<td>.29</td>
<td>3.1</td>
<td>14</td>
</tr>
<tr>
<td>PDB6 pre-anneal</td>
<td>.28</td>
<td>3</td>
<td>12</td>
<td>.29</td>
<td>3.1</td>
<td>14</td>
</tr>
<tr>
<td>PDB7 pre-anneal</td>
<td>.28</td>
<td>3.1</td>
<td>12</td>
<td>.3</td>
<td>3.2</td>
<td>14</td>
</tr>
<tr>
<td>PDB8 pre-anneal</td>
<td>.28</td>
<td>3.1</td>
<td>12</td>
<td>.29</td>
<td>3.2</td>
<td>14</td>
</tr>
<tr>
<td>PDB6 post-anneal</td>
<td>.28</td>
<td>3.1</td>
<td>12</td>
<td>.29</td>
<td>3.2</td>
<td>14</td>
</tr>
<tr>
<td>PDB7 post-anneal</td>
<td>.28</td>
<td>3</td>
<td>12</td>
<td>.29</td>
<td>3.2</td>
<td>14</td>
</tr>
<tr>
<td>PDB8 post-anneal</td>
<td>.28</td>
<td>2.9</td>
<td>12</td>
<td>.29</td>
<td>3.1</td>
<td>14</td>
</tr>
<tr>
<td>PDB6 pre-anneal</td>
<td>.28</td>
<td>3</td>
<td>12</td>
<td>.29</td>
<td>3.1</td>
<td>14</td>
</tr>
<tr>
<td>PDB7 pre-anneal</td>
<td>.28</td>
<td>3.1</td>
<td>12</td>
<td>.29</td>
<td>3.2</td>
<td>14</td>
</tr>
<tr>
<td>PDB8 pre-anneal</td>
<td>.28</td>
<td>3.1</td>
<td>12</td>
<td>.29</td>
<td>3.2</td>
<td>14</td>
</tr>
<tr>
<td>PDB6 post-anneal</td>
<td>.28</td>
<td>3.0</td>
<td>12</td>
<td>.29</td>
<td>3.1</td>
<td>14</td>
</tr>
<tr>
<td>PDB7 post-anneal</td>
<td>.28</td>
<td>3</td>
<td>12</td>
<td>.29</td>
<td>3.2</td>
<td>15</td>
</tr>
<tr>
<td>PDB8 post-anneal</td>
<td>.28</td>
<td>3</td>
<td>12</td>
<td>.29</td>
<td>3.1</td>
<td>13</td>
</tr>
<tr>
<td>PDB6 pre-anneal</td>
<td>.28</td>
<td>3</td>
<td>12</td>
<td>.28</td>
<td>3.1</td>
<td>14</td>
</tr>
<tr>
<td>PDB7 pre-anneal</td>
<td>.28</td>
<td>3</td>
<td>12</td>
<td>.29</td>
<td>3.2</td>
<td>14</td>
</tr>
<tr>
<td>PDB8 pre-anneal</td>
<td>.28</td>
<td>2.9</td>
<td>12</td>
<td>.29</td>
<td>3.2</td>
<td>14</td>
</tr>
<tr>
<td>PDB6 post-anneal</td>
<td>.28</td>
<td>2.9</td>
<td>12</td>
<td>.29</td>
<td>3.1</td>
<td>14</td>
</tr>
<tr>
<td>PDB7 post-anneal</td>
<td>.28</td>
<td>3.1</td>
<td>12</td>
<td>.29</td>
<td>3.2</td>
<td>14</td>
</tr>
<tr>
<td>PDB8 post-anneal</td>
<td>.28</td>
<td>3</td>
<td>12</td>
<td>.29</td>
<td>3.2</td>
<td>14</td>
</tr>
</tbody>
</table>
The results in table 6.2 suggest that the boron implant isolation scheme has achieved improved uniformity over that achieved using proton isolation. The 25\textmu m diameter device exhibited 100% uniformity in device area across the wafer for PDBs 6, 7 and 8. The electroplating technique is therefore not significantly detrimental to the across-wafer uniformity of the device performance. Another parameter was responsible for the lack of process uniformity in the proton isolation experiment. This may have been the lack of uniformity of the proton beam itself, allowing parallel conduction paths around the devices implanted at the periphery of the beam profile, so device resistances appear lower. Use of the proton beam and the modified accelerator was an inexpensive way of establishing the viability of implant isolation in the manufacture of PDBs, but the fully ‘manufacture friendly’ process lies with boron implants, as the contact alloying cycle is carried out at the same temperature as the anneal for the annihilation of hopping states. Electroplating of thick gold contact layers is not an inherent part of the PDB diode process, as it is in the production of low-power graded gap Gunn diodes. The plating must be performed prior to contact alloying in order for the post-implant anneal to include the contact anneal.

6.1.6 Masking with Photoresist

The final modification to the PDB diode process is to protect the evaporated contact with a photoresist mask of 7\textmu m thickness, for implant isolation. This can be achieved with relative ease, and is simpler and quicker than the electroplating process. Shadowing of the implant by the 7\textmu m plateau of photoresist is of the order 1.2 \textmu m when the wafer is tilted 7° away from the (100) plane, so the implant must be performed normal to the wafer.
surface. The risk of ion channeling is minimal as the layers are grown 3° off-axis, which is beyond the acceptance angle for high-energy boron ions into a channel.

### 6.1.7 Implantation of ‘p’-type dopant:

Table 5.3 is repeated below.

<table>
<thead>
<tr>
<th>Sample</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
</tr>
</thead>
<tbody>
<tr>
<td>P⁺ dose (x10¹³ cm⁻²)</td>
<td>1.5</td>
<td>3</td>
<td>1.5</td>
<td>3</td>
<td>1.5</td>
<td>3</td>
</tr>
<tr>
<td>P⁺ energy keV</td>
<td>600</td>
<td>600</td>
<td>600</td>
<td>600</td>
<td>600</td>
<td>600</td>
</tr>
<tr>
<td>Mg⁺ dose (x10¹³ cm⁻²)</td>
<td>1.5</td>
<td>3</td>
<td>1.5</td>
<td>3</td>
<td>1.5</td>
<td>3</td>
</tr>
<tr>
<td>Mg⁺ energy keV</td>
<td>420</td>
<td>420</td>
<td>420</td>
<td>420</td>
<td>420</td>
<td>420</td>
</tr>
<tr>
<td>Si⁺ dose (x10¹³ cm⁻²)</td>
<td>4.8</td>
<td>4.8</td>
<td>4.8</td>
<td>4.8</td>
<td>4.8</td>
<td>4.8</td>
</tr>
<tr>
<td>Si⁺ energy keV</td>
<td>410</td>
<td>410</td>
<td>430</td>
<td>430</td>
<td>450</td>
<td>450</td>
</tr>
</tbody>
</table>

### 6.1.8 Atomic distribution profiles of implanted PDB dopants

Figures 6.2-6.6 depict the SIMS profiles of samples 1 - 6 respectively, excluding sample 5, which was spoilt due to failure of the encapsulant during annealing. Samples 1-6 are the attempted PDB structures after annealing at 900°C for 10 seconds. No diffusion of the Mg⁺ implant is seen, due to the presence of phosphorus, as the annealed samples yield identical SIMS profiles to the ‘as-implanted’ samples. The purpose of the Si₂⁹ implant is to compensate a thin region of the Mg implant, in order to simulate the thin intrinsic region in the PDB layer structure.
Figure 6.2 SIMS profile of sample 1 from table 5.3

Figure 6.3 SIMS profile of sample 2 from table 5.3
Figure 6.4 SIMS profile of sample 3 from table 5.3

Figure 6.5 SIMS profile of sample 4 from table 5.3
Phosphorus profiles are not given, as these were undetectable against the background phosphorus levels in the machine, which is due to the regular analysis of InP by the facility.

All devices fabricated on these samples gave a high-resistance, ohmic characteristic, due, it is thought, to the failure of the Si₃N₄ encapsulant during annealing, and over-diffusion of the contact metal during alloying.

Discussion with Shannon (53,54,55) suggested that a better route might be to implant only the p-type dopant into a n-i-n structure, relying on the reproducibility of the thicker n⁺ contact region, resulting in the following approach:

6.1.9 Single dopant implants

A realistic alternative to the PDB is another member of the BUD family, the Camel diode. Implants of a 'p'-type dopant with correct doping density into a n⁺-n-n⁺ grown structure
could yield a spill-over region of charge into the near-surface $n^*-n$ interface, creating the classic $n^*-p-n-n^+$ camel diode structure[55]. Of course the diode quality in terms of forward resistance and ideality factor is likely to be poor, as, although the doping-width product in the ‘p’-type region can be correctly controlled, it will be a thicker, lower-doped region. This is because we will be utilizing the tail of the implant, as opposed to the peak. This scheme is shown in figures 6.7 - 6.11.

The n-i-n wafer described in section 5.2.2 was grown with a thinner contact region (0.3μm) in order to minimize the implant energy required for p-type doping. This has the overall effect of narrowing the ‘p’-type region in the device, due to the smaller channeling tail of the implanted species.

Figures 6.7-6.11 show the SIMS profiles of the four Mg$^+$-implanted structures after annealing at 800°C for 10 seconds, implanted with $10^{14}$ P$^+$ ions cm$^{-2}$ at 280keV, and $10^{14}$ Mg$^+$ ions at energies given.
Figure 6.9 180 keV

Figure 6.10 200 keV
It is immediately obvious that the doping density due to the Mg$^+$ implant is too high. The contact region will be fully compensated by its presence, assuming 100% activation of the implant. Implantation energies around 140 keV seem to be appropriate for the formation of a thin p-type region at the n$^+$-n$^-$ interface. Attempts were not made to fabricate devices on these samples, as they were not the desired profiles.

Figure 6.11 shows all four Mg and Si profiles superimposed. It is seen that a 20 keV increase in ion energy results in an increase of approximately 0.05 μm in ion range.

Fig. 6.11 Superposition of profiles 6.7 - 6.10
As a gross approximation, simulations of lower doses can be obtained by dividing the SIMS profile by a proportional denominator. Figure 6.12 is obtained by adjusting the SIMS data for the Mg⁺ implant in figure 6.7 by an order of magnitude.

Figure 6.12 Approximate simulation of $10^{13}$ Mg⁺ ions cm⁻² at 140 keV using SIMS data from a higher dose sample.

Inaccuracies arise from the approximation due to a number of factors, chiefly, the increase in ion channeling due to the lower dose of previously-implanted phosphorus, i.e. the lower dose of the phosphorus co-implant has introduced less lattice disorder, or has not pre-amorphized the sample surface, hence ion channeling may occur. Another important parameter is that, as the ion dose reduces, the effect as a compensator of the doping levels
in the low-doped 'n'-type region increases. Assuming the non-uniformity of doping-width product in the p-type region has been eradicated, a new problem has arisen which concerns the reproducibility of doping levels in the low-doped region.

The implants described in table 5.5 were carried out, yielding material on which devices could be made. I-V characteristics of some of the resultant diodes are given in figures 6.13 - 6.16 respectively.

It was expected that these results would demonstrate an increasing barrier height with increasing ion energy and dose. In fact, in every case except one, a punch-through diode has been formed. The simulation in figure 6.12 indicates the spill-over of the Mg+ implant into the low-doped layer, resulting in a p-type region, effectively doped at around $10^{17}$ holes cm$^{-3}$ over approximately 300Å (assuming 100% electrical activity). It is this region that is utilised to give the diode's potential barrier. The doping-width product in this area of the device is of the same order as that in a conventionally grown device ($3\times10^9$ holes cm$^{-3}$) although thicker by a factor of about 6. The presence of a p-type dopant in the contact layer is expected to compensate the electron concentration by ~ 10% in the worst case, resulting in a slightly detrimental effect on device resistance. Figure 6.13 shows the I-V characteristic of such a device, demonstrating the classic bulk unipolar diode turn on features. In comparison to devices fabricated from material implanted at higher dose and energy, the diode in figure 6.13 is leaky in reverse bias, a common trait of structures with a fully depleted acceptor region. All bulk unipolar diodes have a fully depleted acceptor region. Table 6.2 gives the forward knee voltages achieved relative to implanted dose and ion energy. Many of the characteristics obtained (especially those from samples implanted
with high dose and energy) deviate from the ideal diode model to such an extent that analysis based on the model would be meaningless. Barrier heights are, therefore, given as approximate forward knee voltages. The devices implanted at higher energy, are in fact not Camel diodes but 'punch-through' diodes [2]; devices in which the implanted p-type region is not fully depleted. At the two extremes of the measurement range, the reverse to forward current ratio varies between $10^{-9}$ for samples implanted with high dose and energy, and $10^{-6}$ for samples that received a lower dose and energy. The flattening of the curve seen at $10^{-2}$ amperes in 6.14 - 6.17 is due to the current threshold of the analysis equipment.

Figure 6.13 I-V characteristic of n-i-n structure implanted with $10^{13}$ cm$^{-2}$ Mg$^+$ ions at 125keV

An increase in implantation energy corresponds to an increase in the doping density of the acceptor region of the device. Figure 6.14 shows the I-V characteristic of a device
fabricated from the sample implanted with $10^{13}$ cm$^{-2}$ Mg$^+$ at 135keV. Although similar in appearance to the characteristic of the previous device, the kink in the curve at around 0.2V reveals that the device has an undepleted acceptor region (a punch-through diode), [2], in which the acceptor region is progressively depleted with increasing bias until fully depleted, at which point the device behaves as a BUD.

Increasing the dose to $2 \times 10^{13}$ Mg$^+$ at 135 keV (figure 6.15) results in a device which behaves as a punch-through diode at low bias (region 1), and, once the acceptor region is depleted at around 2 volts, behaves as a BUD (region 2), until the device is biased beyond the knee turn-on characteristic, (region 3) where series resistance is predominant.

Further increasing the doping-thickness product in the acceptor region was achieved by implanting $2 \times 10^{13}$ cm$^{-2}$ Mg$^+$ at 150keV, (figure 6.16). Increasing forward bias resulted in the familiar acceptor layer depletion characteristic in region 1, followed at higher bias by breakdown of the device, thought to be due to Zener breakdown of the near-surface n$^+$-p$^+$ junction where the field is high.

All the samples measured yielded across-wafer variability in barrier height. Since the devices produced are sensitive to both variations in the thickness and doping density in both the contact region and the low-doped n-type layer, it is likely that growth non-uniformity is responsible for these differences. This variability was made apparent from SIMS profiles of the samples, which revealed across wafer non-uniformity in the low-doped region resulting in differences in doping density of an order of magnitude.
Figure 6.14 I-V characteristic of n-i-n structure implanted with $10^{13}$ cm$^{-2}$ Mg$^+$ ions at 135 keV.

Figure 6.15 I-V characteristic of n-i-n structure implanted with $2 \times 10^{13}$ Mg$^+$ cm$^{-2}$ at 135 keV.
Figure 6.16 I-V characteristic of n-i-n structure implanted with $2 \times 10^{13} \text{cm}^{-2}$ Mg$^+$ at 150keV, exhibiting Zener breakdown.

Table 6.2 Forward knee and reverse breakdown voltage related to implanted Mg$^+$ dose and energy

<table>
<thead>
<tr>
<th>Mg$^+$ Dose ($\times 10^{13}$ ions cm$^{-2}$)</th>
<th>2</th>
<th>2</th>
<th>2</th>
<th>2</th>
<th>1</th>
<th>1</th>
<th>1</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy (keV)</td>
<td>135</td>
<td>140</td>
<td>145</td>
<td>150</td>
<td>125</td>
<td>130</td>
<td>135</td>
<td>140</td>
</tr>
<tr>
<td>Forward knee voltage (V)</td>
<td>3.5</td>
<td>4</td>
<td>8</td>
<td>4</td>
<td>0.8</td>
<td>1.2</td>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>Reverse Breakdown (V) at 1 µA</td>
<td>36</td>
<td>41</td>
<td>55</td>
<td>48</td>
<td>4</td>
<td>6</td>
<td>11</td>
<td>22</td>
</tr>
</tbody>
</table>

In conclusion, the viability of implant isolation as an alternative to wet chemical etching in the production of planar doped barrier diodes has been demonstrated. Additionally it has been shown that it is possible to introduce the p-type dopant into a grown n-i-n structure, and achieve a bulk unipolar diode structure with a corresponding I-V characteristic.
Combination of these two techniques would result in a device benefiting from all the uniformity advantages that ion implantation has to offer.
6.2 The Graded Gap Gunn diode.

The experiment described in section 5.3.1 of chapter 5, designed to isolate a graded-gap Gunn diode met with great success. Both mesa and implant isolated structures showed a threshold voltage of ~1.7V while carrying a current of ~450mA. The fundamental frequency of oscillation was in the region of 37 GHz frequency. A peak power of ~50mW was achieved at ~3.7V bias and 400mA forward current, implying an average efficiency of 3.4%. It should be noted that greater efficiencies are possible with graded-gap Gunn diodes operating at higher power, but such devices require more sophisticated heat sinking. The Integral Heat Sink (IHS) Gunn diode discussed next is one such device. The relatively simple measurement system employed, and the limited number of devices fabricated to final packaged state precludes a detailed statistical analysis of results.

The spectral noise voltage density calculated from noise amplitude 100kHz off carrier gave typical values of -80dB/Hz for both mesa and implant isolated samples; this is a measure of the attenuation of the emitted signal voltage at a spectral distance of 100kHz from the fundamental frequency, and describes the ‘roll-off’ in signal per Hz in dB. Fears that the implantation process would introduce excess noise have proved unfounded. Encapsulation of the device in ion-implanted GaAs does not seem to significantly impede the emission of electromagnetic power at microwave frequencies.

Further experimental detail is available in the resulting publication [14].

The experiment in section 5.3.2 to implant isolate an integral heat sink (IHS) Gunn diode also met with success. The resultant device structure is shown in figure 6.17.
The desired frequency of operation was 77 GHz, which was demonstrated by the control mesa sample. The implant isolated samples gave peak microwave power at 75 GHz, 2dB down in power from the mesa control samples. This is thought to be because of the parasitic capacitance in parallel with the device, due to the implant isolated regions between the gold heat sink contact, and the highly-doped substrate. The impedance match of the microwave cavity is likely to be poor, and is non-adjustable. In this particular case it has not been possible to simply fit an implant isolation stage into an existing process. The reluctance of the industrial collaborators to make further process modifications and experiment further has precluded total success for this particular process and device.
6.3 Varactor diodes

6.3.1 Zinc Distribution

The following section is a description and interpretation of the outcome of the experiment described in section 5.4.1-2 (Zn and P co-implantation) for control of the diffusion of p-type dopants during activation annealing.

Figure 6.18 is a SIMS profile of the zinc and phosphorus implants showing the relative positions of the high and low energy phosphorus profiles compared to that of the zinc. Slight misalignment of the zinc with the low energy phosphorus profile is seen, with the peak of the higher energy phosphorus implant beyond the tail of the zinc. This misalignment may, at least in part, be due to the different ion beam induced atomic mixing that occurs when using two different analysis conditions for zinc and phosphorus. No redistribution of the phosphorus is observed, even following annealing at 1000°C.

SIMS profiles of zinc implants after furnace annealing at 700°C for 15 minutes are shown in figure 6.19. In the case of the zinc with the shallow phosphorus implant it is evident that limited diffusion has occurred, with the zinc diffusing to occupy the phosphorus profile. The samples with the deep phosphorus co-implant, by comparison to the sample with no implanted phosphorus, show enhanced diffusion, thought to be due to the presence of greater concentrations of gallium vacancies around the projected range of the phosphorus implant.

Annealing at 800 and 1000°C for 15s has a markedly different effect on the final zinc distribution profile, depending on the phosphorus ion energy. Figure 6.20 shows the comparative SIMS profiles of the zinc as-implanted, and annealed at 800°C for 15s, for
the case of both the shallow and deep phosphorus co-implant. Profile broadening is apparent at 800°C with evidence of significant diffusion towards the surface, in the case of the deep P implanted sample, and more so at 1000°C, depicted in figure 6.21. Overall broadening is more prominent in the case of the deep phosphorus implanted samples. This is thought to be due to two factors; firstly, the relative lack of phosphorus present at the peak of the as-implanted zinc profile, and secondly, the presence of large concentrations of gallium vacancies in the tail of the zinc implant, due to the implant damage peak, causing enhanced diffusion of zinc towards them.

Figure 6.18. SIMS profiles of zinc and phosphorus as-implanted
Figure 6.19. SIMS profiles of Zinc co-implanted with phosphorus and annealed at 700°C for 15 minutes

Figure 6.20. SIMS profiles showing diffusion of zinc after annealing at 1000°C for 15 seconds
6.3.2 Carrier Profiles: Table 6.3 and 6.4 give the values of sheet carrier concentration, sheet resistivity, and sheet mobility, as a function of anneal temperature, for the samples with the shallow and deep phosphorus implants respectively.

Table 6.3. Sheet carrier concentration, mobility, and resistivity values for GaAs implanted with shallow phosphorus followed by zinc

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>750</th>
<th>800</th>
<th>850</th>
<th>900</th>
<th>950</th>
<th>1000</th>
<th>700</th>
</tr>
</thead>
<tbody>
<tr>
<td>Duration (s)</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>900</td>
</tr>
<tr>
<td>Rs (x10³ Ω/□ )</td>
<td>8.52</td>
<td>0.413</td>
<td>0.216</td>
<td>0.201</td>
<td>0.184</td>
<td>0.177</td>
<td>0.302</td>
</tr>
<tr>
<td>Ns (x10¹⁴ cm⁻²)</td>
<td>.725</td>
<td>4.11</td>
<td>5.53</td>
<td>5.83</td>
<td>6.33</td>
<td>6.39</td>
<td>3.88</td>
</tr>
<tr>
<td>μs (cm²/V-s)</td>
<td>10.1</td>
<td>36.7</td>
<td>52.3</td>
<td>53.2</td>
<td>53.3</td>
<td>55.2</td>
<td>52.3</td>
</tr>
</tbody>
</table>

Table 6.4. Sheet carrier concentration, mobility, and resistivity values for GaAs implanted with deep phosphorus followed by zinc

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>750</th>
<th>800</th>
<th>850</th>
<th>900</th>
<th>950</th>
<th>1000</th>
<th>700</th>
</tr>
</thead>
<tbody>
<tr>
<td>Duration (s)</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>15</td>
<td>900</td>
</tr>
<tr>
<td>Rs (x10³ Ω/□ )</td>
<td>.438</td>
<td>.256</td>
<td>.194</td>
<td>.174</td>
<td>.154</td>
<td>.136</td>
<td>.265</td>
</tr>
<tr>
<td>Ns (x10¹⁴ cm⁻²)</td>
<td>3.05</td>
<td>4.43</td>
<td>5.31</td>
<td>5.62</td>
<td>6.24</td>
<td>6.78</td>
<td>3.95</td>
</tr>
<tr>
<td>μs (cm²/V-s)</td>
<td>46.7</td>
<td>55.1</td>
<td>60.7</td>
<td>63.2</td>
<td>67.6</td>
<td>63.7</td>
<td>60.7</td>
</tr>
</tbody>
</table>

In both cases increasing activation efficiency is observed with increasing anneal temperature, until at 1000°C, efficiency reaches almost 100%, suggesting that little zinc is
lost to the Si$_3$N$_4$ cap by diffusion. One interesting point to note in table 6.3 is the increased activation efficiency exhibited by the sample annealed at 700°C for 15 minutes, over that of the sample annealed at 750°C for 15 seconds, demonstrating the time dependence of activation at lower anneal temperatures. Figure 6.21 shows the carrier and mobility profile of the sample with implants of zinc and shallow phosphorus, annealed at 700°C for 15 minutes. In comparison to the deep phosphorus-implanted sample (shown after annealing at 700°C for 900s) in figure 6.22 it is a shallow profile, with a peak carrier concentration at around 7x10$^{19}$ cm$^{-3}$. Lower mobility values at high carrier concentrations are thought to be due to ionised impurity scattering.

These profiles are virtually replicated at the lower RTA temperatures, but at temperatures near 1000°C, significant profile broadening occurs. After annealing at 1000°C for 15s, the carrier profile in the shallow phosphorus-implanted sample (fig. 6.23) has broadened toward and away from the surface. Peak carrier concentrations of 7x10$^{19}$ cm$^{-3}$ are seen near the surface, with a remarkable overall similarity to the as-implanted SIMS profile. The zinc has been almost entirely pinned in place by the phosphorus.

In contrast, the deep phosphorus-implanted profile in figure 6.24 shows that after 1000°C for 15s, the hole concentration peak has diffused to a depth of 0.25 µm, its carrier profile terminating within a distance of one or two measurement steps, (0.01 µm). Mobility values are improved due to lower peak carrier concentrations, and the sheet resistance is lower than the shallow phosphorus implanted sample due to a combination of higher mobility and greater p-type layer thickness.
Figure 6.21. Carrier and mobility profile of implants of zinc and shallow phosphorus, annealed at 700°C for 15 minutes.

Figure 6.22 Carrier and mobility profile of implants of zinc and deep phosphorus, annealed at 700°C for 15 minutes.
Figure 6.23 Carrier and mobility profile of implants of zinc and shallow phosphorus, annealed at 1000°C for 15s

Figure 6.24 Carrier and mobility profile of implants of zinc and deep phosphorus, annealed at 1000°C for 15s
A technique has thus been demonstrated to control both the thickness, and junction carrier profile of ion-implanted acceptor layers in GaAs.

An abrupt, highly doped profile may be achieved by the implantation of phosphorus at the tail of the acceptor implant before activation annealing. Alternatively, a non-abrupt, highly doped profile is possible if the phosphorus implant overlaps the zinc. Potential applications include the tailoring of p-n junction profiles, in any GaAs device where an ion-implanted p-n junction is required, and hence, tailoring their capacitance-voltage profiles and breakdown characteristics.

Figure 6.26 shows the doping profiles of two commonly used types of Schottky varactor diode (repeated from figure 3.10). The first, the abrupt varactor, is one in which the interface depletion width is narrow in comparison to the epilayer thickness. This type of profile provides a capacitance proportional to the inverse square root of the reverse bias voltage. The second, the hyperabrupt tuning varactor is a device with an exceptionally narrow depletion width at the surface due to the high doping density present, which reduces as it extends into the epilayer. This causes a rapid fall-off of capacitance as reverse bias is increased, with an inverse square capacitance relationship, due to the depletion width of the device increasing at an ever greater rate with applied bias. The most important factor affecting the device characteristic, is not whether the material the other side of the junction is a metal or a p-type semiconductor, but the shape of the barrier profile. In the case of the Schottky varactor, the barrier shape is dictated by the doping profile inside the semiconductor epilayer. In an implanted p'-n junction varactor, the barrier, and hence the tuning curve is affected by both the doping profile of the epilayer to
be implanted, and the final activated p-type doping profile. This is demonstrated by the results of the experiment described in section 5.4.1.

**Figure 6.26** Abrupt (a) and hyperabrupt (b) tuning varactor doping profiles.

![Graphs showing abrupt (a) and hyperabrupt (b) doping profiles.](image)

Table 6.5 shows breakdown voltages, rest capacitances, and capacitance ratios for the devices fabricated. These are the standard assessment parameters for varactor diodes. The capacitance ratios are given as the ratio of the capacitance at zero bias to the capacitance at a certain reverse bias voltage (-2V in the case of $C_{j0}/C_{j-2}$). As a reminder to the reader, the deep phosphorus implanted samples are those labelled V2.
6.3.3 Capacitance ratios

Table 6.5 Varactor diode properties

<table>
<thead>
<tr>
<th>Material</th>
<th>Device Resistance (Ω)</th>
<th>Reverse Breakdown (V)</th>
<th>Forward breakdown (V)</th>
<th>Zero Bias Capacitance (pF)</th>
<th>( C_{jo}/C_j )</th>
<th>( C_{jo}/C_{j-4} )</th>
<th>( C_{jo}/C_{j-20} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>V1 700°C 15s</td>
<td>30</td>
<td>22</td>
<td>5</td>
<td>1</td>
<td>1.1</td>
<td>1.27</td>
<td>2.14</td>
</tr>
<tr>
<td>V1 800°C 15s</td>
<td>1</td>
<td>26</td>
<td>1.4</td>
<td>1.1</td>
<td>1.1</td>
<td>1.3</td>
<td>2.3</td>
</tr>
<tr>
<td>V1 900°C 15s</td>
<td>2</td>
<td>23</td>
<td>0.9</td>
<td>1.05</td>
<td>1.12</td>
<td>1.27</td>
<td>2.3</td>
</tr>
<tr>
<td>V1 1000°C 15s</td>
<td>2</td>
<td>19</td>
<td>0.9</td>
<td>0.67</td>
<td>1.03</td>
<td>1.1</td>
<td>N/A</td>
</tr>
<tr>
<td>V1 700°C 15 min</td>
<td>2.2</td>
<td>25</td>
<td>0.9</td>
<td>1.1</td>
<td>1.1</td>
<td>1.24</td>
<td>2.2</td>
</tr>
<tr>
<td>V2 700°C 15s</td>
<td>2</td>
<td>32</td>
<td>1</td>
<td>1.25</td>
<td>1.37</td>
<td>1.68</td>
<td>2.96</td>
</tr>
<tr>
<td>V2 800°C 15s</td>
<td>2</td>
<td>35</td>
<td>1</td>
<td>1.27</td>
<td>1.39</td>
<td>1.72</td>
<td>3.1</td>
</tr>
<tr>
<td>V2 900°C 15s</td>
<td>1.25</td>
<td>41</td>
<td>1.1</td>
<td>1.1</td>
<td>1.32</td>
<td>1.57</td>
<td>2.65</td>
</tr>
<tr>
<td>V2 1000°C 15s</td>
<td>1.3</td>
<td>41</td>
<td>1.1</td>
<td>1.1</td>
<td>1.32</td>
<td>1.57</td>
<td>2.65</td>
</tr>
<tr>
<td>V2 700°C 15 min</td>
<td>1.5</td>
<td>36</td>
<td>1</td>
<td>1.0</td>
<td>1.35</td>
<td>1.61</td>
<td>2.73</td>
</tr>
</tbody>
</table>

Sample V1 annealed at 700°C for 10 seconds exhibits an unusually high forward breakdown voltage, and is thought to be a Schottky barrier at the contact metallisation-semiconductor interface, with the p-n junction below. i.e. the forward biased device has a
reverse biased Schottky barrier at the surface. This argument is reinforced by the ‘normal’ reverse breakdown voltage of the device, apparently receiving little contribution from the forward biased junction at the metal-semiconductor interface.

Reverse breakdown voltage increases with anneal temperature for the deep phosphorus implanted samples (V2). This is thought to be due to enhanced diffusion at elevated temperatures towards the diffusion block, caused by the presence of phosphorus at the zinc tail. The result is a sharper interface.

Junction capacitance at zero bias for V1 (the shallow phosphorus implanted samples) reduces with increasing annealing temperature, indicating wider depletion widths at the interface, caused by enhanced diffusion tails at higher temperatures.

In contrast are the V2 samples, which do not appear to present any particular trend. Capacitance measurements are of course dependent on etch uniformity from one sample to the next, although capacitance ratios, discussed next, are not.

Capacitance ratios between 0 and -2V, 0 and -4V and 0 and -20V are given in the table. The values indicated for V1 show that the device improves with increasing anneal temperature, up to around 900°C, when the junction abruptness fails due to enhanced diffusion. Perhaps, in fact, 800°C is nearer to the optimal anneal temperature, due to the higher reverse breakdown voltage at that point.

The V2 samples all give a similar $C_{j0}/C_{j-2}$ value. This is interpreted as meaning that the interfacial quality/properties of all these devices are very similar, since -2V bias is only likely to deplete the part of the implanted region nearest to the interface. Similarities between ratios at elevated anneal temperatures are indicative of a sharp interface, due to
the steep doping profile gradient causing only the 'n'-type epilayer to deplete further at higher reverse bias.

In this chapter the viability of ion implantation for the manufacture of various types of microwave diode has been investigated. It has been shown that the traditional wet chemical etching techniques may be replaced with implant isolation with no detriment to device performance, and improvements in across wafer uniformity. It has also been shown that the introduction of dopants by ion implantation for the fabrication of bulk unipolar diodes and varactor diodes is a realistic alternative to epitaxy, and that even buried layers and planar doping may be achieved, with all the additional advantages of ion implantation.
7. Conclusions and further work

We have demonstrated that the manufacture of high performance microwave devices fabricated from semiconductor multilayers can benefit from ion implantation.

7.1 Planar doped barrier diode

The PDB diode has been shown to be compatible with the implant isolation process. The improvements achieved over wet chemical etching are as follows

a) Greater uniformity of the electrically active area of the device
b) Implantation is self-aligned, using the contact metallisation as a mask.
c) Eradication of one photolithography step, and other process steps.
d) A more robust die for wire bonding purposes.

Further work might include optimisation of ion doses and energies for particular device structures (layer thicknesses).

7.2 Camel diode

Camel diodes have been fabricated in GaAs using ion implantation for the first time. The judicious mix of ion implantation and epitaxy employed demonstrated the feasibility of using ion implantation as a planar doping technique. Potential benefits of this system lie in the superior controllability of ion implantation over epitaxy, when a very thin layer of semiconductor is required with a specific doping-width product. This is likely to result in greater reproducibility of barrier height from diode to diode, and from wafer to wafer.

Further work is necessary before a fully manufacturable device is achievable. It is the belief of the author that the most useful device would be one in which the contact region dopants as well as the p* spike were ion implanted, and the whole device based upon a
shallow contact technology, such as the Ge/Pd system. Work is underway at Surrey to meet this end.

7.3 Graded-gap Gunn diode

The implant isolation process has been demonstrated for the graded-gap Gunn diode. It has been shown that the process results in neither degraded noise performance, nor loss of power. Again, the advantages include improvements in device area uniformity, self-aligned ion implantation, the elimination of a photolithography step, and a more physically robust device. A further advantage is the improved heat sinking of the device, due to the encapsulation of the active area in ion-implanted GaAs.

The IHS Gunn diode has not yet shown such a degree of compatibility with the implant isolation process. Peak microwave power emission occurs at 75 GHz in the implant isolated samples, compared to 77 GHz in the mesa control samples. This is due to the additional parasitic capacitance caused by the implant isolated region.

Further work in this area will consist of seeking an alternative geometry for the IHS Gunn diode in order to eliminate the parasitic effect.

7.4 Varactor diodes

Abrupt, and non-abrupt p-n junction varactor diodes have been fabricated using ion implantation as a method of introducing the p-type dopant, with a phosphorus co-implant for diffusion control, their capacitance-voltage ratios assessed, and compared with their dopant profiles. It has been shown that the junction profile may be tailored by altering the energy of the phosphorus co-implant, from one with a resultant profile overlapping the p-
type dopant implant, to one at the tail of the p-type implant, and that this has a direct
effect on the C-V relationship of the varactor.

Further work: It is anticipated that a hyperabrupt Schottky varactor could be fabricated
using multiple energy implants of the n-type dopant to emulate the epitaxial n-type layer
in current use.

Work is also underway to create a high-power varactor stack in the lateral plane, using
selective-area ion implantation.

The work has opened up the way for the investigation of similar devices fabricated in
different semiconductors, such as indium phosphide, and shown results successful enough
to encourage more research into the application of ion beam processing of different
devices, such as the Schottky varactor. The investigation of new devices fabricated using
ion implantation such as the lateral varactor stack mentioned above is only possible with
selective area ion implantation, and implant isolation offers promise as a possible
technique for the vertical integration of devices, since buried isolation layers may be
achieved.
8. References


Publication List-Stuart Hutchinson


