

Development of a Reference Wafer for On-Wafer Testing of Extreme Impedance Devices

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Abstract — This paper will describe the design, fabrication and testing of an on-wafer substrate that has been developed specifically for measuring extreme impedance devices using an on-wafer probe station. Such devices include Carbon Nano-Tubes (CNTs) and structures based on graphene which possess impedances in the $k\Omega$ range and are generally realised on the nano-scale rather than the micro-scale that is used for conventional on-wafer measurement. These impedances are far removed from the conventional $50\ \Omega$ reference impedance of the test equipment. The on-wafer substrate includes methods for transforming from the micro-scale to the nano-scale and reference standards to enable calibrations for extreme impedance devices. The paper includes typical results obtained from the designed wafer.

Index Terms — Calibration, on-wafer measurement, nano-scale, co-planar waveguide, RF nanotechnology, extreme impedance measurement.

I. INTRODUCTION

New nano-scale device and material technologies are rapidly emerging to support, the Internet-of-Things (IoT), wearable electronics and quantum computing. These new devices derive their advantages from material properties and physical dimensions. Universal high-frequency techniques and standards are required to measure accurately and characterize these devices for their further use in new applications. The intrinsic high impedances ($k\Omega$) [1] of these devices are significantly higher than the $50\ \Omega$ reference impedance of the measurement equipment. This is the main barrier to accurately characterize such devices using the available test equipment, as a highly sensitive system will be required to account for the high reflections generated by these devices [2]. In addition, their dimensions are three orders of magnitude smaller than the available microwave probes. This paper describes a reference wafer that contains access structures and calibration standards that deal with the change in mechanical dimensions to enable reliable on-wafer metrology of nano-scale devices.

Research has been published to date on physically accessing and using conventional systems measuring nano-scale devices, using a co-planar waveguide (CPW) that is tapered down to a few μm [3]-[5]. The reference wafer described in this paper includes similar access structures. The wafer also includes calibration standards that enable the reference planes of the measurements to be moved to the device-under-test (DUT). The standards will enable several calibration techniques to be investigated for high-frequency characterization at this scale.

II. DESIGN

The design of the access structures is based on a ground-signal-ground (GSG) CPW transmission line similar to [3]. Fig. 1 shows the dimensions of an open structure used as one of the calibration standards. The signal conductor has $100\ \mu\text{m}$ width and the separation between the signal and ground conductors is $66\ \mu\text{m}$. The signal and ground conductors are tapered so that the signal conductor width is reduced to $4\ \mu\text{m}$. This provides a position where a nano-scale device can be placed and subsequently measured. The conductor metal used is gold (Au) of $500\ \text{nm}$ thickness on a $400\ \mu\text{m}$ gallium arsenide (GaAs) dielectric substrate. A $20\ \text{nm}$ titanium (Ti) layer was used beneath the Au to enhance adhesion to the substrate. The dimensions of the CPW were chosen to preserve a $50\ \Omega$ characteristic impedance at all places along the CPW line. This minimizes reflections originating from the structures, and thus transfers the maximum amount of the generated RF signal to the DUT.

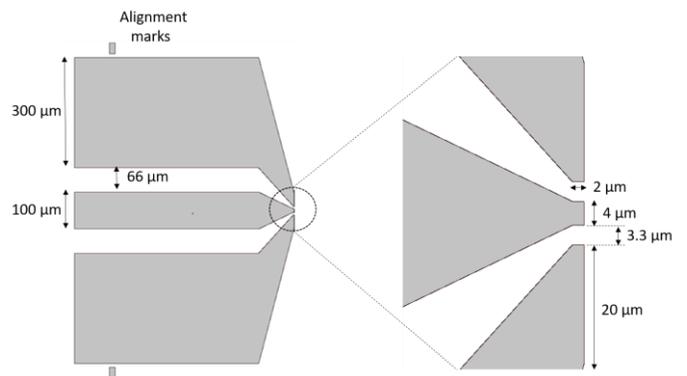


Fig. 1. Open calibration standard. The dimensions of the structure were selected to achieve a characteristic impedance of $50\ \Omega$ across the entire structure.

The calibration standards included on the fabricated wafer are five lines (0.5, 1, 2, 3, 5 mm), six offset shorts designed for 15 GHz, open, short, $50\ \Omega$ load, and thru. In addition, empty one-port and two-port structures with gaps between $2\ \mu\text{m}$ and $20\ \mu\text{m}$ were included to enable nano-scale devices to be placed and measured. Calibration standards were designed to perform a two-tier calibration moving the reference plane of

the measurement from the tips of the microwave probes to the end of the tapered conductor line of the CPW.

III. FABRICATION

The fabrication of the wafer was implemented at the Institute of Electronics, Microelectronics and Nanotechnology (IEMN, RENATECH). The metal layer is constituted of 500 nm thick Au and the resistive layer (Ti) thickness of 24 nm. The process flow is based on conventional optical lithography, metal evaporation and liftoff steps. Scanning electron microscope (SEM) based images show a dispersion of the structure dimensions over the full wafer less than ± 300 nm. The dispersion of the metallic layers thickness obtained by atomic-force microscopy (AFM) measurements is of ± 10 nm and ± 1.5 nm for Au and Ti layers respectively. Fig. 2 shows the 3 inch wafer designed including eight copies of the designed access structures and calibration standards.

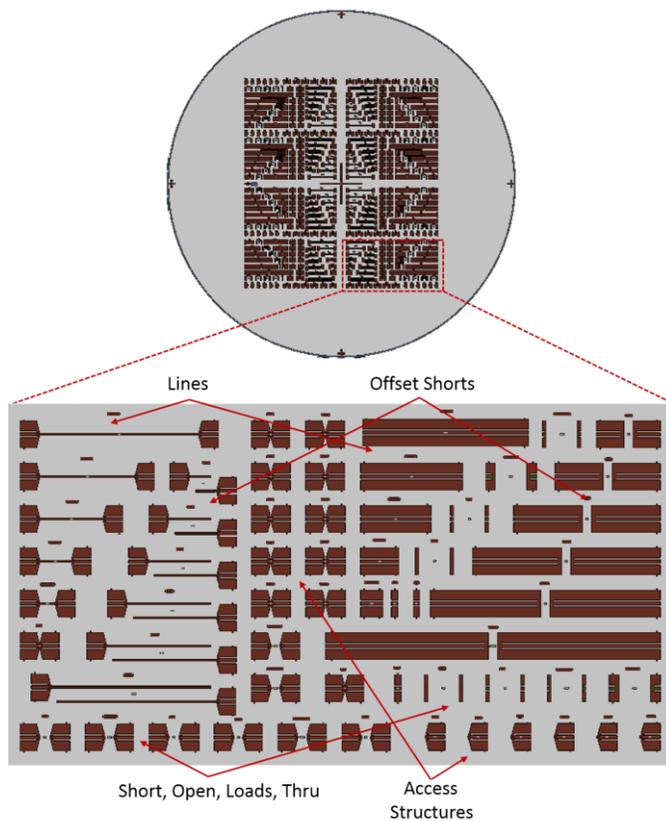


Fig. 2. Layout of the fabricated 3 inch wafer including all the access structures and calibration standards.

IV. MEASUREMENT SET-UP

Initial measurements were conducted on the fabricated structures to verify, by comparing with electromagnetic simulations, that they have been designed and fabricated correctly. For the S-parameter measurements, a Keysight

N5247A PNA-X Vector Network Analyzer was used. The on-wafer probes used were MPI Titan 26 GHz GSG probes with 150 μm pitch.

The system was fully calibrated up to the probe tips by SOLT calibration method using an MPI AC-2 impedance standard substrate [6]. The measurement configuration on a MPI TS-2000 probe station is shown in Fig. 3. QAlibria software [7] was used to calibrate the VNA and to obtain the corrected results. The frequency range of the measurement was set to 0.1 – 20 GHz with 100 Hz IF bandwidth.

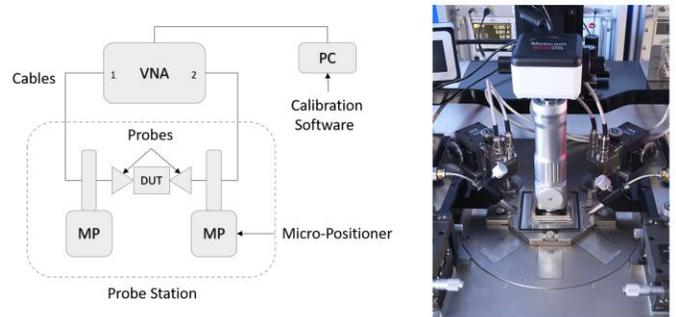


Fig. 3. (Left) Simplified block diagram of the two-port test set-up, (Right) Photograph of the measurement set-up at n3m-labs¹.

V. RESULTS

The reflection and transmission coefficients obtained for the measurements of a thru calibration standard are shown in Fig. 4 and Fig. 5 respectively. Measurements were performed on two different thru structures, represented by the blue and red lines, and were compared with the electromagnetic simulation (black line). The simulation and design of the structures was implemented using Sonnet Software [8].

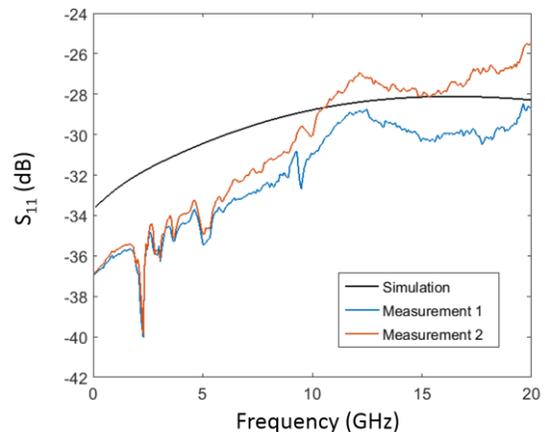


Fig. 4. Simulated and measured reflection coefficient of the thru calibration standard.

¹ n3m-labs is the joint NPL/University of Surrey ‘Nonlinear Microwave Measurement and Modeling Laboratories’.

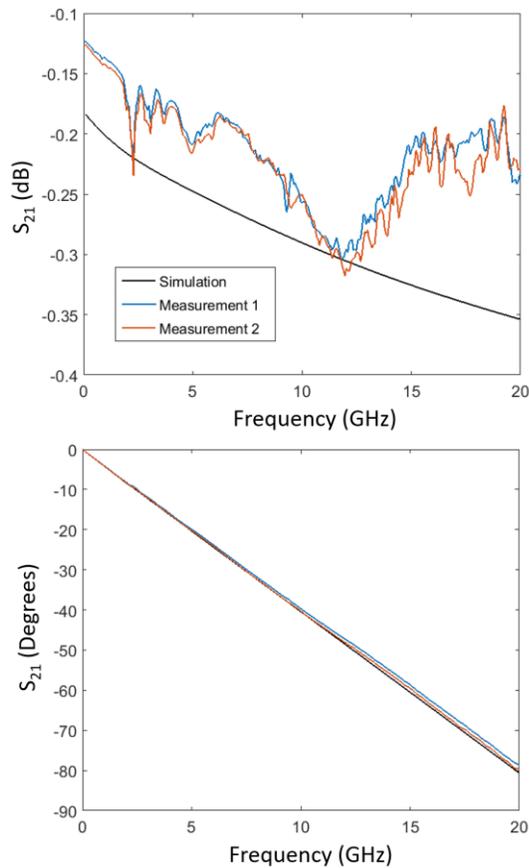


Fig. 5. Simulated and measured transmission coefficient of the thru calibration standard.

The results show that the designed structures have approximately 50Ω characteristic impedance with a reflection coefficient of better than -25 dB at all frequencies. Moreover, there is good agreement between the simulated and measured data. A plot of the reflection coefficient's phase is not included because phase becomes indeterminate when the magnitude of a signal is relatively small (i.e. compared to the system noise floor). However, further measurements are required and several factors must be considered, to perform an accurate evaluation of the structures. These measurements will be presented in the final, submitted, version of this paper.

VI. CONCLUSIONS

The design and fabrication of a reference wafer containing access structures and calibration standards enabling the measurement of nano-scale devices at microwave frequencies has been presented. The structures presented are based on a CPW design, moving the reference plane of the measurement from the conventional micro-scale to the sub-micro scale.

These structures and standards will be utilized in a new method which transforms the 50Ω impedance of the test equipment in the $k\Omega$ range for the accurate characterization of nano-scale devices. In addition, the validity of different

calibration techniques for nano-scale microwave measurements will be investigated using the calibration standards included on the wafer.

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