A GPU Implementation of a MAP Decoder for Synchronization Error Correcting Codes

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Abstract—In this paper we present a parallel implementation of a MAP decoder for synchronization error correcting codes. For a modest implementation effort, we demonstrate a considerable decoding speedup, up to two orders of magnitude even on consumer GPUs. This enables the analysis of much larger codes and worse channel conditions than previously possible, and makes applications of such codes feasible for software implementations.

Index Terms—Insertion-Deletion Correction, MAP Decoder, Forward-Backward Algorithm, CUDA, GPU

I. INTRODUCTION

While most coding schemes focus on the correction of substitution errors, the problem of correcting synchronization errors has seen a recent increase in interest [1]. A key development has been the concatenated scheme by Davey and MacKay [2], where a random binary marker sequence is used by the decoder to determine synchronization. A sparse representation of the message is then added to this marker sequence. We presented a maximum a-posteriori (MAP) decoder representation of the message is then added to this marker sequence. While most coding schemes focus on the correction of substitution errors, the problem of correcting synchronization errors has seen a recent increase in interest [1]. A key development has been the concatenated scheme by Davey and MacKay [2], where a random binary marker sequence is used by the decoder to determine synchronization. A sparse representation of the message is then added to this marker sequence. We presented a maximum a-posteriori (MAP) decoder representation of the message is then added to this marker sequence. Initial attempts at speeding up the decoding either result in sub-optimal decoding [2] or are based on a speed/memory trade-off [5]. In both cases the effect on decoding performance either was not analyzed in detail, or is only known for particular conditions. An alternative approach is to look at a parallelization of the MAP algorithm on a graphics processing unit (GPU) using CUDA [6].

Other MAP decoders have been implemented on GPUs; the closest to our work are for convolutional codes (as used in turbo codes) [7], [8] or for general hidden Markov models [9]. However, there are fundamental differences in our application which require a different approach. First, the state-space in turbo codes is fixed and generally very small (e.g. [8] uses an 8-state trellis). In our case, the state space can easily run into hundreds of states for poor channel conditions. Second, the cited work is for binary codes; our application requires a non-binary decoder, adding another complexity dimension. Finally, the branch metric for convolutional codes is trivial to compute, so is generally recomputed as needed. In our case this requires a separate forward pass, and dominates complexity.

This paper starts with general notation and a system description in Section II, followed by a definition of the MAP decoder and its complexity in Section III. In Section IV we consider the problem of parallelizing the decoder and analyze the scalability and expected speedup of this solution in Section V. Practical results follow in Section VI for two GPU systems, with conclusions drawn in Section VII.

II. PRELIMINARIES

We use the channel model of [2]. At time $t$, one bit enters the channel, and one of three events may happen: insertion with probability $P_I$ where a random bit is output; deletion with probability $P_D$ where the input is discarded; or transmission with probability $P_T = 1 - P_I - P_D$. A substitution occurs in a transmitted bit with probability $P_S$. In the case of insertion the channel remains at time $t$ and is subject to the same events again, otherwise we proceed to time $t + 1$, ready for another input bit. We define the drift $S_t$ at time $t$ as the difference between the number of transmitted bits and the number of received bits before the events of time $t$ are considered.

For any sequence $z$ we denote arbitrary subsequences as $z^{(i)}=(z_a,\ldots,z_{b-1})$, where $z^{(i)}=()$ is an empty sequence. The juxtaposition of $y$ and $z$ is denoted by $y||z$. For $n,q,N \in \mathbb{N}$ we assume a message sequence $D^{(0)} = (D_0,\ldots,D_{N-1})$, where each symbol $D_i \in \mathbb{F}_q$ is mapped to a codeword of length $n \geq 2^t$ by an encoding $C_i : \mathbb{F}_q \leftrightarrow \mathbb{F}_2^t$ for $i = 0,\ldots,N - 1$. Therefore the message $D^{(n)}$ is encoded as $X^{(n)}_k = C_0(D_0)||\ldots||C_{n-1}(D_{N-1})$, where $r = nN$. Note that a different mapping may be used for each symbol index; in the Davey-MacKay scheme this is obtained as the addition of the sparse representation of $D_i$ and the section of the random marker sequence corresponding to the symbol at index $i$. This is transmitted over the channel, resulting in the received sequence $Y^{(n)}_k$, where in general $\rho \neq \tau$.

III. THE MAP DECODER

The MAP decoder of [3] calculates the $a$ posteriori probability $L_i(D)$ of having encoded symbol $D \in \mathbb{F}_q$ in position $i$ for $0 \leq i < N$, given the entire received sequence, using:

$$L_i(D) = \frac{1}{\lambda_N(\rho - \tau)} \sum_{m',m} \sigma_i(m',m,D) \quad (1)$$

$$\lambda_i(m) = \alpha_i(m)\beta_i(m) \quad (2)$$

$$\sigma_i(m', m, D) = \alpha_i(m')\gamma_i(m', m, D)\beta_{i+1}(m) \quad (3)$$

$$\alpha_i(m) = \sum_{m',D} \alpha_{i-1}(m')\gamma_{i-1}(m', m, D) \quad (4)$$

Manuscript received October 31, 2012; revised January 25, 2013. Parts of this research have been carried out using computational facilities procured through the European Regional Development Fund, Project ERDF-080. J. A. Briffa is with the Dept. of Computing, University of Surrey, Guildford GU2 7XH, England. Email: j.briffa@surrey.ac.uk
\[ \beta_i(m) = \sum_{m',d} \beta_{i+1}(m') \gamma_i(m,m',D) \]  
\[ \gamma_i(m',m,D) = \Pr \{ D_i = D \} R(\mathbf{y}_{m(i+1)+m} | C_i(D)) \]

where the prior probabilities are denoted by \( \Pr \{ D_i = D \} \).

The state transition metric is calculated using

\[ R(\mathbf{y}|x) = \alpha_n(\mu - n), \]
\[ \alpha_t(m) = \sum_{m'} \alpha_{t-1}(m') \cdot Q(\mathbf{y}_{t+m}^{|t-m'|}|x_{t-1}), \]

\( \mu \) is the length of \( \mathbf{y} \), \( n \) is the length of \( x \), and \( Q(y|x) \) can be directly computed from \( y, x \) and the channel parameters:

\[ Q(y|x) = \begin{cases} 
P_d & \text{if } \mu = 0 \\
\left( \frac{P_f}{P_d} \right)^{\mu-1} \left( P_f P_s + \frac{1}{2} P_t P_d \right) & \text{if } \mu > 0, y_{\mu-1} \neq x \\
\left( \frac{P_f}{P_d} \right)^{\mu-1} \left( P_f P_s + \frac{1}{2} P_t P_d \right) & \text{if } \mu > 0, y_{\mu-1} = x,
\end{cases} \]

where \( \mu \) is the length of \( y \) and \( P_d = 1 - P_s \).

Since the set of all possible states is unbounded for the channel considered, a practical implementation has to take sums over a finite subset, chosen so that only the least likely states are omitted. We denote the number of states required for a segment of length \( T \) bits by \( M_T \). Therefore, computations (1), (4), and (5) have a state space of size \( M_T \), while computation (7) has a state space of size \( M_n \).

Similarly, the number of drift changes considered over a single bit depends on the number of consecutive insertions, and is denoted by \( I_T \) for a segment of length \( T \) bits. This limits the connectivity of consecutive states. The precise determination of the size of the state space is beyond the scope of this paper, and is left for a separate work.

The \( \alpha \) and \( \beta \) computations as given in (4) and (5) have a very wide numerical range. However, the decoder needs only the relative values of \( L_i(D) \) for different \( D \), so we can safely normalize the \( \alpha \) and \( \beta \) metrics as they are computed. For example, for \( \alpha \) the computation (4) is changed to:

\[ \alpha_i(m) = \frac{\alpha'_i(m)}{\sum_{m'} \alpha'_i(m')} \]
\[ \alpha'_i(m) = \sum_{m',D} \alpha_{i-1}(m') \gamma_{i-1}(m',m,D) \]

A similar argument applies for the computation of \( \beta \) and \( \alpha \).

For typical codeword sizes and channel conditions it is sufficient to compute (7) at single precision (float). The use of double precision (double) is indicated for the remaining equations, particularly for large \( N \) and poor channel conditions. This has been verified by simulation, comparing the decoding error rate with a reference multi-precision implementation [10]. Therefore float performance has a dominant effect on computing the \( \gamma \) metric, while double performance is dominant for the remaining metrics.

The asymptotic complexity of the decoder is given by \( O(NnqM_T M_n^2 I_n) \), where \( N, n, q \) depend only on the code parameters while \( M_T, M_n, I_n \) also depend on the channel conditions [3]. It was argued in [2] that capping the number of consecutive insertions to two causes minimal loss of decoding performance; the same cap was also used in [3], [11]. However, more advanced constructions require a higher cap or lifting the restriction [4].

### IV. Parallel Implementation

The MAP decoder consists of four functions, one for computing each of the \( \gamma, \alpha, \beta, \) and \( L \) matrices. These depend on each other, dictating the order of computation. We follow the usual CUDA notation, where a block is the collection of threads executing on the same multiprocessor, and a grid is the set of equally-shaped blocks in a kernel call.

Starting with the \( \gamma \) computation (6), which needs to be performed first, it can be seen that computation is independent for each of \( i, D, m, m' \). This facilitates a data-parallel implementation across any of these variables. For the expected ranges of \( i \) and \( D \) it is natural to consider using a grid size \( N \) and block size \( q \). We store the four-dimensional \( \gamma \) matrix as a flat array in global memory, with indices \( m' \) and \( m - m' \) innermost. This allows each thread to access a contiguous range of memory sequentially, while separate threads access regions that are far away from each other. This maximizes cache re-use as long as the number of concurrent threads is not greater than the number of cache lines.

The \( \alpha \) and \( \beta \) computations pose greater difficulty due to their recursive nature and the need to normalize. Considering the pre-normalization computation (9), there is a clear data dependency across the range of \( i \); however, for any given \( i \) the computation is independent for different values of \( m \). The expected range of \( m \) depends on \( N, n, q \) and channel error rate, and can be as high as several hundred. This makes \( m \) a natural candidate for parallelization across blocks, for a grid size of \( M_T \). Further, the summation over \( D \) can be separated across threads, with the partial summation over \( m' \) computed independently for each \( D \), and the final result computed from these partial sums. This gives a block size of \( q \).

Due to data dependency, for a given \( i \) all \( \alpha'_i(m) \) must be computed before \( \alpha_i(m) \) can be determined. The only way to synchronize across a grid is the completion of a kernel call [6], so a separate call is required for each \( i \) to compute (9). After each call, a separate kernel is required to perform normalization (8). This requires two steps: computing the sum of all \( \alpha'_i \), and dividing each \( \alpha'_i \) by this sum. Both can be parallelized across a single block of \( M_T \) threads.

A similar argument applies to the computation of \( \beta \). Further, \( \alpha \) and \( \beta \) can be computed concurrently as there is no data dependency. On devices supporting concurrent kernel execution, this can be achieved using streams, but is complicated by Fermi hardware limitations. A new kernel is only dispatched if preceding kernels in the same stream have completed. Since Fermi has only one compute engine queue, if any stream has more than one kernel scheduled consecutively, the issuer will stall until the last kernel in the sequence is dispatched. The kernels for \( \alpha \) and \( \beta \) at each index have the same complexity, so a successful strategy is as follows: schedule the computation of \( \alpha_{i=0} \) in stream one and of \( \beta_{i=0} \) in stream two, followed by the normalization of \( \alpha_{i=N} \) in stream one and of \( \beta_{i=N} \) in stream two. This is repeated, incrementing \( i \) for \( \alpha \) and decrementing for \( \beta \). Concurrent execution improves device utilization when the grid size for a single kernel call is small.

Finally, the \( L \) computation (1) is independent across \( i, D \). Similarly to the computation of \( \gamma \), we parallelize this with a
grid size \( N \) and block size \( q \).

V. Analysis

A summary of the kernels used is given in Table I, where it can be seen that the block size is equal to \( q \) or \( M_\tau \). Now the device architecture imposes a hardware limit on the maximum block size \([6]\), limiting the alphabet sizes and state space supported by our implementation. Current code constructions fall well within these limitations, as we will see in Section VI.

We also list in the table the complexity of computations for a single thread, assuming \( M_n \gg I_n \).

The effectiveness of the parallelization depends on the utilization at various levels. At device level, utilization for a single kernel depends on the grid size: ideally this is a multiple of \( N_{SM} \), the number of streaming multiprocessors (SM). At a SM level, determining the utilization is rather more complicated. Threads in a block are grouped into warps, and instructions are issued at warp level; ideally the block size should be a multiple of the warp size \( W \). However, maximizing throughput also depends on having enough resident warps, which is limited by the compute capability and by the number of registers required per thread. The number of arithmetic operations that can be executed in parallel depends on the number of cores per SM, \( N_C \), and on the precision. Furthermore, global memory access has a high latency, so minimizing data transfers between global memory and the SM is important. It is also important to organize any global memory access into optimal patterns to make use of memory access coalescing.

For the problem considered, the parallelization efficiency depends on the device specifications and the code parameters; for some kernels it also depends on the channel conditions. Consider first the \( \gamma \) computation, which has the highest overall computational cost. Device usage is optimal when \( N \) is a multiple of \( N_{SM} \), and close to optimal for \( N \gg N_{SM} \). Under these conditions, we get an ideal speedup equal to \( N_{SM} \). When \( N < N_{SM} \), the gain is equal to \( N \). For \( \text{float} \), the arithmetic throughput is equal to \( N_C \) operations per clock cycle per SM. Ideally, therefore, the block size \( q \) is a multiple of both \( N_C \) and \( W \). Under these conditions, and if latency is completely hidden, we could expect a speedup equal to \( N_C \). For \( q < N_C \), we could expect at best a speedup equal to \( q \), and only under ideal conditions. A similar argument can be applied for the computation of \( L \), except for the use of \text{double} and a lower potential throughput. Arguments for the computation of \( \alpha \) and \( \beta \) are further complicated by the kernel call overhead.

VI. Results

We determine GPU performance on two Fermi consumer devices. CPU timings are given for a serial implementation, used as a reference for validation of results and speedup comparisons. Hardware specifications are summarized in Table II. The choice of codebook has no impact on the decoding speed, so we always use the construction of [2]. However, we do not cap the number of consecutive insertions and do not perform any path truncation. This considers decoder complexity under worst-case conditions, as needed for more advanced constructions. The SM cache has been kept at the default configuration, where on-chip memory is allocated as 48 KiB of shared memory and 16 KiB of L1 cache. This is equivalent to 128 lines of cache for each SM.

We consider first the time to compute the \( \gamma \) metric over a range of \( N \), for fixed \( q \) and channel conditions \( p := P_1 = P_0 \). To analyze the effect on parallelization efficiency, we plot the computation time normalized by the expected complexity in Figure 1a. Note that the normalized GPU time is not constant as one would expect. This indicates that the expected complexity is missing some details. This is not surprising, as the complexity expressions consider only the floating-point arithmetic, ignoring the computational overhead of loop handling or memory access. For the GPU timings, note that maximum efficiency is achieved at \( N = 8 \) for the GT 520 and close to \( N = 100 \) for the GTX 480. This means that as the grid size increases beyond the number of SMs on the device, performance continues to improve as the additional blocks allow the device to hide latency more efficiently, until we reach...
eight blocks per SM, the maximum number of resident blocks.

The GPU to CPU speedup under the same conditions is shown in Figure 1b, together with the peak speedup for a compute-bound problem on each device. On the GTX 480 for \( N \geq 100 \) the speedup tops out at more than 100× for \( p = 10^{-4} \); this compares favourably with the theoretical peak of 278.8×. At a higher \( p = 10^{-5} \) the speedup decreases to around 70×, indicating a loss of efficiency for larger state spaces. This is most likely due to the increased access to global memory. The GT 520 peak performance is achieved at \( 70 \times \), indicating a loss of efficiency for larger state spaces. This can be overcome by splitting the alphabet over different blocks. Our implementation assumes that there is sufficient memory to pre-compute the \( \gamma \) metric; this can be overcome by computing \( \gamma \) incrementally as needed by the computations for \( \alpha, \beta, \) and \( L \). This impacts performance as each \( \gamma \) metric needs to be computed more than once. All this is the subject of further work.

**ACKNOWLEDGMENT**

The author would like to thank Prof. Ing. V. Buttigieg and Dr S. Wesemeyer for helpful discussions and comments.

**REFERENCES**


