A Nonlinear Electro-Thermal Model for High Power RF LDMOS Transistors

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***Abstract*— A new nonlinear, charge-conservative, dynamic electro-thermal compact model for LDMOS RF power transistors is described in this paper. The transistor is characterized using pulsed I-V and S-parameter measurements, to ensure isothermal conditions. The intrinsic model current and charge sources are obtained by integration of the real and imaginary components, respectively, of the small-signal Y-parameters: this yields a charge-conservative model by design. A thermal sub-circuit is used to introduce dynamic thermal dependence, and thermal threshold voltage shift is built in. DC and large-signal validation of the model is presented.**

I. Introduction

Power amplifiers for wireless communications systems are tightly specified in terms of their linearity performance, bandwidth, etc., while at the same time customers are requiring higher powers, greater efficiencies, as well as easily-linearizable performance. These system specifications and performance compromises, and the increasing adoption of complex signal modulations make it very difficult to design an optimized power amplifier in a timely manner without the use of CAD techniques. This places a premium on the availability of accurate nonlinear transistor models.

The combination of high powers and high frequencies in RF and microwave power amplifiers brings together a unique set of challenges for the device modeling engineer. The power transistors themselves are physically large, and may occupy a significant fraction of a wavelength, even at microwave frequencies. The electrical behavior in this distributed environment must be captured in the model. The device will generate a lot of heat, and the thermal effects on the transistor's electrical behavior will also need to be characterized and modeled accurately.

Laterally-diffused MOS (LDMOS) FETs are used almost exclusively for high power transistors for wireless infrastructure or base-station applications. They provide an unmatchable combination of performance and cost, and are capable of delivering hundreds of watts of RF power.

In this paper we shall outline a new nonlinear intrinsic model for the LDMOS transistor, and its extraction and implementation. The model architecture, shown in Fig. 1, is, by design, technology-independent. The technology-specific components will be defined in the manifolds and extrinsic parts of the model, which capture the electrical behavior of the layout and physical structure of the transistor. The intrinsic part of the model, shown in the center of Fig. 1, describes the nonlinear behavior of the transistor, using voltage-controlled current and charge sources: the model state functions. This

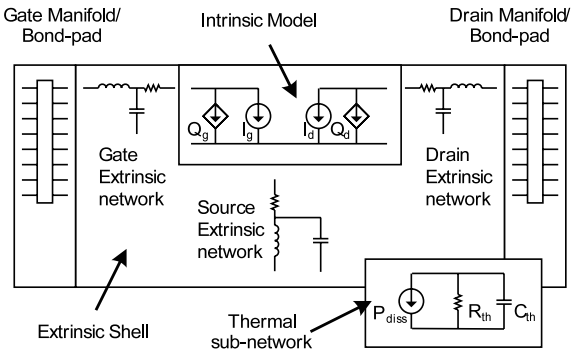

Fig. 1. Block representation of the transistor model architecture.

basic structure is no different in principle to those nonlinear models presented by [1]–[3]. The model is implemented in such a manner as to enable the choice of a variety of model functions and approximation techniques for the state functions, from look-up tables to analytic models using elementary functions, and neural network function approximations [3].

A charge-conservative approach is adopted, as this is crucial to the accurate prediction of the low-level nonlinearities such as those described by intermodulation products, adjacent channel power, and so forth [4]. Included in this model are accurate, continuously-differentiable functions for the model currents and charges, and a self-consistent electro-thermal model coupled to these sources. An accurate, broadband extrinsic network model and extraction procedure are described in detail elsewhere [5].

II. Transistor Characterization and Extraction

The transistor characterization is carried out on-wafer. The test transistor is GSG-probe-able. This transistor has the same basic structure as the production device, but is much smaller - fewer gate fingers - than the production device, and is stable in a 50 Ω environment. A two-tier RF calibration to the probe tips is carried out using TRL technique and an impedance standard substrate. The current-voltage and S-parameter measurements are made at constant, controlled substrate temperature using pulse techniques, to capture data isothermally, and to measure beyond the DC dissipation limit of the device, into realistic instantaneous voltage and current regimes.

A dense pattern of pulsed I-V and S-parameter measurements are taken over the gate-drain voltage space of the transistor, bounded by the maximum drain current, breakdown voltage, and the maximum allowable power dissipation. The

manifold structure and the extrinsic network are de-embedded to obtain S-parameter data at the intrinsic model reference planes [5]. After converting to Y-parameters, the LDMOS transistor model current and charge state functions can then be obtained by integration of the small-signal voltage-dependent parameters, using the following equations found in [3].

$$I_{\rm d}\left(V_{\rm gs},V_{\rm ds}\right)=\int_{V_{\rm gs0}}^{V_{\rm gs}} g_{\rm m}\left(v_{\rm gs},V_{\rm ds0}\right)dv_{\rm gs}+\int_{V_{\rm ds0}}^{V_{\rm ds}} g_{\rm ds}\left(V_{\rm gs},v_{\rm ds}\right)dv_{\rm ds} + I_{\rm d}\left(V_{\rm gs0},V_{\rm ds0}\right) \tag{1}$$

$$Q_{\rm g}\left(V_{\rm gs},V_{\rm ds}\right)=\int_{V_{\rm gs0}}^{V_{\rm gs}}\left[C_{\rm gs}\left(v_{\rm gs},V_{\rm ds0}\right)+C_{\rm gd}\left(v_{\rm gs},V_{\rm ds0}\right)\right]dv_{\rm gs} - \int_{V_{\rm ds0}}^{V_{\rm ds}} C_{\rm gd}\left(V_{\rm gs},v_{\rm ds}\right)dv_{\rm ds}+Q_{\rm g}\left(V_{\rm gs0},V_{\rm ds0}\right) \tag{2}$$

$$Q_{\rm d}\left(V_{\rm gs},V_{\rm ds}\right)=\int_{V_{\rm gs0}}^{V_{\rm gs}}\left[C_{\rm m}\left(v_{\rm gs},V_{\rm ds0}\right)-C_{\rm gd}\left(v_{\rm gs},V_{\rm ds0}\right)\right]dv_{\rm gs} + \int_{V_{\rm ds0}}^{V_{\rm ds}}\left[C_{\rm ds}\left(V_{\rm gs},v_{\rm ds}\right)+C_{\rm gd}\left(V_{\rm gs},v_{\rm ds}\right)\right]dv_{\rm ds} + Q_{\rm d}\left(V_{\rm gs0},V_{\rm ds0}\right) \tag{3}$$

The gate current source in the MOS device is set to zero. This integral formulation for determining the charges ensures a conservative charge formulation, essential for accurate prediction of low-level phase nonlinearity, and for convergence in time-domain simulations [3], [6].

III. Drain Current Model

The drain current given by (1) is a 'high frequency' drain current, and using this for the model at RF overcomes some of the dispersion issues present in some FET technologies. Even though LDMOS does not suffer from significant trap-induced dispersion, we use the high frequency drain current to derive the model.

In this nonlinear model, we use the analytical expression (4) due to Fager *et al.* [7] to fit the high frequency drain current data, as this expression has been shown to give improved fit to the current data in the near-threshold region. This is typically where the LDMOS power transistor is biased for power amplifier applications. The improved fit in this region enables a more accurate prediction of distortion products.

$$I_{\rm d}=\beta\frac{V_{\rm gst}^2}{1+V_{\rm gst}^p/VL}\tanh\left(\frac{\alpha V_{\rm ds}}{V_{\rm gst}^{psat}}\right)\left(1+\lambda V_{\rm ds}\right) \tag{4}$$

In addition to the expression above, which is used to fit the data in the active on-state and threshold regions, we add functions to mimic the drain current behavior in the on- and off-state breakdown regions of the FET. These breakdown currents are modeled using diode-like expressions, as used in the Motorola Electro-Thermal (MET) model [8]. It is essential to include these effects in the model for large-signal applications.

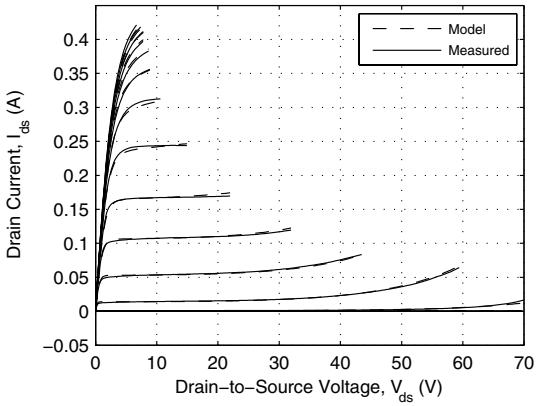

Fig. 2. Drain current characteristic of the new model compared to the intrinsic measured data.

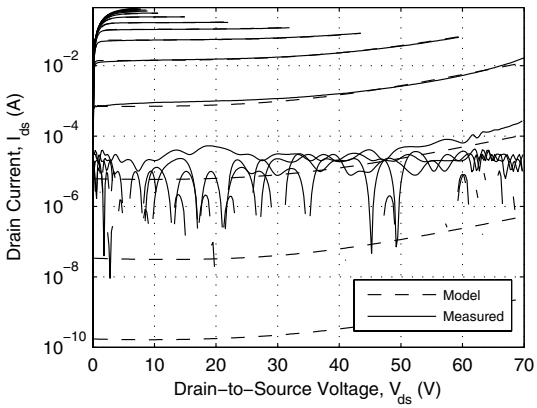

Fig. 3. Drain current characteristic of the new model in the near-threshold region of operation, compared with the intrinsic measured data, which can be seen to be strongly affected by measurement noise.

The accuracy of the fit of the drain current model is shown in Fig. 2. The measured data is seen to probe the breakdown region, and the model replicates this exactly. The behavior of the model in the threshold and sub-threshold region is shown in Fig. 3. It is clear that the measured data is noisy in this region, whereas the model current is smooth, with continuous and smooth derivatives. Unlike table- or data-based models, this analytical drain current model is able to predict distortion products accurately in this bias region.

IV. Charge Model

One of the main objectives of this new nonlinear model development was to improve the charge model description over that of the existing MET model. In particular, a charge-conservative model formulation, approximated by a smooth and differentiable function, and capable of including temperature dependence, was seen as an essential goal.

In this implementation, the conservative gate and drain charges, Q_g and Q_d of (2) and (3) were obtained through a Root model extraction from the measured intrinsic data, using the commercial Agilent-EEsof IC-CAP™ function. In our model extraction, this produces tables of the charge data indexed by the intrinsic gate and drain voltages. These data are then approximated using artificial neural networks (ANNs), resulting in smooth and infinitely differentiable two-dimensional charge functions that are used directly in the model in Fig. 1. It is also possible to obtain the neural network charge functions by fitting an adjoint neural net to the small-signal capacitances, avoiding the direct integration step in (2) and (3) [9].

Although the temperature dependence of the charges is weak, it can be included by carrying out the neural network function approximation of the charges over several temperatures. In the transistor model, the average temperature of the device is found from a self-consistent electro-thermal model, described below.

V. Electro-Thermal Model

Power transistors dissipate a lot of heat, and so it is necessary to include temperature dependence into the model parameters. Further, the information signals used in modern wireless communications have large peak-to-average ratios of the signal voltage or power: therefore, the dynamical response of the transistor's thermal behavior to these inputs must also be captured in the model. An accurate dynamical electro-thermal model is required. A simple way of including the thermal effects on the output current is to use a de-rating function on the drain current expression [3], [10]. This is effectively a wrapper around the drain current model, and can be expressed in the following way:

$$I_{\rm d} = \frac{I_{\rm d0}}{1+\dfrac{(T-T_0)}{T_0}} = \frac{I_{\rm d0}}{1+\dfrac{R_{\rm th}P_{\rm avg}}{T_0}} \tag{5}$$

where T is the temperature, I_{d0} is the drain current measured at a reference temperature T_0, P_{avg} is the average dissipated power. The thermal resistance, $R_{\rm th}$ is found from the difference between the drain current measured under isothermal (pulsed) conditions and DC, at a fixed substrate temperature. This is still a static expression. The instantaneous channel temperature is related to the instantaneous power, which is related to the average dissipated power through

$$\begin{aligned}\text{Heat Generation}(i_{\rm d}, v_{\rm ds}) &= \text{Heat flow}(T-T_0)\\ &\quad + \frac{d}{dt}(\text{Heat Storage})(T-T_0))\end{aligned}$$

which becomes

$$P_{\rm diss}(t) = \frac{(T-T_0)}{R_{\rm th}} + C_{\rm th}\frac{d}{dt}(T-T_0) \tag{6}$$

A new thermal parameter, C_{th} the thermal capacitance, has been introduced in this expression. This parameter accounts for the thermal memory in the transistor. Its value can be estimated using a pulse profiling technique: the decay with time of a pulse of drain current is measured, and this capacitance is found from the characteristic decay time, using the thermal resistance found earlier.

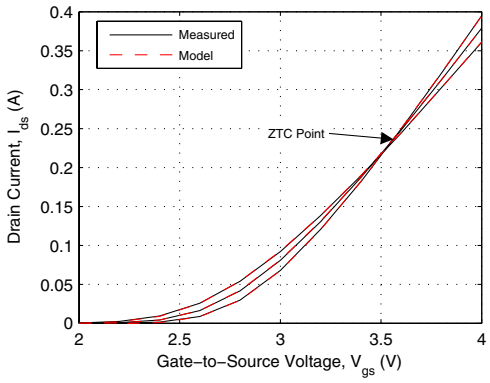

Fig. 4. The modeled and measured drain current of an LDMOS transistor as a function of the applied gate voltage, showing the accurate prediction of the zero-temperature coefficient (ZTC) point. The drain current is plotted at 25, 75, and 125°C.

The threshold voltage thermal variation acts in the opposite sense to the drain current de-rating, producing a point in the drain current-gate voltage relationship that is independent of temperature: the *zero-temperature coefficient* or ZTC point [11]. This threshold voltage variation is accommodated by an additional parameter in the drain current model, as in the MET model [8]. The measured and modeled transistor drain current as a function of the gate voltage is shown in Fig. 4, indicating the ZTC point is modeled accurately.

VI. Model Implementation and Results

The model has been implemented in using the Agilent-EEsof MINT™ modeling interface. A modular approach has been adopted allowing us to choose from and compare a variety of model implementations for the current and charge models: table-based models, MET expressions, neural networks, and the new model descriptions. This new model has been compared against the measured data, and existing MET and Root models extracted from the same data. In the comparisons that follow we have measured and modeled a LDMOS FET at 2.14 GHz under class AB bias conditions. The unit gate with is 600 µmand the transistor is 2.4 mm in total gate periphery.

In Fig. 5, we show that the new model exhibits the correct asymptotic behavior of the intermodulation products at low drive power, and predicts higher order products, unlike the table model which is limited by the spline interpolation. At higher powers, the new model matches the Root model, which is accurate in this regime. This indicates that the new model is behaving correctly.

The correct prediction of large-signal performance by the nonlinear model is also crucial. In Fig. 6 the drive-up characteristics of the model are compared with measurement at two different biases, showing very good agreement, even in compression. The measured and predicted power-added efficiency load-pull contours for various output powers are shown in Fig. 7. This is a stringent test of a model: the large-signal,

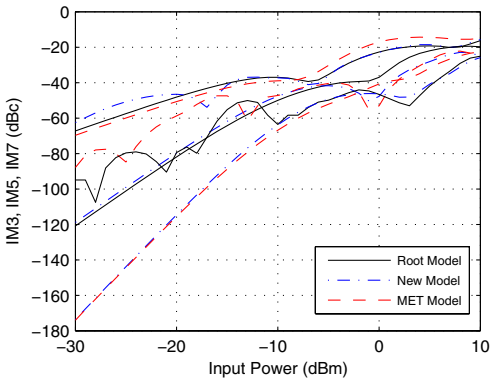

Fig. 5. Simulation results of the intermodulation distortion products for $f_o = 2.14$ GHz with a tone spacing of 100 kHz, as a function of the input power, at the intrinsic reference plane, comparing MET and Root models to the new model.

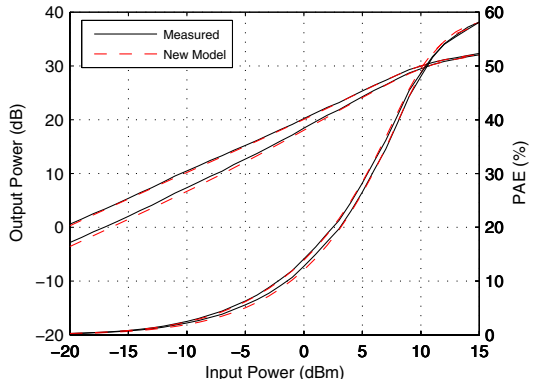

Fig. 6. Measured and modeled output power versus input power for bias currents equal to 6 and 9 mA/mm.

TABLE I

COMPARISON OF THE ROOT AND NEW MODEL (TIME IN SECONDS).

	DC-IV	Envelope	HB 1-tone	LSSP	SP	Trans.
Root	1.97	67.90	6.19	3.73	1.39	24.73
Model	1.36	58.59	6.86	3.38	0.97	19.88

high-frequency nonlinear behavior and the DC conditions must be predicted accurately at the same time, and to do this over a range of load conditions and output powers indicates that the model is accurate, tracking the measured data very closely.

This new model also executes in the simulator with no speed penalty. In benchmarking tests, it is faster than the Root model in almost all simulation conditions, as indicated in Table I.

VII. Conclusion

We have described the architecture, extraction and implementation of a new, nonlinear, charge-conservative, dynamic electro-thermal compact transistor model for RF power LDMOS FETs. The new Freescale Electro-Thermal model is shown to be more accurate than both the industry-standard Motorola Electro-Thermal (MET) model for power FETs, and the Root model, which is another charge-conservative

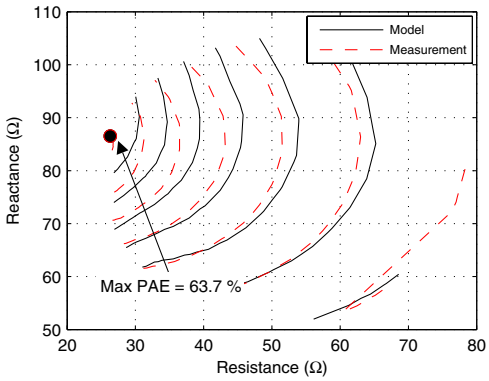

Fig. 7. Load-pull contours of power-added efficiency at P_{1dB}, comparing measured data and the new model.

formulation. The new model is also faster in simulation of typical power amplifier design applications, saving valuable design time.

VIII. Acknowledgments

Thanks are due to the management staff of RF Division, Freescale, in particular Jaime Plá, for encouraging and supporting the development of this new nonlinear model.

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