Low-field behaviour of source-gated transistors

J. M. Shannon, R. A. Sporea*, *Member, IEEE*, S. Georgakopoulos, M. Shkunov, *Member, IEEE,* and S. R. P. Silva

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J. M. Shannon, R. A. Sporea, S. Georgakopoulos, M. Shkunov and S. R. P. Silva are with the Advanced Technology Institute, University of Surrey, Guildford, Surrey, GU2 7XH, United Kingdom (*email: r.a.sporea@surrey.ac.uk).

***Abstract* — A physical description for low-field behavior of a Schottky source-gated transistor (SGT) is outlined where carriers crossing the source barrier by thermionic emission are restricted by JFET action in the pinch-off region at the drain end of the source. This mode of operation leads to transistor characteristics with low saturation voltage and high output impedance without the need for field relief at the edge of the Schottky source barrier and explains many characteristics of the SGT observed experimentally. Two-dimensional device simulations with and without barrier lowering due to the Schottky effect show that transistors can be designed so that the current is independent of source length and thickness variations in the semiconductor. This feature, together with the fact that the current in an SGT is independent of source-drain separation, hypothesizes the fabrication of uniform current sources and other large-area analog circuit blocks with repeatable performance even in imprecise technologies such as high-speed printing.**

***Key words* — Schottky barrier, field effect transistor, thin-film transistors, source-gated transistor, organic semiconductors, printed electronics.**

I. Introduction

Source-gated transistors (SGTs) provide an alternative to the standard thin-film field effect transistor (FET) and because of their unique electrical characteristics they are attractive for several important applications. In general, the SGT has a higher output impedance and a lower saturation voltage than a geometrically identical thin-film FET (TFT) [1-3]. It therefore should perform well in analog circuits where high amplification and low power consumption is a prerequisite. A fundamental aspect of the SGT is that the current is controlled by the source barrier rather than the conductance of the channel between source and drain contacts (d, Figure 1). This is more likely to occur when source-drain gaps are small since the channel conductance increases as $1/d$. Since the current is controlled by the source barrier, electrical characteristics remain largely unchanged even when the separation between source and drain is not very uniform. The SGT should be more stable in poor quality or disordered semiconductors because the concentration of excess carriers responsible for instability is lower along the parasitic channel of length d compared to a FET [4].

To engineer a source-gated transistor, three conditions need to be met. Firstly, the source comprises a potential barrier; secondly, the gate extends under the source on the opposite side of the semiconductor (Figure 1); and thirdly, the source barrier must be able to deplete the semiconductor fully when operated in reverse bias. The first condition occurs in many technologies while the second condition is often satisfied in staggered-electrode structures. The third condition is met in most thin-film FETs (TFTs) since the semiconductor is thin.

SGTs have been made in polysilicon [3], amorphous silicon [5] and zinc oxide [6]. SGT behavior has also been shown in studies of contact effects on organic semiconductors [7, 8], and in-depth SGT studies have been recently conducted in conjugated polymer devices [9]. The SGT is an extreme example of a contact effect where the influence of the gate bias on the contact does not just modify FET behavior but completely changes the transistor characteristics.

A common feature in Schottky Barrier FETs is a peak in the transconductance g_m with gate voltage [10]. This is attributed to a change in the contact injection mechanism from thermionic emission to thermionic-field emission at higher electric fields. Similar peaks in g_m have been found in SGT structures [11] when current changes from being dominated by thermionic emission at low fields to transport across a lowered barrier at high fields.

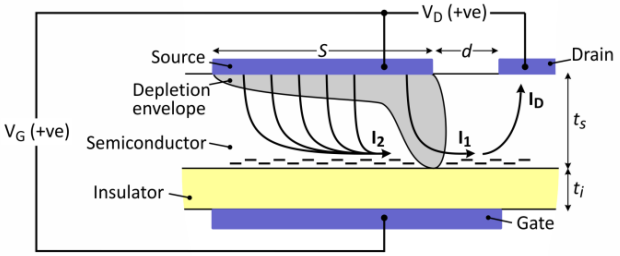

Figure 1. Schematic cross-section of a n-channel SGT in saturation. The voltage on the drain reverse-biases the source Schottky barrier. The current I_2 from the low-field region of the source is restricted by the JFET action at the edge of the source nearest the drain contact.

Therefore, the SGT has two distinct modes of operation [12]: the high electric field mode in which the current is dominated by the emission of carriers over the source barrier

in the high-field pinch-off region under the source (I_1 in Figure 1) and the low-field mode in which the current is determined by transport through the pinched-off region at the drain end of the source (I_2 in Figure 1). This latter current arises from the source area farthest from the drain where the source is screened from the drain field by the high impedance of the pinch-off region.

In the past, physical models of the SGT have mainly been concerned with the high-field mode of operation [1, 2] in which the current increases strongly with gate voltage. However, some experimental results [6] and simulations [7, 8, 13] of the SGT show the current increasing approximately linearly with gate voltage and a near constant g_m. This is a characteristic of low-field operation.

This paper is concerned with the low-field behavior of the SGT and with how transistor characteristics depend on geometrical parameters. It aims to provide a physical description for low-field operation and to identify potential applications of the SGT working in this mode.

II. High- and low-Field behaviour of the SGT

The high-field operation of the SGT is well documented. The current is determined by emission of carriers over the source barrier in the pinch-off region at the edge of the source nearest the drain contact. Assuming that the barrier lowering is proportional to electric field, this gives an exponentially increasing current with gate voltage (Figure 2a) [2].

Since the high-field region under the source covers a short area opposite the drain, we expect current in this regime to be independent of the length of the source, S [14]. However, the current will be sensitive to changes in source barrier height, ϕ_B. More importantly, the current will be sensitive to drain voltage and its respective electric field, which will act to lower the effective height of the barrier leading to the deterioration of the output impedance in saturation unless a field relief structure is incorporated [8, 15]

In low-field mode, however, the situation is very different. In this case, provided that the current under the pinch-off region (I_2 in Figure 1) is easily supplied by the saturation current of the reverse-biased source barrier, the change of current with gate voltage will depend on the characteristics of the pinch-off region. For this mode of operation, the pinch-off region behaves rather like a JFET where all the charge is located at the semiconductor-insulator interface [16]. This feature leads to a more uniform change of current with gate voltage and a near constant transconductance (g_m). An example of this behavior is shown in Figure 2b. Clearly since the current is controlled by the 'JFET' action of the pinch-off region, low-field behavior is more likely to occur when barrier heights are low and sources are long. If source barriers are high or sources are short, then the saturation current of the source barrier, I_0 may not be able to supply sufficient current for it to be controlled by the JFET action of the pinch-off region.

Assuming thermionic emission over a Schottky barrier [16]:

$$I_0 = SWAT^2 exp\left(\frac{-q\phi_B}{kT}\right), \quad (1)$$

where S is the source length, W the source width, A is Richardson's constant and ϕ_B the source barrier height. In cases when I_0 is insufficient for it to be controlled by the pinch-off region, g_m will actually fall as V_G increases and the current will tend to saturate. An example of this is shown in an organic transistor in Figure 3a. Here the current steps decrease as V_G increases and g_m falls. For a lower barrier (Figure 3b), the current is controlled by the JFET at the drain end of the source. These SGTs made with organic semiconductors (bottom gate staggered structure, spin coated amorphous polymer semiconductor and polymeric insulator) have high output impedance despite lacking a field-relief structure at the drain edge of the source. This is because, in low-field operation, barrier lowering at the drain end of the source is less important and drain current is less sensitive to drain field.

A schematic based on this behavior (Figure 4) shows how the transconductance varies with gate voltage. In the case where there is no field dependence of the source barrier height, the current is limited by I_0.

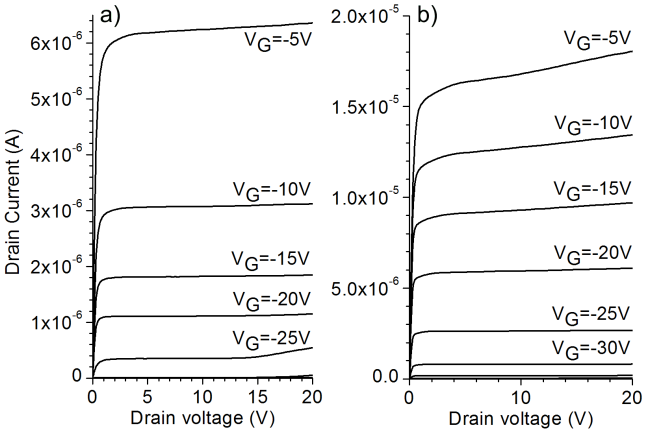

Figure 2. Transistor characteristics of polysilicon SGTs. W = 50μm, S = 4μm. a) shows current strongly increasing with gate voltage; For a lower barrier[3] the current intervals are more uniform (b). Both devices had a field plate realised by overlapping the source electrode and the source window.

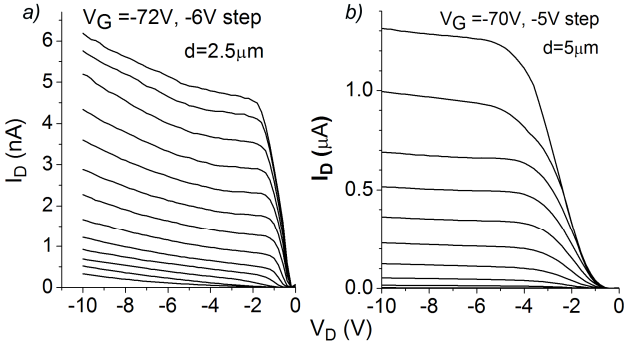

Figure 3. Source-gated transistors fabricated in organic materials operating in low-field mode having high (a) and low (b) effective source barriers. Neither has a field relief structure at the edge of the source nearest the drain contact.

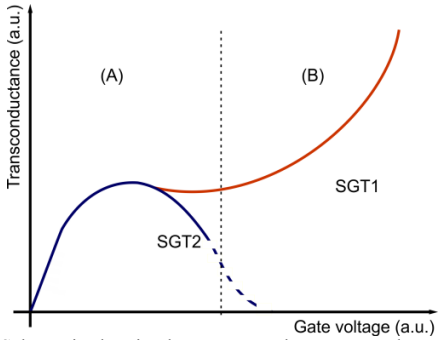

Figure 4. Schematic showing how transconductance, g_m changes with gate voltage. The barrier for SGT1 has a strong field dependence,while that of SGT2 has no field dependence. For SGT2 the current in the low-field region (A) is limited by I_0 and g_m falls to zero. For SGT1 the current increases exponentially at high fields (region (B)).

Therefore at low V_G the current is determined by the characteristic of the JFET but, as V_G increases, the current saturates and g_m tends to zero. Introducing a field-dependent barrier height enables the current to increase until, at high V_G, the high-field behavior dominates and both current and g_m increase exponentially. A plot of g_m vs. V_G for the polysilicon device shown in Figure 2a shows the bump in g_m and the transition from low field to high field behavior as V_G increases (Figure 5).

III. Numerical Simulation

A. Device simulations

Two-dimensional numerical simulations were carried out on structures similar to that shown in Figure 1 (amorphous silicon, Schottky contact model) using the commercial package Silvaco Atlas. The structure considered was derived from the ones described in [12, 13]: semiconductor thickness t_s = 20, 25, 30, 100nm, insulator (Si_3N_4) thickness t_i = 300nm, insulator dielectric constant ε_i = 7.5, source-drain gap d = 5µm, source contact length S ranging from 1 to 105 µm, drain contact length 5 µm, source contact and device width W = 1 µm source barrier ϕ_{B0} = 0.5, gate work function 4.5eV and default material parameters for amorphous silicon (intrinsic). No field relief was introduced at the drain end of the source. Simulations were performed for temperature T = 300K with the gate electrode completely overlapping the entire structure.

For this study, the values for the barrier lowering parameters in Equation 2:

$$\Delta\phi_B = \alpha E^{\gamma} + \beta\left(\frac{qE}{4\pi\varepsilon_S}\right)^{\frac{1}{2}} E^{\frac{1}{2}}, \qquad (2)$$

were: α = 0, β = 0 and 1; γ = 1.

B. Low-field simulation

At low fields, the dominant contribution to barrier lowering is the image force or Schottky effect [16]. Simulations were made on identical SGT structures with and without barrier lowering in order to examine the physical description outlined in Section II. and to explore geometrical effects. A plot of I vs. E (the electric field normal to the source interface) is shown in Figure 6 for a barrier height of 0.5eV. It is observed that with no barrier lowering, the maximum reverse current is limited to I_0 (Equation 1).

Silicon SGTs (ε_S = 11.8) similar to the structure in Figure 1 and having no source field plate were modeled with and without image force barrier lowering. The output characteristics are shown in Figure 7.

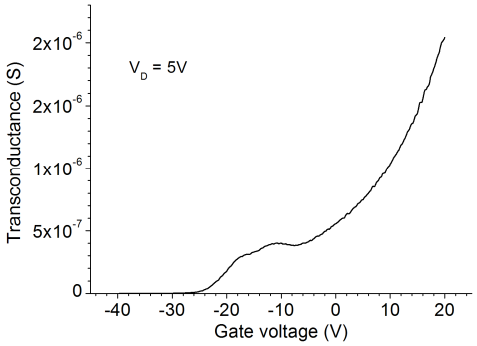

Figure 5. Plot of transconductanc vs. gate voltage for the device in Figure 2a. g_m is fairly constant between -20 and -5V before increasing exponentially at higher V_G.

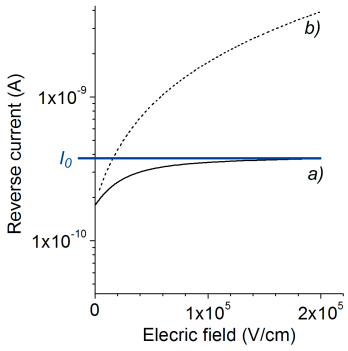

Figure 6. Reverse current of a Schottky diode with barrier height ϕ_B = 0.5eV. a) no barrier lowering; b) including image force.

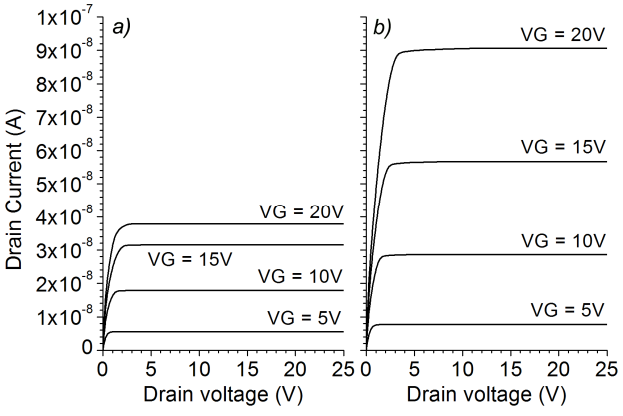

Figure 7. Output characteristics for silicon SGTs without (a) and with (b) Schottky barrier lowering. t_s = 100nm, t_i = 300nm, ε_s = 11.8, ε_i = 7.5, S = 105µm.

With no barrier lowering, the current at low V_G grows steadily but as V_G increases the source is unable to supply sufficient current and drain current tends to saturate (Figure 7a). When introducing barrier lowering via the Schottky

effect, the source can provide more current and the drain current is determined by the limiting action of the JFET (See Section II). The output characteristics have low saturation voltage and high output impedance characteristic of SGTs despite the lack of source field relief. The change in saturation voltage V_{SAT1} with gate voltage is well described by the dielectric approximation [2] used in high-field analysis, i.e.:

$dV_{SAT1} / dV_G = C_i / (C_i + C_S)$. In this case, the calculated dV_{SAT1} / dV_G is 0.018, which is close to that observed in the simulation (Figure 7b).

Plots of transconductance (g_m) against gate voltage for different source lengths are shown in Figure 8. It is seen that with no barrier lowering, g_m becomes restricted to progressively lower values as S and I_0 decrease. With barrier lowering enabled, the current continues to rise with electric field, therefore g_m does not reduce to zero but remains fairly constant, a feature also observed experimentally.

Current against source length is shown in Figure 9 for two different semiconductor permittivities, ε_S = 11.8, typical of silicon and ε_S = 4.0, representative of organic semiconductors. With high gate voltage and with no barrier lowering the current is proportional to S because it is limited by I_0, but as I_0 and S increase, the drain current becomes limited by the JFET and is independent of S (at V_G =5V for example). We note that drain current for ε_S = 4.0 is larger than when ε_S = 11.8, presumably because the shape of the depletion (pinch-off) region (see Figure 1) is different. However, drain current is the same regardless of semiconductor permittivity when the current is limited by I_0. When barrier lowering is introduced, it is much easier to get saturation of drain current via JFET action, and a current that is independent of S. Despite this, at large V_G there is a gradual deterioration of this independence. We propose that this effect occurs because the current is not completely determined by the JFET and there is some small restriction from the source barrier.

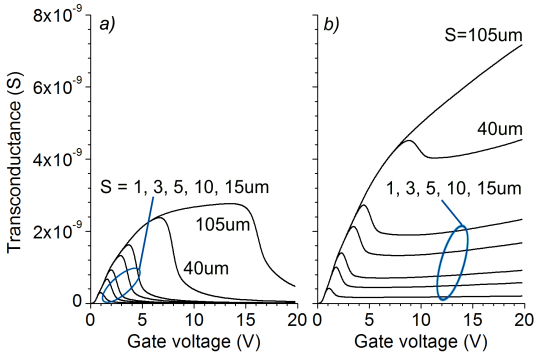

Figure 8. Plot of transconductanc vs. gate voltage for different source lengths and ϕ_B = 0.5eV: a) with no barrier lowering and b) with Schottky effect.

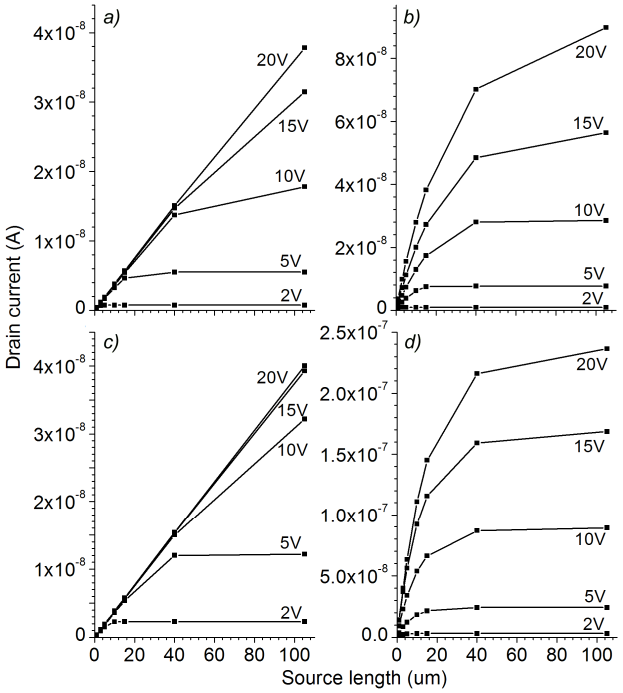

Figure 9. Drain current vs. source length. Parameters same as Figure 7, but ε_S = 11.8 (a) and (b); ε_S = 4.0 (c) and (d). (a) and (c) no barrier lowering; (b) and (d) with Schottky effect.

Based on this information, the optimum design if one wants the current to be independent of S and t_s is to make both t_s and ε_S small. Figure 10 shows the variation of drain current with S for different gate biases and for a t_s = 25nm ± 20%. It is seen that the current is almost identical for large S despite substantial variations in the layer thickness.

The simulations of low-field behavior agree very well with the physical description discussed in Section II and the low-voltage measurements on SGT devices. Clearly the low-field behavior depends on many parameters including barrier height and source length (Equation 1) but the general features and mechanisms that determine the current below I_0 seem to be well described by the JFET action in the pinch-off region at the drain end of the source.

IV. Potential Applications

The main features of the SGT, namely a high output impedance and low saturation voltage, make it useful for analog and low-power circuits. In the high-field mode of operation, however, the current is sensitive to drain field [2, 8, 15], therefore some form of field relief at the drain end of the source is required. This is easily done in silicon technology [3] but in other systems, such as solution-processed organics, introducing field relief is more problematic. In low-field operation, the current is less sensitive to drain field and a high output impedance can be preserved (Figures 3, 7) enabling organic source-gated transistors to be used for a variety of low-power application. Moreover, low-field SGTs can be designed to have virtually

constant transconductance over a large range of gate voltage, allowing larger input swings and lower distortion when used in the design of transconductance amplifiers.

The drain current in an SGT at a given gate voltage has been shown in the past to be independent of source-drain separation [2]. We have shown that, in properly designed low-field SGTs, drain current can be made to be independent of variations in source length (S) and semiconductor thickness (t_s) as well. The only geometrical parameters remaining are the width of the device (W) and the insulator thickness t_i. In practice, W can be made wide enough so variations (as a percentage) are small. Furthermore, the insulator can be thick with small relative variations across a large area. The SGT offers the prospect of providing uniform current sources in technologies where patterning is imprecise, such as high-speed, high-throughput printing, because geometrical variations and alignment errors do not matter for such devices.

Long source lengths and their associated capacitance, together with the reduced current due to the source barrier will result in significantly slower devices compared to standard FETs but there are many applications where uniform current is more important, particularly if it can be obtained at low cost. This is of great practical importance as it would allow circuits to be made with consistent performance on large-area substrates without resorting to stringent process control or complex compensation circuitry.

V. CONCLUSIONS

There are two distinct modes of operation of a source-gated transistor (SGT). In the high field mode, the current is determined by the field dependence of barrier lowering at the drain end of the source contact, where the semiconductor pinches off. This current is sensitive to drain field, and in order to achieve good output impedance, some form of field relief at the edge of the contact is required [15].

In the low-field mode of operation, the current comes from the source region furthest form the drain. Provided that the reverse saturation current of the barrier is sufficient, in this mode the current is controlled by the JFET action of the pinched-off region at the edge of the source and high output impedance can be obtained without the need for field relief. This situation is very advantageous when simple staggered structures are used with semiconductors without well developed, elaborate technologies, such as solution-processed organics.

Simulations of the SGT in low-field mode show that the transistor can be designed such that the current at a given gate voltage is independent of source length (S) above a critical value. This value depends on the barrier height and its ability to provide sufficient current for it to be restricted by the JFET.

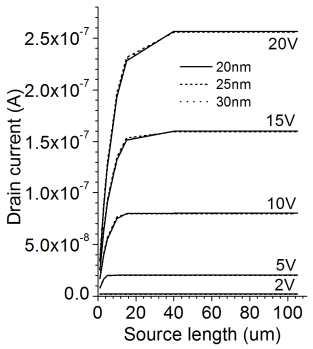

Figure 10. Drain current (I_D) vs. source length (S) for different gate biases. t_i = 300nm, t_s = 20, 25 and 30nm, , ε_s = 4.0, ε_i = 7.5. It is seen that for larger S, is independent of both S and t_s at a given gate voltage.

Simulations also show that if the thickness of the semiconductor layer is reduced and $C_S >> C_i$ we can have a situation where the current does not vary with semiconductor thickness. We therefore can engineer structures in which current is independent of all geometric variations apart from source width and insulator thickness. However, provided that the insulator is thick and the device wide compared to reasonable variations, these two parameters should not represent obstacles to uniform current.

These results suggest that it should be possible to make uniform current generators and robust circuit blocks on a large substrate area using simple but imprecise technologies such as printing, a technology ideally suited for organic electronics.

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John M. Shannon was Head of the Display and Large Area Electronics Group at Philips Research, UK (1985 – 1994). He is Professor of Semiconductor Devices at the University of Surrey and a Fellow of the Royal Academy of Engineering.

Radu A. Sporea (M'05) is a Royal Academy of Engineering Research Fellow at the University of Surrey, working on low power and large area electronics. He is a member of SID and IET and was a Design Engineer for Catalyst Semiconductor.

S. Georgakopoulos recently completed his PhD on conjugated polymer transistors at the Advanced Technology Institute, University of Surrey, U.K.

M. Shkunov holds an academic position at Advanced Technology Institute, University of Surrey, and leads research activities on large area electronics. His interests cover functional inorganic nanomaterials, organic semiconductors, printing and deposition technologies, device engineering and physics. He has (co)-authored more than 90 publications, including articles in peer reviewed journals, book chapter and patents.

S. Ravi P. Silva, FREng is the Director of the Advanced Technology Institute (ATI) at the University of Surrey and winner of the Royal Society "Clifford Patterson Medal and Lecture". He has published over 380 journal papers and 20 patents.