Performance trade-offs in polysilicon source-gated transistors

R. A. Sporea, J. M. Shannon, S. R. P. Silva
Advanced Technology Institute
University of Surrey
Guildford, Surrey, GU2 7XH, U.K
r.sporea@surrey.ac.uk

M. J. Trainor
MiPlaza, Philips Research
High Tech Campus 4
5656 AE Eindhoven, The Netherlands
mike.trainor@philips.com

N. D. Young
Philips Research
101 Cambridge Science Park, Milton Road
Cambridge CB4 0FY, U.K
nigel.young@philips.com

***Abstract*—Self-aligned Schottky-source source-gated transistors (SGTs) have been made in polysilicon. The structures enable a direct comparison to be made between a SGT and a standard thin-film field-effect transistor (FET) on the same device. SGTs having excellent characteristics have been fabricated, with intrinsic gains approaching 10,000. The effects of bulk doping in the polysilicon and of the source barrier modification implant are considered in the context of the electrical output characteristics. It is shown that the choice of source length is a tradeoff between device speed and current uniformity.**

I. INTRODUCTION

Source-gated transistors (SGTs) operate using the field dependence of the current through a reverse biased source barrier. As such, their characteristics and properties are very different from those of thin-film field effect transistors (FETs). In this paper we report measurements and modeling on SGTs in polysilicon and show the well known advantages of the SGT compared to standard FETs, namely high output impedance and low saturation voltage [1, 2]. The kink effect [3] due to bipolar amplification of carriers generated in the high field regions around the drain is absent, postulated as a result of minority carrier extraction by the reverse biased source barrier.

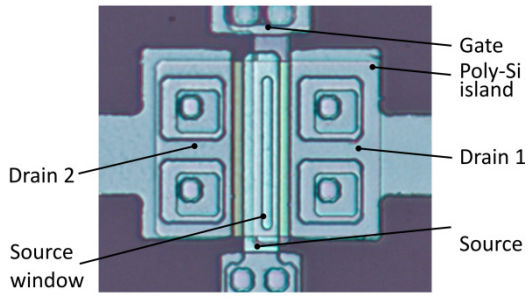

Figure 1. Microphotograph of a self-aligned polysilicon SGT.

In this paper, special attention is given to how the electrical characteristics and intrinsic gain depend on the doping of the polysilicon and on the barrier modification implant. There is some consideration of how source length affects current density and frequency response. We also introduce the hybrid mode of operation in which the current is influenced by the parasitic FET in series with the source barrier. It is suggested that this mode of operation can explain the very low temperature dependence of the drain current measured in some devices. These polysilicon SGTs are particularly relevant to high performance thin-film analog circuits.

Source-gated transistors were fabricated in polysilicon on a glass substrate using back exposure and ion implantation to align a bottom gate with ohmic drain contacts on either side of a Schottky source barrier. A micrograph of one of the devices is shown in Fig. 1. A 40nm layer of polysilicon was formed on top of 200nm SiN_x plus 200nm SiO_2 using a 308nm XeCl excimer laser. The Schottky source barrier was realised via a window in 120nm of SiO_2 and was modified using low energy implants of either P or BF_2. The chromium was extended over the oxide to form a field plate structure to provide field relief at the edge of the source (Fig. 2).

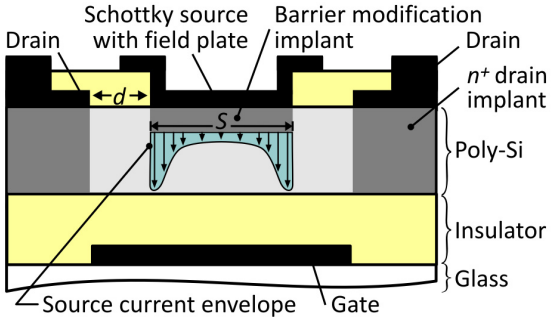

Figure 2. Schematic cross-section of a self-aligned SGT showing current crowding at the edge of the source.

II. RESULTS AND DISCUSSION

A. *Effect of bulk doping on SGT and FET characteristics*

Since the drain contact of a SGT is forward biased in the on-state, it can be a barrier just like the source. The source and the drain can therefore be reversed to give symmetrical SGT characteristics. However, in the structure made here, the drain contact is ohmic. Therefore, if we make the ohmic contact the source we get an FET and the characteristics of the SGT can be compared directly to those of the FET on the same device. An example is shown in Fig. 3.

The high output impedance and the low saturation voltage of the SGT are apparent, as is the kink effect in the FET. The on-current through the SGT depends on the source barrier height (see Fig 5). It is also seen that the FET does not switch off as well as the SGT. The off-current of the FET increases with n-type doping in the polysilicon (Fig. 4) but we see that the off-current of the SGT is always the same independent of doping. This is because the reverse biased source barrier of the SGT blocks current flow through the polysilicon between source and drain.

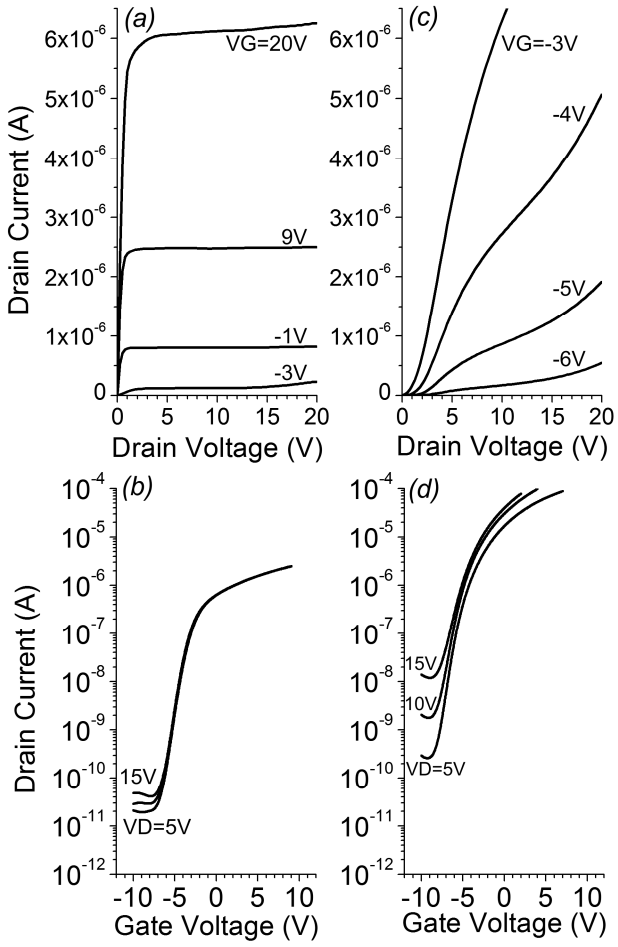

Figure 3. Characteristics of SGT (a), (b) and FET (c), (d) behaviour, at a similar current, obtained by interchanging the source and the drain on the same device. W=50μm, S=8μm, d=10μm, $1\cdot10^{13}$/cm^2 BF_2 barrier modification implant.

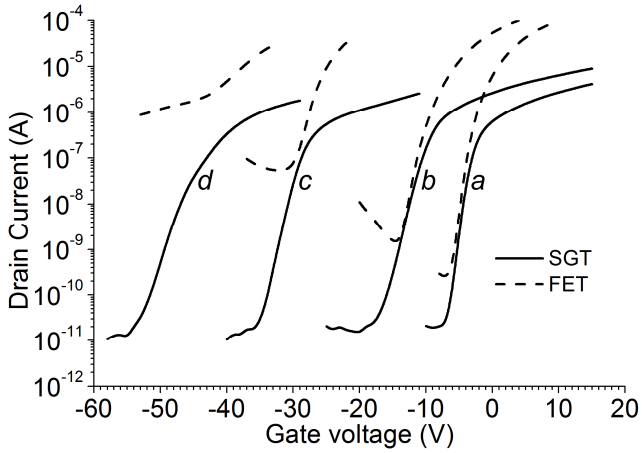

Figure 4. Transfer curves of SGTs and FETs for different substrate dopings. W=50μm, S=8μm, d=10μm, $1\cdot10^{13}$ BF_2 barrier modification implant; areal doping: a) $0.5\cdot10^{12}$; b) $1.5\cdot10^{12}$; c) $2.5\cdot10^{12}$; d) $3.5\cdot10^{12}$ /cm^2 n-type; V_D=15V.

B. *Effect of barrier modifying implants*

Low energy BF_2 or P implants into the source window were made before metallization in order to affect the Schottky barrier height. The transfer curves (Fig. 5) are consistent with an increase in barrier height for p-type doping and a decrease for n-type doping, as expected from barrier modification theory [4]. However, the changes in current are small when considering the doses used, which suggests poor electrical activity. This is not surprising, because the annealing temperature was only 500^{O}C to avoid glass compaction. All transistors showed SGT behaviour, even those with the highest n-type implants. As can be seen, the current handling of the SGT can approach that of a FET having the same geometry by tailoring the source barrier. Also, changing the source barrier height has no effect on the off-current; on to off ratios can be more than 6 orders of magnitude.

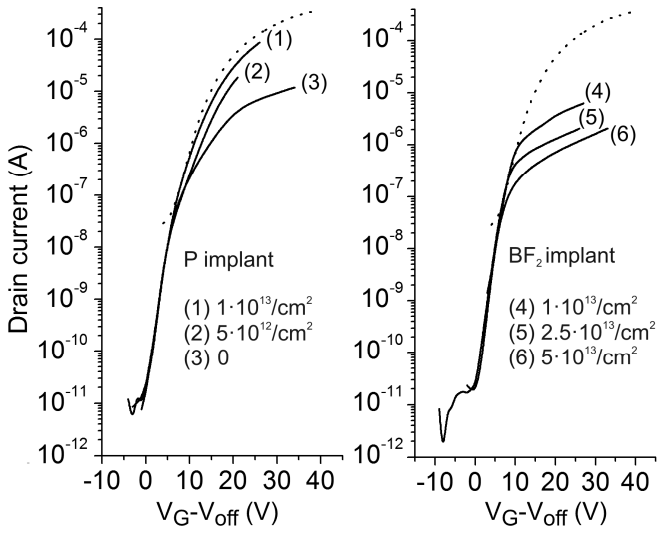

Figure 5. Transfer curves for different barrier implants at V_D=5V. Dotted line – FET, continuous line – SGT.

C. *Effect of bulk doping and barrier modifying implants on intrinsic gain*

The high output impedance of the SGT makes it very useful for analog circuits. A key parameter in this context is the intrinsic gain, g_m/g_d. The high impedance arises because the device first pinches off at the source (at $V_D=V_{SAT1}$), and then at the drain, as in a conventional FET (at $V_D=V_{SAT2}$). [5]

Fig. 6 shows measured intrinsic gains for identical devices but for different n-type doping levels in the polysilicon. Peak gains are very high, approaching 10,000. The peaks in the curves tend to be associated with V_{SAT1} and V_{SAT2} [5] while the falloff in gain at high V_D is related to an increase in g_d due to carrier generation in the high field regions at the drain end of the device.

It is seen that the gain at low V_D around V_{SAT1} increases with decreasing substrate doping levels. This can be explained by an increase in the electric field at the periphery of the source as V_D increases and the depletion layer expands towards the drain. For higher doping levels in the polysilicon, the increase in electric field will be greater, as will the increase in g_d. At higher V_D, however, gains are greatest for higher substrate doping. Since g_m is the same, this effect must be due to carrier generation in the high field regions.

Overall, the gain envelope over V_D is highest for the more lightly doped polysilicon and gain variations with V_D are due to changes in the output conductance.

In Fig. 7, intrinsic gains are shown for two transistors with the same doping level in the polysilicon but with different barrier modification implants. Both are operating at the same current, but gm in (a) is larger than in (b) (see Fig. 5), which explains its higher intrinsic gain. In this case, while the peaks and the dips are due to changes in g_d, the downward shift of (b) relative to (a) results from a change in g_m. For comparison, the intrinsic gain of the FET is ~10.

D. *Effect of source length on current density*

The change of current with source length (S) has been measured in the past and it has been shown that the

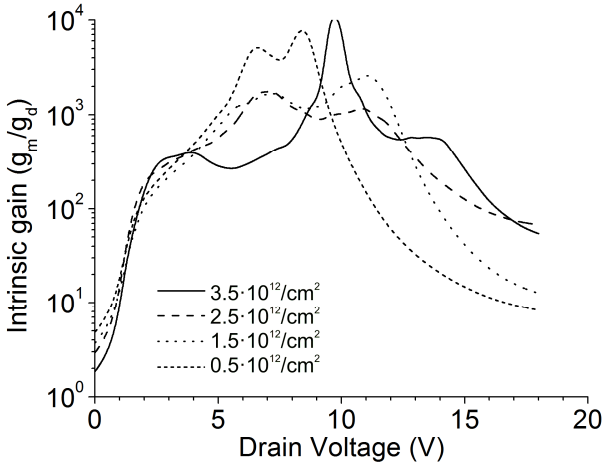

Figure 6. Intrinsic gain as a function of drain voltage for different substrate doping levels.

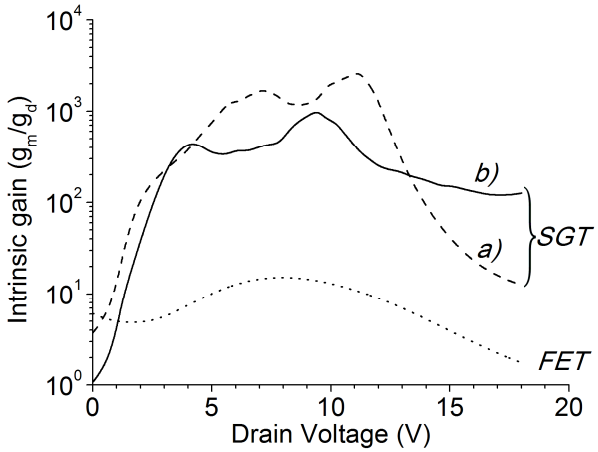

Figure 7. Intrinsic gain for a) $1\cdot10^{13}$/cm^2 P and b) $5\cdot10^{13}$/cm^2 BF_2 measured at 1μA. W=50μm, S=2μm, d=10μm, $0.5\cdot10^{12}$/cm^2 n-type bulk doping. Also shown is the gain of an equivalent FET

current is concentrated at the edge of the source as shown in Fig. 2. This has important implications because calculations show [6] that the cutoff frequency (f_T) of the SGT is proportional to the average current density (J_S) passing though the source. In Fig. 8, the results of computer simulations using Silvaco Atlas are plotted for drain current over a range of source lengths. Fig 8(a) shows that, as source length increases, the drain current saturates (S_{SAT}). Therefore, increasing S reduces J_S, since the current becomes almost independent of S. If high f_T is required, the source should be less than S_{SAT}. If current uniformity is required, however, S should be greater than S_{SAT}. The current mismatch between two devices with a change of 0.1μm in source length is shown in Fig. 8(b).

E. *Hybrid operation and the temperature dependence of drain current*

One parameter that is worse in a Schottky source SGT compared with an FET is the temperature dependence of the current. Since there is a barrier at the source, the current is thermally activated. Although we have been able to pull barriers down to around 150meV, this is still much larger than that measured in a polysilicon FET [7]. One way of reducing the temperature coefficient would be to make a thermionic emission source in which, under bias, carriers would tunnel through the barrier at the Fermi level of the metal [8]. This structure would require careful engineering using thin insulating layers and doping profiles.

The activation energy of current transport against (V_G-V_T) is shown for two SGT devices in Fig. 9. Device (a) is typical of a Schottky source SGT; the source barrier is pulled down by the gate but remains high. However, we have measured SGT devices where the activation energy falls to very low values with increasing V_G, as shown in Fig. 9 (b). Since no deliberate attempt had been made to make a field emission source, it seems unlikely that the low activation energy is due to the source, but it is possible. It was observed that devices with low activation energies operated at the highest currents

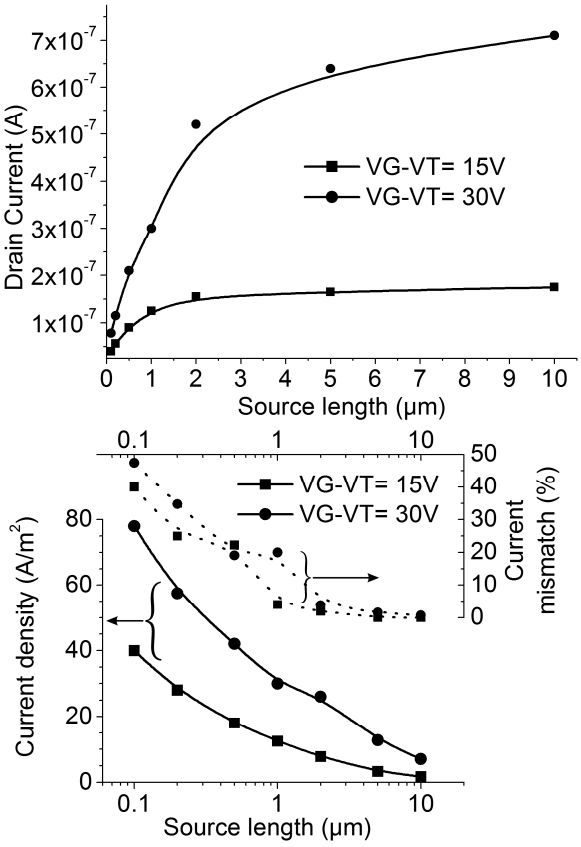

Figure 8. Computed vatiation of current and current density through the source as a function of source length. Current mismatch was calculatd for a 0.1µm change in source length.

and there was a small increase in V_{SAT1} compared with low current devices, at the same V_G.

We conclude, therefore, that these devices operate in a hybrid mode in which the on-state is partly controlled by the source barrier and partly by the parasitic FET.

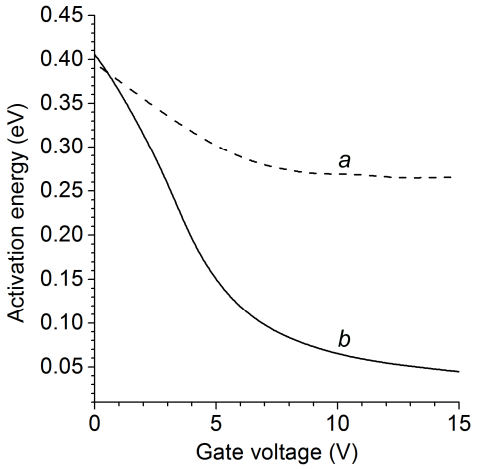

Figure 9. Change of activation energy for current transport for a) a SGT operating at low current and b) a SGT operating at high current.

It seems that there is a negative feedback effect in which the FET, with its very low activation energy of the current restricts the change of current through the source. This hybrid mode could be very important when small changes of current with temperature are required. The tradeoff is a small increase in V_{SAT1}. To fully understand the interaction between the source barrier and the parasitic FET in this situation requires a further 2D analysis.

III. Conclusions

Self-aligned polysilicon SGTs have been made. Measurements show an absence of the kink effect responsible for degrading the output characteristics of polysilicon FETs. Output impedances are very high, in some cases resulting in intrinsic gains approaching 10,000. While a FET cannot be switched off when the semiconductor is highly doped, an SGT can always be switched off and the off-current is independent of doping level. The intrinsic gain envelope is broader for higher substrate doping but the highest gains were observed with the lowest doping. It is shown that the choice of source length is a tradeoff between speed and current uniformity. Some high current transistors with SGT characteristics have very low activation energies. We attribute this behaviour to a hybrid mode of operation. It has been shown that there are a number of options and tradeoffs which should enable high performance digital and analog circuits to be made in polysilicon.

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