

Polysilicon Source-Gated Transistors for Mixed-Signal Systems-on-Panel

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The performance benefits of using source-gated transistors (SGTs) in analog large-area electronic circuits are examined practically and via numerical simulations. In current mirror circuits made using thin-film technology, significant advantages are observed for SGT implementations. A comparison of current mirrors implemented with standard field effect transistors (FETs) and SGTs shows that the SGT version can operate at a lower voltage and has larger output dynamic range for a given device geometry. The results are explained in relation to the saturation mechanisms of the SGT and are supported by experimental measurements of polysilicon devices.

Introduction

Thin-film polysilicon technology is widely used in large area electronics, such as flat panel displays and touch-sensitive input devices (1) due to its ability to deliver large scale integrated circuits at a comparatively low cost. Significant research efforts have been made recently towards integration of complex electronic circuitry directly onto the flat panel, resulting in System on Panel (SoP) architectures (2). However, polysilicon thin-film field-effect transistors (FETs) have generally modest performance when being used in analog circuits. A relatively new device structure, the source-gated transistor (SGT) (3), has the potential to extend the applicability of disordered semiconductors to analog and mixed signal circuits.

Source-Gated Transistor Operation

A Schottky barrier SGT (Figure 1) is comprised of a metal-semiconductor barrier at the source terminal in series with a parasitic FET transistor. The gate extends over the source and, apart from its usual role of modulating the FET channel conductance, controls the effective height of the source barrier. The relevance of the SGT to analog circuits is a consequence of the defining characteristics of the SGT: reduced kink effect, low saturation voltage and high output impedance in saturation. The reverse biased barrier at the source prevents bipolar amplification of carriers generated in the high-field regions near the drain, thus reducing the kink effect (4). Due to the SGT's construction (Figure 1), when the drain voltage is increased, the current saturates as the semiconductor area under the source is depleted of free carriers at a voltage

$$V_{SAT1} = (V_{GS} - V_T) \cdot C_i / (C_i + C_s), \quad [1]$$

where V_T is the threshold voltage and C_i and C_s are the insulator and semiconductor capacitances, respectively (3). At $V_{SAT2} = V_{GS} - V_T$, the channel between the source and the drain pinches off at the drain, similar to a standard FET, and saturation becomes stronger. Since the current is controlled by the reverse biased source barrier, the drain current in saturation is independent of source-drain separation (3) and the output impedance in saturation, Z_O , can be very high (5), especially for $V_{DS} > V_{SAT2}$.

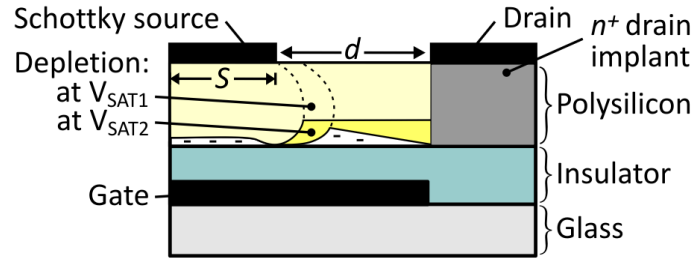


Figure 1. Schematic cross-section of the self-aligned polysilicon SGT, showing source length (S), source-drain separation (d) and depletion region when the channel pinches off at the source ($V_{DS} = V_{SAT1}$) and at both the source and the drain ($V_{DS} = V_{SAT2}$), as explained in the text.

Results and Discussion

Typical output characteristics measured on an excimer laser crystallized polysilicon SGT are shown in Figure 2a. The thick insulator (300nm equivalent oxide thickness) ensures that V_{SAT1} is very small, at the expense of a low transconductance. Figure 2b shows that the output impedance Z_O is very high over a wide range of drain voltage, which is not the case for a typical FET design. By swapping the source and drain terminals, the Schottky barrier is forward biased and the device operates as a FET. Figures 2c and 2d show the measurement results for the same device in the FET configuration: saturation occurs at high voltages and output impedance is comparatively low. The region under the Schottky barrier is usually doped in order to modify the barrier profile and this may be a disadvantage for operation in the FET mode, as the drain of the FET may be highly resistive as a result. However, careful design can minimize this effect and it is conceivable that the same device can be used either as a SGT or as a FET by changing the direction of the current through the semiconductor. This would allow circuits to be designed with both FET and SGT devices on the same substrate by using a single technology platform.

As a result of the source barrier controlling the current, the SGT has lower current than the FET for a given gate bias. Despite their lower transconductance³, SGTs can operate at high frequency (6) if the source-drain gap (d) and source length (S) (Figure 1) are optimized. d can be made very small without the need for precise dimensional control, ensuring that frequency behavior is not compromised by the conductance of the parasitic FET channel. S should be set as a process parameter to obtain the highest current density through the source.

These properties of the SGT suggest that this type of device is well suited to circuit applications in which low operation voltage or high output impedance is required. The basic circuit blocks used to accurately replicate d.c. currents, called current mirrors, require high output impedance to copy current precisely in analog bias schemes. Similarly, as high-impedance active loads for high gain amplifier circuits, such current mirrors circuits are essential constituents for future mixed-signal system-on-panel configurations.

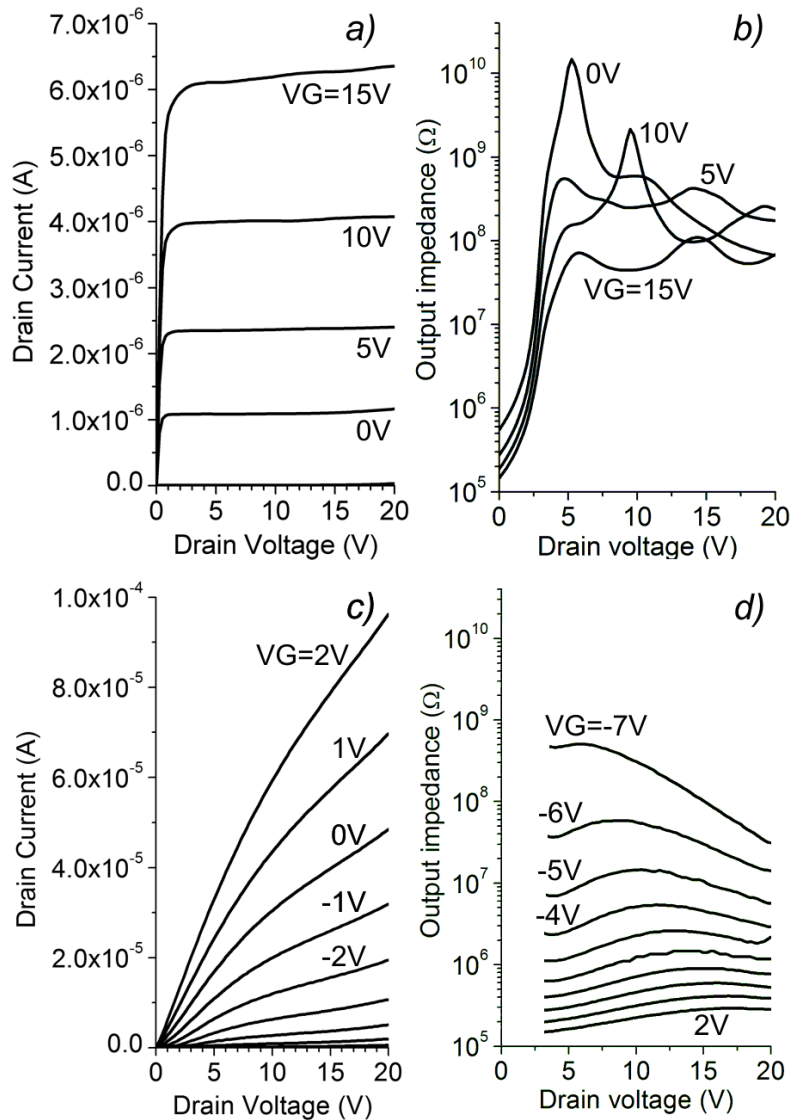


Figure 2. *a)* Output characteristic and *b)* output impedance measurements at several gate voltages for a self-aligned polysilicon SGT with $W=50\mu\text{m}$, $S=8\mu\text{m}$, $d=10\mu\text{m}$, $3.5 \cdot 10^{12}/\text{cm}^2$ n-type doping in the polysilicon and $1 \cdot 10^{13}/\text{cm}^2$ p-type barrier modification implant; *c)* output characteristic and *d)* output impedance measurements for the same device operated as a standard FET by swapping the source and drain terminals.

Using numerical simulations, we have compared the performance of standard current mirrors built with polysilicon FETs and SGTs respectively (Figure 3). Simulations have been performed using the Silvaco mixed-mode environment. For FETs, we have used

commercial polysilicon SPICE, free from the limitations described in relation to Figures 2c and 2d, thus ensuring a fair comparison. Since no accurate SPICE model is available for the SGT, these devices were simulated using numerical device modeling and were embedded in the mixed-mode circuit simulation flow.

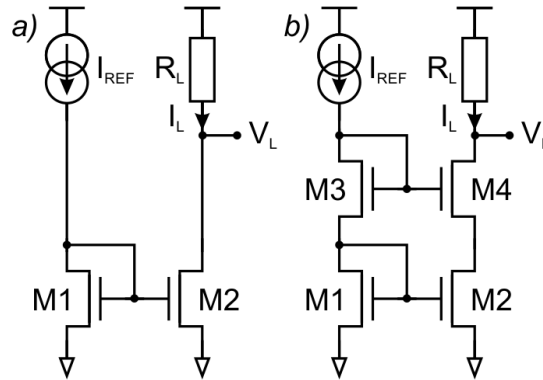


Figure 3. Schematic of the *a)* simple and *b)* cascoded n-type current mirror.

For this initial investigation we neglect geometry and threshold mismatch with all transistors being identical. Transistor M1 is connected in the diode configuration (Figure 3a), with the gate tied to the drain. A current $I_{REF} = 500\text{nA}$ is injected into the drain of M1 and, by virtue of the common gate bias of M1 and M2, is copied to the drain of M2 (I_L). Non-idealities such as short channel and kink effects, lead to a mismatch between I_{REF} and I_L which is dependent on the drain-to-source voltage (V_{DS}) of M2. A cascode configuration (Figure 3b) minimizes these effects by dropping the variable output voltage across M4 and keeping V_{DS} of M2 relatively constant regardless of V_L , and close to that of M1.

FET current mirror performance was assessed based on the output voltage swing (i.e. range of V_L) for which I_L matches I_{REF} to a given accuracy (0.5% and 10% were considered). The results are shown in Figure 4 (considered geometries were: $W=50\mu\text{m}$, $L_{FET}=10\mu\text{m}$ and $W_{FET}=50\mu\text{m}$, $L_{FET}=100\mu\text{m}$). As expected, a longer channel FET needs a higher gate bias in order to sink the same current. Accurate current copying starts from a higher voltage but has less dependence on V_{DS} and slightly better performance can be achieved, as indicated by the overall longer bars. The cascode configuration performs substantially better, but requires higher supply and load voltages to account for the additional threshold voltages of M3 and M4. It is apparent however that all FET configurations have a very small range of V_L (several 100mV to $\approx 2\text{V}$) over which I_L is within 0.5% of I_{REF} .

For comparison, simulations were performed on SGT the current mirror comprised of devices with $d=1\mu\text{m}$ and $W=35\mu\text{m}$, which are supported by measurements on self-aligned polysilicon SGT structures (Figure 2). Despite the value of d_{SGT} being an order of magnitude less than L_{FET} , the simple SGT current mirror begins operating at a much lower voltage and has a greatly improved output voltage swing, in the range of 10-20V for an accuracy of 0.5% (Figure 4). The drain current of the SGT is controlled by the source barrier, and is thus independent of the source-drain separation and, as a

consequence, d can be made very small, resulting in area savings and potential of being operated at a higher frequency. A cascode configuration is not necessary for the SGT mirror circuit and 10% accuracy can be achieved from below V_{SAT1} up to the supply voltage. Repeating the simulation for A device with $d=1\mu\text{m}$ and $W=10\mu\text{m}$ results in an even larger output voltage range. Just as in the FET implementation, the narrower devices require a higher gate bias to be able to sink the same current. This increases the minimum operating voltage of the mirror, but at the same time allows M2 to function in a regime in which the kink effect⁴ is diminished. Choosing the right geometry for the transistors allows the operation of the current mirror either over a large range of output voltage, in the case of wider devices, or starting at a lower V_L , for narrower ones (Figure 4). As far as process variability is concerned, the mirror is immune to mismatch in d and S (Figure 2) and alignment errors (7), leading to accurate current copying over a large range of V_L .

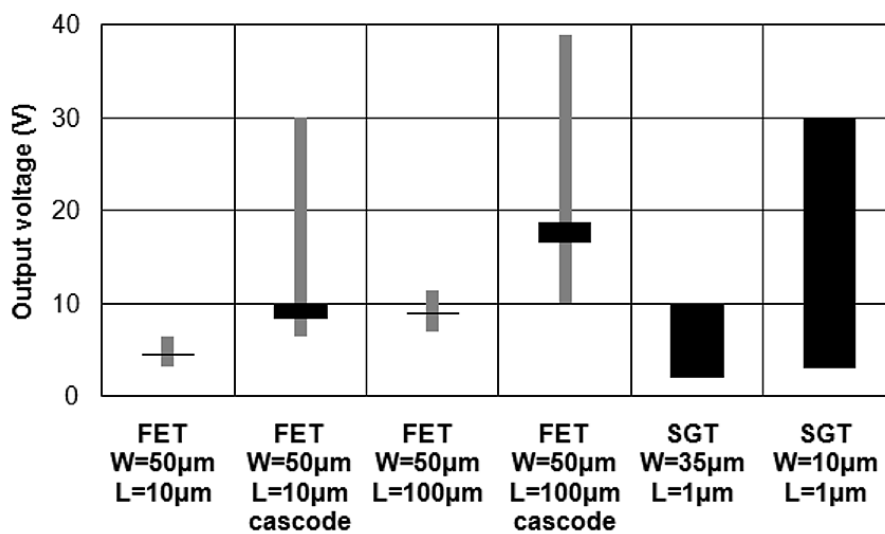


Figure 4. Simulation results of output voltage range for 10% (grey) and 0.5% (black) current copying accuracy. Cascode versions of the FET current mirror have significantly better performance than simple mirrors. Similarly, increasing the FET channel length improves the current copying accuracy. However, the performance of the SGT mirror is far superior for a much shorter source-drain separation: 10% accuracy can be achieved throughout the saturation region but, more importantly, 0.5% accuracy is realized over a much larger output voltage range than the equivalent FET circuit; cascoding is not required to achieve good performance. Narrower SGTs need a higher gate voltage to sink the same current and raises the minimum operating voltage, but this higher bias allows operation in a region of reduced kink effect compared to the wider devices.

Conclusions

In this paper we have outlined the applicability of the SGT to current mirror circuits in polysilicon. Simulation results show that current mirrors using SGTs can copy current with an accuracy of 0.5% over a range of output voltages which is one to two orders of magnitude higher than can be obtained with a similar FET design. Minimum output voltage is also significantly lower. In an SGT, as the drain bias is increased, the semiconductor pinches off first at the source and then at the drain, leading to low

saturation voltages and kink-free, high Z_O characteristics to high V_{DS} . Simulation results are supported by experimental data.

The SGT can function as an FET by swapping the source and drain terminals, (a desirable property with for incorporating both types of device in the same circuit design). Furthermore, the SGT can easily be integrated in the majority of thin-film technologies and can be used alongside regular FETs on the same panel. Therefore, it is suitable for high performance analog applications made with a variety of semiconductors (8).

Based on our findings, the current mirror circuit using SGTs is proved to be an essential building block for bias circuits or as active loads for high-gain amplifiers as part of future system-on-panel applications made in large-area semiconductors.

Acknowledgments

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