Abstract—This paper describes some of the performance characteristics of self-aligned polysilicon Schottky Source-Gated Transistors (SGTs) made on glass by laser annealing of amorphous silicon. The threshold and Schottky barrier height are tuned by varying the dose of dopants in the bulk and under the source respectively. These devices are well suited for analog applications owing to their low saturation voltage, low drain field dependence of the current and intrinsic gain which is in excess of 1000 for well designed structures. Double drain operation leads to $f_T \approx 100\text{MHz}$ for non-optimized devices.

Index Terms—Source-Gated Transistor, polysilicon, analog circuits, Schottky barrier

I. INTRODUCTION

The concept of the Source-Gated Transistor (SGT) has been introduced in [1]. The main performance characteristics of this device, namely high output impedance in saturation and low saturation voltage were examined in [2-3], by characterization of structures made in hydrogenated amorphous silicon and polysilicon.

This paper discusses a wider range of properties of SGTs and their applicability to circuit design. To this end, measurements have been made on back-gate, Schottky source, polysilicon devices, the structure of which is outlined below.

A typical self-aligned device is shown in Fig. 1. Fig. 2 illustrates a schematic cross-section of the device in Fig. 1.

The Cr gate was defined on a glass substrate. A gate insulator consisting of 200nm SiN$_x$ and 200nm SiO$_2$ was deposited by PECVD. A 40nm-thick layer of a-Si:H followed and was dehydrogenated by baking at 450°C. Back exposure through the glass was used to define the n$^+$ drain contacts, which were self-aligned to the gate. The polysilicon was formed by laser annealing. The Schottky source contact was modified by using implants of BF$_2$ or P which were annealed at 500°C. Finally, metal contacts were formed, incorporating a source field plate. (Fig. 2)

The following sections describe the performance of the SGT in d.c. (on- and off-state) based on measurements and discuss frequency behaviour.

II. THE SGT “ON” STATE

We assume the on-state to begin at a gate voltage where the drain current is controlled predominantly by the source barrier.

A comparison between the transfer characteristics of an SGT and a Thin Film Field-Effect Transistor (FET) is given in Fig. 3a. The FET characteristics were achieved by operating the SGT in reverse (i.e. swapping source and drain terminals). The threshold shift between FET and SGT is due to the barrier modification implant under the source.

A. Saturation regimes (double pinch-off)

In an SGT, the role of the gate is two-fold: to change the channel conductance in the parasitic FET formed between the source and the drain and to modulate the effective height of the source barrier.

Fig. 1. Microphotograph of the structure. Source window area: 2μm * 50μm.

Fig. 2. Schematic cross-section of polysilicon SGT, showing source length (S) and source-drain gap (d).

Fig. 3. a. Transfer characteristics for FET and SGT; b. Output characteristic for the same SGT. W=50μm, S=2μm, d=10μm, 2.5·10$^{13}$/cm$^2$ n-type doping in the polysilicon layer and 10$^{13}$/cm$^2$ p-type doping in the barrier modification implant.
When the drain voltage increases, the channel first pinches off under the source (Fig. 4b), resulting in saturation at a lower $V_D$ than $V_G - V_T$. In fact, saturation at the source occurs at a drain voltage $V_{SAT1} = (V_G - V_T) \cdot C_i / (C_i + C_s)$, where $C_i$ and $C_s$ are the insulator and semiconductor capacitance per unit area respectively [1] (Fig. 3b and Fig 4a).

This low saturation voltage can be exploited to allow greater voltage swing in gain stages or to minimize drop-out in linear circuits. Increasing $V_D$ up to and above $V_{SAT1} = V_G - V_T$ results in pinch-off at the drain, as in a standard FET, in addition to pinch-off at the source. (Fig. 4)

B. Output impedance in saturation

Because the current in saturation is controlled by the source (or by the source and the channel above $V_{SAT}$), very low drain field dependence can be achieved. In well passivated devices, the output impedance in saturation is very high (Fig. 3b), and sometimes can even be negative. This holds true even at high drain voltage; regular FETs suffer from the so-called “kink effect” [4], but the SGT is less affected, due to its construction. The reverse biased barrier at the source extracts any minority carriers generated in high field regions and prevents bipolar amplification. This property makes the SGT well suited to applications where an active load with very high impedance (low output conductance) is required.

C. Intrinsic gain

By studying Fig. 3a and neglecting the threshold mismatch, one possible shortcoming of the SGT becomes apparent. The drain current of the SGT must be less than that of the FET (at least a factor of 5) otherwise the current would be influenced by the parasitic FET [1]. As a consequence, $g_m$ will also be lower in the SGT.

**Fig. 4.** a. Schematic showing drain current changes with drain voltage for two values of $V_G$; b. Schematic depicting the two pinch-off states of the SGT; left: pinch-off occurs first at the source ($V_{SAT1}$ in a); right: the semiconductor pinches off at both the source and the drain when $V_D = V_G - V_T$ ($V_{SAT2}$ in a.). A is the corner of the source most sensitive to drain field. B is the position of the floating source of the parasitic FET.

Fig. 5. a. Intrinsic gain measurements on a device with $W=50\mu m$, $S=2\mu m$, $d=10\mu m$, $2.5 \cdot 10^{12}/cm^2$ n-type doping in the polysilicon layer and $0.5 \cdot 10^{13}/cm^2$ n-type doping in the barrier modification implant; b. Activation energy versus gate bias over the threshold for a similar device with $1 \cdot 10^{13}/cm^2$ n-type barrier modification implant and $V_D=5V$.

However, owing to the exceptionally low output conductance discussed above, the intrinsic gain ($g_m/g_d$) of the SGT can be extremely high, even though the source barrier is higher than optimum. Fig. 5a shows the dependence of intrinsic gain on drain voltage at three gate voltages just above threshold (only one of the drain terminals was connected for this measurement). In the region of $V_{SAT1}$ the gain increases with voltage as $g_m$ increases. The peak to the right, associated with $V_{SAT2}$ shifts to higher drain voltage as $V_G$ is increased.

The shift is roughly consistent with the 1V/V change in $V_{SAT2} = V_G - V_T$, as in a standard FET. Around $V_{SAT2}$ the gain reaches several hundred and sometimes more than 1000, even in a device in which $g_m$ is much smaller than optimum. This can be explained by the very low drain conductance.

At high $V_D$, the gain drops off as the output conductance increases slightly due to the mild kink effect discussed in section II B. High gain single or multiple stage amplifiers can be designed using suitably biased SGTs as the gain devices.

D. Schottky contact activation energy

The current through the Schottky barrier that makes up the source of the SGT is thermally activated [5], and the drain current increases with temperature.

An application of this is temperature sensing, but there are times when strong temperature dependence is not desirable.

The activation energy of the current has been extracted from measurements (Fig 5b). The figure shows that as the gate field pulls the effective barrier height down, activation energy decreases, which implies that at higher gate bias the current is less dependent on temperature.

III. THE SGT “OFF” STATE

The subthreshold region is described as the range of gate voltages where the barrier is not controlling the current (i.e. the FET has a very low conductance). This region is in fact the lower part of the transfer characteristic of an FET.
identical to the SGT, but which has an ohmic source contact. Therefore, the subthreshold and off-state of the SGT will be governed by the subthreshold characteristics of a regular FET.

A. Effect of bulk doping

The effect of bulk doping is well understood from standard CMOS and thin-film FET technology. By making the semiconductor between the source and the drain more n-type, the threshold becomes more negative, creating a depletion device as opposed to a positive- or zero-threshold enhancement device. Just as in standard FETs, bulk semiconductor doping can be used in SGTs to tune the threshold voltage [6].

The amount of bulk doping also changes the subthreshold slope (Fig. 6). The slope is relatively small (on the order of volts per decade), due to the very thick insulator.

B. Effect of source-drain separation

The gap between the source and the drain of the SGT (d in Fig. 2) can be viewed, broadly, as the channel of a parasitic FET in series with the source barrier.

A well-documented short-channel effect is increased leakage in the subthreshold regime. Our analysis only took into consideration devices with \( d=4 \mu m \) and larger, which makes it difficult to observe any major variation of the current with \( d \) (Fig. 7a).

The off-state of the FET will depend on the channel profile from under the source through to the drain. As a consequence, the barrier modification implant may play a role in the off-state and calls for further investigation.

C. Effect of drain voltage

Fig. 3a shows that a moderately long SGT (\( d=4 \mu m \)) turns off very strongly and can be used as a reliable switch or in logic applications, findings corroborated by Fig. 7a.

IV. FREQUENCY RESPONSE

The SGT’s frequency behaviour has been analyzed in [7]. An important finding is that \( f_T \) is proportional to the average current density through the source, assuming that \( d \) is small enough such that it does not compete with the source barrier in restricting the carrier flow to the drain.

At a given gate bias, one can significantly increase the average current density flowing through the source by using a symmetrical structure such as the one shown in Fig. 1 and Fig. 2. This is due to the fact that the majority of the current is concentrated at the drain end of the source [8], a fact verified in the present study (Fig. 7b). The increase of current that comes with a longer source is not enough to offset the larger capacitance; therefore a longer source will lead to a slower device [7].

The current to each drain was measured independently for the device depicted in Fig. 1. The results are shown in Fig. 8a, for a source length of 2 \( \mu m \). It is interesting to point out that the source-drain separations from the edge of the source window to each of the drains are significantly different (around 4 \( \mu m \) and 16 \( \mu m \) instead of the designed 10 \( \mu m \)) due to misalignment during fabrication. The device shows very little dependence of the drain current on \( d \) [9], but the shorter channel exhibits more kink.

Fig. 8b shows the results of the double-drain measurement on the same device and compares the result with the sum of the currents obtained by connecting each drain independently. We can conclude that by using both drains we are operating the device at very close to double the current and keeping the source area unchanged. This almost doubling of the average current density translates in nearly double the \( f_T \) of the device. With respect to the magnitude of the drain current, this operating mode is roughly equivalent to doubling the channel width in standard FET circuit design.

By using Eq. (6) in [7], we arrive at \( f_T \approx 100 \text{MHz} \) for the polysilicon SGT in Fig. 1, operated in double-drain configuration at \( V_G=-20V \) and \( V_D=3V \).

Moreover, the SGT operates in saturation at \( V_D \approx 2V \) for lower gate bias, ensuring better output impedance at calculated frequencies in the order of tens of MHz, making it ideal for medium-speed signal processing applications in system-on-panel (SoP) architectures.
V. CONCLUSION

The measurements performed on the polysilicon Schottky barrier SGTs confirm the versatility of the SGT concept. The off-state and subthreshold regimes depend strongly on the parasitic FET characteristic. In the on-state, the barrier controls the current and as such limits the values of $g_m$ and $g_d$, leading to very low output conductance and high intrinsic gain in strong saturation. Operation at high drain voltages is possible due to a weak kink effect. The temperature coefficient of the drain current is directly linked to the effective barrier height and diminishes with gate bias.

Frequency behavior is proportional to current density so a short source and double drain architecture are required for optimum performance.

The SGT opens up the possibilities of transferring some analog and mixed signal functionality from the package to the panel in large area electronics. A similar concept has been proven to increase the output impedance and allow better control of short channel effects in deep-sub-micron SOI CMOS [10]. Significant improvements are expected in applications based on poor quality or disordered semiconductors when SGTs are part of analog or mixed signal circuits [11].

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