Diffusion and activation of ultrashallow B implants in silicon on insulator: End-of-range defect dissolution and the buried Si/SiO_2 interface

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The fabrication of preamorphized *p*-type ultrashallow junctions in silicon-on-insulator (SOI) has been investigated. Electrical and structural measurements after annealing show that boron deactivation and transient enhanced diffusion are reduced in SOI compared to bulk wafers. The reduction is strongest when the end-of-range defects of the preamorphizing implant are located deep within the silicon overlayer of the SOI silicon substrate. Results reveal a very substantial increase in the dissolution rate of the end-of-range defect band. A key player in this effect is the buried Si/SiO_2 interface, which acts as an efficient sink for interstitials competing with the silicon surface. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2240257]

Formation of highly activated, ultrashallow, and abrupt profiles is a key requirement for the next generation of complementary metal oxide semiconductor (CMOS) devices, particularly for source-drain extensions.[1] For *p*-type (boron) dopant implants, a promising method of increasing junction abruptness is to use Ge preamorphizing implants (PAI) prior to ultralow energy B implantation. Advantages of this method are a reduction in B channeling and an increase in B electrical activation due to the solid-phase-epitaxial (SPE) regrowth process.[2]

SPE regrowth of the amorphized silicon does not remove interstitial defects located at depths greater than the initial amorphous/crystalline (a/c) interface. Excess interstitial atoms in this region agglomerate into "end-of-range" (EOR) defects situated just below the former a/c interface. During higher temperature annealing these defects undergo a series of transitions from self-interstitial clusters to {113} defects to dislocation loops depending on the initial PAI and subsequent conditions.[3] These defects dissolve during annealing and the silicon self-interstitials so released migrate to nearby sinks such as the silicon surface.[3] Transient enhanced diffusion and B electrical deactivation result from the interstitials that diffuse towards the silicon surface during annealing.[3,4] In the absence of sinks within the silicon, all of the released interstitials diffuse towards the surface. Thus they either end up reacting with B atoms in the implant or migrating unscathed through the B-doped layer to the silicon surface—the former being the more probable event in the case of high-dose B implants.

One possible method to reduce the number of interstitials that migrate to the B implanted region is to provide an efficient alternative sink for the interstitials. In this letter we investigate whether the buried oxide interface of the silicon top layer in silicon on insulator (SOI) may function in this way. This question is of considerable importance as SOI emerges as a candidate technology for future CMOS applications.[5]

Experiments were performed on *n*-type ⟨100⟩ Czochralski silicon wafers with a resistivity of $\sim 10-25\ \Omega$ cm and on SOI wafers with a 145-nm-thick buried oxide and a 55-nm-thick *p*-type Si overlayer. Silicon and Soitec© SOI wafers were implanted with Ge^+ at energies of 8 and 20 keV to a dose of 1×10^{15} Ge cm^{-2}, amorphizing the silicon to depths of ~ 20 and ~ 40 nm, respectively.[6] The crystalline region remaining below the a/c interface was thus approximately 35 nm thick in the 8 keV case and 15 nm thick in the 20 keV case—enough to create a strong difference in the distance between the EOR defects and the buried oxide, without trapping a significant fraction of the implantation damage in the oxide. The implants were performed using an Applied Materials Quantum III high-current implanter, with an implant orientation of 0° tilt and 0° twist. Boron was subsequently implanted at an energy of 500 eV to a dose of 2×10^{15} B cm^{-2}.

To study the electrical (de)activation of the boron, isochronal annealing (60 s) was carried out using a Process Products Corporation 18 Lamp rapid thermal processing annealer over a temperature range of 700–1000 °C. The electrical activity of the B implants was assessed by Hall sheet-resistance (R_s) measurements using an Accent HL5500 machine. Boron atomic profiles were also analyzed in se-

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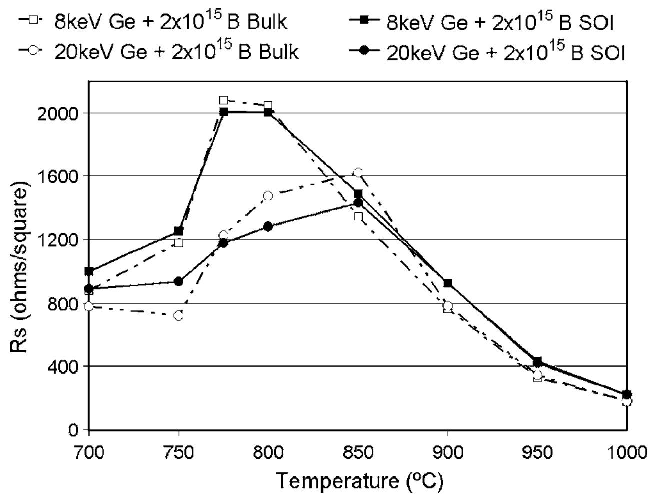

FIG. 1. Van der Pauw resistivity after 60 s isochronal anneals. Dotted lines with open symbols are bulk Si, solid lines with closed symbols are SOI, squares represent 8 keV Ge PAI, and circles represent 20 keV Ge PAI.

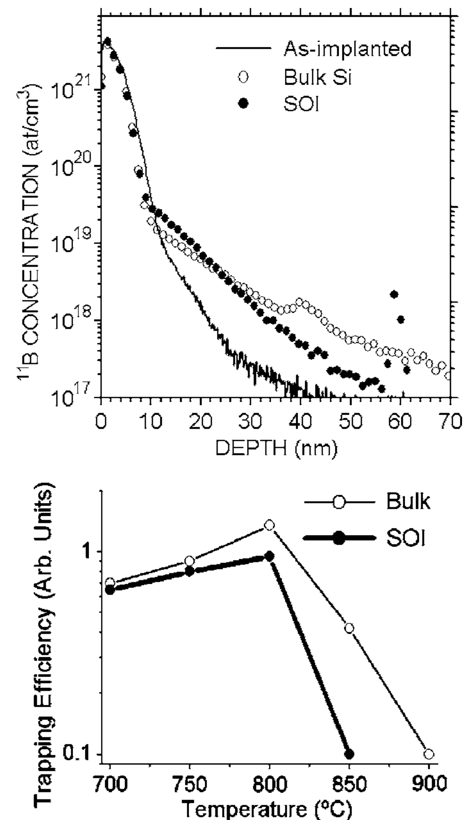

FIG. 2. Boron SIMS profiles (top) for 20 keV Ge samples as implanted and after an 850 °C for 60 s anneal in bulk Si and SOI. Solid line, open, and closed circles represent the as-implanted, bulk, and SOI samples, respectively. The bottom graph is the interstitial trapping efficiency of the EOR band after annealing, inferred from the trapped B peak in the SIMS profiles. Open circles and thick solid line with closed circles represent bulk and SOI, respectively.

lected samples by secondary ion mass spectrometry (SIMS) with a CAMECA Wf SC-Ultra instrument using a 0.5 keV O_2^+ primary beam at 70° incidence angle. Oxygen flooding and stage rotation were used during the analyses in order to avoid ripple formation.[7] The presence and structure of extended defects were investigated by cross-sectional transmission electron microscopy (XTEM) observations in weak beam (WB) mode using a FEI Tecnai F20 electron microscope operating at 200 kV.

Figure 1 shows R_s data in bulk and SOI samples implanted with 8 and 20 keV Ge and annealed for 60 s in the temperature range of 700–1000 °C. This temperature range was chosen in order to reveal the deactivation and reactivation of B in bulk silicon and SOI. The data show the well known reverse annealing effect associated with the deactivation and subsequent reactivation and diffusive broadening of PAI B implants.[3] In the SOI samples, R_s starts out (at 700 °C) about 100 Ω/sq higher than in the bulk samples, possibly as a result of a difference in the two materials. This fits with previously published observations of a lower level of B activation in SOI.[8]

At temperatures above about 750 °C, for both the bulk Si and SOI substrates, R_s rises steeply, as a result of B deactivation, reaching a peak at around 775–800 °C in the 8 keV implanted samples and around 850 °C in the 20 keV implanted samples. The shift in the temperature for peak deactivation is well known and is caused by a reduction in the concentration gradient of interstitials towards the B-doped region when the EOR band is located deeper into the material.[3,4] The rapid onset of deactivation is a result of the rapid Ostwald ripening/dissolution phase of interstitial defects in the EOR defect band, during which a substantial fraction of the interstitials contained in the band are emitted into its surroundings.[3]

Comparing now the deactivation in the SOI and bulk samples in Fig. 1, we see that the change in sheet resistance ΔR_s from the initial 700 °C to the peak is significantly smaller in the SOI cases. In the 8 keV case, where the EOR defects are located in the upper part of the SOI layer, the effect is small: ΔR_s for bulk is $\sim 1200\ \Omega/\text{sq}$ and for SOI $\sim 1000\ \Omega/\text{sq}$, the resultant ΔR_s is 200 Ω/sq less in SOI than in bulk. However, in the 20 keV case, where the EOR defects are within the lower part of the layer, the resultant ΔR_s is over 300 Ω/sq lower in SOI. This is about half the amount of deactivation that occurs in the bulk sample.

These results show that the reduced deactivation of preamorphized B implants in SOI is strongly related to the position of the EOR band within the silicon film. It is our hypothesis that the proximity of the EOR band to the buried Si/SiO_2 interface of the silicon top layer leads to an increased number of interstitials migrating to this interface, thus reducing the number that can reach the shallow B-doped region. If this hypothesis is correct, we would expect to observe a reduction in the density of EOR defects in the 20 keV Ge PAI case, relative to the corresponding bulk case.

SIMS results from the 20 keV Ge PAI as-implanted and annealed samples at 850 °C for 60 s in bulk and SOI are shown in Fig. 2 (top). Several features are clearly evident. First, there is dramatically more transient enhanced tail diffusion in the bulk sample, indicating that a larger number of interstitials have traveled from the EOR band to the surface in bulk Si than in SOI. Second, the *kink* concentration, at which boron diffuses into the wafer from the peak region of the implant, occurs at a significantly higher concentration in SOI (3×10^{18} cm^{-3}) than in bulk (1.5×10^{18} cm^{-3}), indicating a higher level of activation in SOI in agreement with the electrical data in Fig. 1. Third, in the bulk Si there is a peak in the tail of the boron profile, centered on a depth of 40 nm. This corresponds to the position of the EOR defect band determined from Rutherford backscattering.[6] The peak is not

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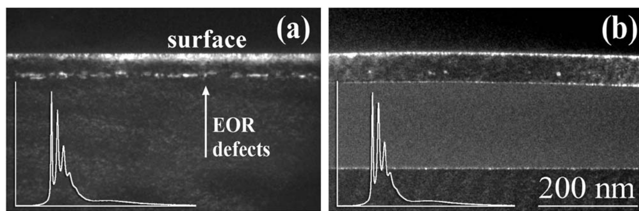

FIG. 3. WB, $(g,2g)$ $g=\langle 400\rangle$, XTEM micrographs of 20 keV Ge Bulk Si (a) and SOI samples (b) annealed at 850 °C for 60 s. Parallel electron energy loss spectrocopy spectra obtained in both cases in the center of the image with the electron beam positioned onto the defect band are superimposed to the corresponding TEM micrographs to witness the close equivalence of the thickness of the TEM samples.

seen for the SOI sample at this temperature (850 °C) although a similar peak—at the same location and somewhat greater in height—appears in both SOI and bulk samples annealed at lower temperatures.

The area of this peak divided by the background B tail concentration is a measure of the B trapping efficiency of the EOR defects. In order to determine this quantity the SIMS profile is interpolated from either side of the peak to obtain a background curve, and then windows are set on each side of the B peak. The background is then subtracted and the resultant net peak area is divided by the background area. The results, obtained as a function of annealing temperature and material type, are shown in Fig. 2 (bottom). The relative uncertainties between data points are comparable to the size of the symbols.

The graph shows that, over the entire temperature range, the 20 keV Ge EOR band has a lower B trapping efficiency in SOI than in the corresponding band in bulk Si. At low temperatures the difference between the materials is small and the trapping efficiency values increase slowly with temperature. It is interesting to speculate, in passing, about the reason for this increase. It occurs during a phase of very rapid Ostwald ripening within the EOR band, and arguably the increase in trapping efficiency reflects the increase in mean lifetime of individual EOR defects, from short-lived defects that quickly release B back to the lattice into slower evolving larger defects. The increase in trapping can be explained if this longer lifetime is needed to bring about "quasi-steady-state" segregation between the lattice and the EOR band.

Most importantly for the discussion in this letter, at temperatures above 800 °C, a clear difference emerges between the amounts of B trapped at the EOR band in the two materials. This coincides with a strong decrease in the overall amount of trapping. These results are a strong indication that (a) the defects have entered the dissolution phase and (b) the defect band is dissolving faster in SOI than in the bulk material. This is despite the fact that, as seen from the viewpoint of the B profile, fewer interstitials have flowed down the concentration gradient from the EOR band to the B-doped region near the surface.

To investigate the defect structure in more detail, bulk and SOI samples annealed at 800 and 850 °C were examined by plan-view and XTEM. Figure 3 shows weak-beam dark-field XTEM micrographs for 20 keV Ge PAI in bulk Si and SOI annealed at 850 °C for 60 s. For this Ge PAI energy the EOR defects lie ~40 nm below the surface as indicated by the arrow in Fig. 3. They are clearly evident in the bulk silicon sample, but in the SOI sample their number has decreased so much that very few defects remain. Plan-view images, which contain the full EOR depth distribution within the TEM sample, show the same trend. Similar results, albeit with a smaller decrease in defect density, occur after the 800 °C anneal. These results confirm our conclusion from the SIMS measurements in Fig. 2 that most of the EOR defects have disappeared during the 850 °C anneal. This is clearly strong evidence in support of our hypothesis that the buried Si/SiO_2 interface of the silicon top layer becomes the predominant interstitial sink when the EOR band is located close to that interface. It may also provide part of the explanation for the reduced interstitial defect content in (non-preamorphized) B-implanted SOI, observed in earlier work.[8]

In conclusion, previously published results showing differences in B activation and transient enhanced diffusion in Soitec© SOI and bulk Si have been directly correlated with SIMS and XTEM data showing an accelerated dissolution of end-of-range defects in the SOI material. B activation, transient enhanced diffusion, and the density of EOR defects all decrease as the EOR band is brought closer to the buried Si/SiO_2 interface of the silicon top layer. We interpret this result as evidence that a substantial portion of the interstitials contained in the EOR defects are absorbed by the buried interface, which acts as an efficient sink for interstitials.

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