Multi-Physics Modeling of RF and Microwave High-Power Transistors

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Abstract—In this paper, we present a multi-physics approach for the simulation of high-power RF and microwave transistors, in which electromagnetic, thermal, and nonlinear transistor models are linked together within a harmonic-balance circuit simulator. This approach is used to analyze a laterally diffused metal-oxide semiconductor (LDMOS) transistor that has a total gate width of 102 mm and operates at 2.14 GHz. The transistor die is placed in a metal-ceramic package, with bondwire arrays connecting the die to the package leads. The effects of three different gate bondpad layouts on the transistor efficiency are studied. Through plots of the spatial distributions of the drain efficiency and the time-domain currents and voltages across the die, we reveal for the first time unique interactions between the electromagnetic effects of the layout and the microwave behaviour of the large-die LDMOS power field-effect transistor (FET).

Index Terms—Global modeling, electrothermal, laterally-diffused metal-oxide-semiconductor (LDMOS) transistor, power field-effect transistor (FET).

I. INTRODUCTION

POWER transistors for wireless infrastructure applications have become increasingly complex over the past two decades, from a single die mounted in the package to sophisticated multi-chip modules, as shown in Fig. 1. Modern high-power devices have total gate widths of several hundred millimeters, achieved by connecting many gate fingers in parallel. The packaged transistors are further complicated by in-package matching networks, comprising several bondwire arrays connecting metal-oxide semiconductor (MOS) capacitors, and other passive circuit elements, to create the matching networks. The 200-W transistor in Fig. 1 contains almost 250 individual bondwires.

Market demands for increased power and efficiency show no sign of abating, and more circuit functions are expected to be integrated within the package. The complexity of the design and construction of high-power microwave transistors continues to increase.

In spite of this increasing complexity of the power transistor device, the compact models that are provided by the device manufacturer are often simplified, reducing the arrays of bond wires and capacitors to a few lumped components, and ignoring distributed effects. This has the benefit of reducing the model to only a few essential ports, simplifying the model extraction and speeding up the circuit simulation [1]–[5]. Apart from a few notable exceptions [1], [6]–[13], the internal operation of the packaged transistor is described only coarsely, and the voltages and currents are only available at a few nodes of interest, effectively obscuring the detailed internal operation of the packaged device. Because of this low number of internal nodes, we are limited in our ability to explain poor performance scaling [7], [14] as well as observed temperature distributions that are dependent on frequency, power, and load termination [6].

Fully coupled multi-physics approaches to modeling transistors, where the governing equations are all solved simultaneously, have been developed by a number of researchers [15]–[17]. While undoubtedly valuable for physically small, high-frequency transistors, the physical scale and consequent computational expense prohibit these approaches for high-power microwave transistors. To overcome the computational expense, ‘weakly-coupled’ approaches have been defined where electromagnetic simulation results (through S-parameters), thermal models (through a thermal impedance matrix), and nonlinear electrothermal transistor models are coupled in the netlist of a circuit simulator. This provides a comprehensive description of the transistor for computationally efficient simulation [6]–[8], [12], [18].

Weakly-coupled approaches for distributed multi-physics modeling are not without their own expense. For example,
schematic representations can become unwieldy, model evaluation can suffer from long simulation time, and data processing can be intense. With the availability of cluster computing, it is possible to simulate circuits containing hundreds of nonlinear transistors, connected to fully distributed matching networks and their interconnections to distributed thermal models. Using this approach, the voltages and currents at all nodes of interest within the packaged device are available, and they can be interrogated to develop a better understanding of its internal operation.

In this paper, we present a multi-physics methodology that combines electromagnetic and thermal simulations with nonlinear electrothermal transistor models in harmonic-balance circuit simulations. In Section II, we present the methods by which we develop the constituent models. We also introduce an experiment where the simulation methodology and models are used to explain performance changes exhibited for three different packaged 102-mm LDMOS transistors where modifications have been made to the layout of the gate bondpad metallization. In Section III, we present a comparison of measured and simulated temperature distributions and large-signal performance. In Section IV and V we present for the first time the visualization of the spatially distributed drain efficiency and time-domain voltages and currents across an electrically large die. As will be shown, these visualization methods provide unique insights into the operation of high-power microwave packaged transistors, which can be very beneficial in the development of future designs. Finally, we conclude the paper in Section VI.

II. Model Development

The packaged LDMOS transistor we examined is illustrated in Fig. 2. This device has 204 individual gates, each having a 500 µm unit gate width. The individual transistors are fed in pairs, with two gates attached to the metallization that connects to the gate bondpad. The individual drains are connected together in a similar way. On the outer edges of the die only one individual transistor gate is connected to the gate bondpad. Of the 204 gates, six pairs are not connected to the gate and drain manifolds. These non-functioning ‘dead’ fingers were relics of a separate experiment where the output power of the transistor could be tailored with only minor metallization changes. As will be seen, the dead fingers contributed significant detail to the temperature distributions along the center of the die.

We used this strategy of defining the power transistor in terms of its constituent electromagnetic, thermal, and nonlinear electronic component parts, to investigate the relationships between the internal behaviors and the terminal performance of the transistor. We have called this strategy a multi-physics modeling methodology, as it couples directly the important physical environments that affect the operation of the device.

We applied the multi-physics modeling methodology to study the effects of changing only the gate bond-pad structure on the device performance. The bondpad width has values of \( w = 0, 80, \) and 160 µm, as illustrated in Fig. 3. For \( w = 160 \) µm, the bondpad has discrete areas for the bondwires to connect, whereas the \( w = 0 \) µm bondpad is uniformly wide. A packaged device for each value of \( w \) was measured in a loadpull test bench over a range of input power from 23 to 37 dBm at 2.14 GHz. Harmonic-balance simulations were performed over a range of source and load impedances to simulate load pull of the packaged transistors.

In the following sub-sections we present the development of each constituent component of the packaged transistor and explain in detail how the multi-physics model is constructed.

A. Transistor Model Development

Our comprehensive model incorporates a measurement-based nonlinear electrothermal transistor model [19], which was extracted from a 5.0-mm on-wafer transistor. A dense pattern of pulsed I-V and S-parameter measurements are taken over the gate-drain voltage space of the transistor, bounded by the maximum drain current, breakdown voltage, and the maximum allowable power dissipation. The manifold structure and the extrinsic network are de-embedded to obtain S-parameter data at the intrinsic model reference planes [20]. After converting to Y-parameters, the LDMOS transistor model current and charge state functions \( (I_d, Q_g, \) and \( Q_d) \) can then be obtained by integration of the small-signal voltage-dependent parameters [14]. This integral formulation for determining the charges ensures a conservative charge formulation, essential for accurate prediction of low-level phase nonlinearity, and for convergence in time-domain simulations [14], [21].
In our model extraction process we obtain charge data indexed by the intrinsic gate and drain voltages. These data are then approximated using artificial neural networks (ANNs), resulting in smooth and infinitely differentiable two-dimensional charge functions that are used directly in the model.

For the drain current, we use the analytical expression (1) from [22] as this expression has been shown to fit accurately the current data in the near-threshold region. This is typically where the LDMOS power transistor is biased for power amplifier applications:

\[
I_d = \frac{\beta V_{gst}^2}{1 + V_{gst}/V_L} \tanh \left( \frac{\alpha V_{gst}}{V_{gst}^{peak}} \right) \left(1 + \lambda V_{ds} \right)
\]  

where \( \beta \) and \( V_L \) are parameters that control the slope in the quadratic region and the transition to the linear region. The parameter \( p \) allows the slope of the transconductance to be modified in the linear region, \( V_{gst} \) is the gate control function, and \( \lambda \) and \( \alpha \) are additional fitting parameters. The current in the sub-threshold region and between the quadratic region is modeled with \( \beta V_{gst}^2 \) where

\[
V_{gst} = V_{ST} \ln \left(1 + e^{(V_{gst} - V_t)/V_{ST}}\right)
\]

and \( V_t \) is the threshold voltage, \( V_{ST} \) controls the abruptness of the ‘turn-on’ characteristic, \( V_{gst} \) is the gate-to-source voltage, and \( V_{ds} \) is the drain-to-source voltage.

The effects of self-heating on the drain current are incorporated using a self-consistent electro-thermal model [23]. A straight-forward method of including the thermal effects on the output current is to use a de-rating function on the drain current expression [14], [24], and it can be expressed as:

\[
I_d = \frac{I_{d0}}{1 + \left(\frac{T}{T_0} - 1\right)} = \frac{I_{d0}}{1 + \frac{R_{th} P_{avg}}{T_0}}
\]

where \( T \) is the temperature, \( I_{d0} \) is the drain current measured at a reference temperature \( T_0 \), \( R_{th} \) is the thermal resistance, \( P_{avg} \) is the average of the dissipated power,

\[
P_{diss}(t) = \frac{(T(t) - T_0)}{R_{th}} + C_{th} \frac{dT}{dt} (T(t) - T_0)
\]

and \( C_{th} \) is the thermal capacitance.

During a harmonic-balance simulation, the power dissipated as computed by the transistor model is passed to the thermal model. The temperature rise is then computed and it is then passed back to the transistor model. This process continues until convergence is reached.

Once the model has been extracted based upon the characterization data obtained from the 5.0-mm transistor, the model is scaled down to the 500 \( \mu \)m unit-gate width. One such model is used to represent each gate finger of the transistor; this is our unitary transistor model.

B. Thermal Model Development

The thermal model for the entire packaged transistor is obtained through finite-element based simulations using ANSYS™. In these simulations, the bottom of the package flange is held at a constant temperature. All other surfaces are assumed to be adiabatic, and for simplicity we neglected the heat-spreading effects of the metallization on the die, as well as convective and radiative cooling.

As reported in [25], we demonstrate the accuracy of our finite-element simulations by comparison with measurements of an LDMOS transistor biased under DC conditions to obtain 4.8 W of dissipated power. In this example, the transistor had a total gate width of 4.8 mm, 600 \( \mu \)m unit-gate width, 30 \( \mu \)m source-drain pitch, is built on an approximately 80 \( \mu \)m thick silicon substrate, and is mounted on top of a 730 \( \mu \)m thick copper carrier. Simulations of the same device were performed and plots of the temperature profiles across the transistor are shown in Fig. 4. The measurements are performed using a QFI InfraScope II™ system outfitted with a 15× magnification lens resulting in a spot size of 1.6 \( \mu \)m.

Using the finite-element method, we generate the thermal resistance matrix \( (R_{th}) \) for the packaged transistor by turning on an incident heat-flux at each finger and then examining the temperature over the whole die, and measuring the temperature at all other fingers. We proceed by exciting each finger in order, until the full thermal resistance matrix is obtained [6]. The temperature for a given finger is defined by averaging the temperature by integration over the finger area. Since the material properties change with temperature, we are careful to perform these single source simulations at temperatures close to those expected in the solution [26]. The thermal resistance matrix for the devices under study has 204 ports, each port being connected to the thermal node of the electro-thermal transistor model, and is written as a Touchstone file for easy inclusion in the circuit simulator.

C. Electromagnetic Simulations

The electromagnetic environment seen by the device plays an important role in its terminal behavior, as will be shown later. This electromagnetic environment includes the on-die metallization of the transistor – the bond pads, the gate and drain metallization structures – and the package and bond-wires that connect the device to the outside world. The metallization structure is simulated using a planar electromagnetic simulator, where the substrate definition has been carefully
determined beforehand using transmission line measurements made over the passive and active regions of the transistor [20]. This simulation has ports where the bond-wires connect to the bonding pads and ports where the gates and drains of each unitary transistor connect to the bonding pads. The resulting S-parameter model has over 200 ports [13]. The package and bond-wires were simulated using a three-dimensional finite element electromagnetic simulation, yielding a multi-port S-parameter model [27]. This model has two ports representing the connections of the complete device to the external circuit, and ports at the ends of each of the gate and drain bond-wires. These two multi-port S-parameter models are connected in cascade and enable us to include the model of the electromagnetic environment in a simple manner.

D. Model Integration - Enabling Multi-physics

Our multi-physics model couples together models of the electromagnetic environment of the transistor, that is the electromagnetic simulations of the package and die metallization, a thermal model of the die, and nonlinear electro-thermal models representing each gate finger in the large LDMOS FET die. The constituent component models are generated independently as described in the preceding subsections.

Following [6], the gate and drain of each of the 204 unitary transistor models is connected to the appropriate ports of S-parameter matrix representing the bondpad metallizations. The thermal resistance matrix is included through a 204-port (one port for each unitary transistor) impedance matrix. The dissipated power from each unitary transistor model is computed and is provided to the thermal model, which in turn provides the temperature increase resulting from the dissipated power and the thermal coupling with the other unitary transistors. Finally, the model for the 102-mm LDMOS die is connected to the ports of the S-parameter matrix representing the package and bonding wires.

A schematic representation of the connections of the various models is shown in Fig. 5. In a harmonic-balance simulation, each finger is simulated individually, and by monitoring the voltage and currents at each node in the circuit we obtain the temperature distribution and we can compute the performance of each unitary transistor. Simulations of the packaged transistor performance for changes in frequency, impedance terminations, or ambient temperatures are readily made. Modifications to the gate bondpad metallizations are incorporated by changing only the appropriate S-parameters file.

III. RESULTS

A. Measurement Setup

The high output power capability of the packaged transistor is achieved by connecting the 204 unitary transistors in parallel. As a result the input and output impedances that need to be presented to the transistor for optimal operation are very low. Obtaining repeatable loadpull measurements on transistors with very low impedance using mechanical tuners based on 50-Ω slotted transmission lines is very difficult. To overcome the limitations posed by mechanical tuners, pre-matching networks are used to transform the tuner impedances to lower values [28]–[30].

In our test-fixture a 10:1 transformer, having a 20 dB return loss or better over the frequency range 1.5–3.5 GHz was placed between the tuner and the packaged transistor. The test-fixture was characterized using thru-line-reflect (TRL) calibrations for loadpull fixtures [29] and the resulting S-parameters were de-embedded from the measurements.

A photograph of the test-fixture is shown in Fig. 6, where the microstrip transformers, bias networks, and the 7mm-to-microstrip connectors are indicated. A thermocouple is mounted through a small hole, approximately 250 µm in diameter, directly beneath the package. The thermocouple monitors the temperature at the backside of the package flange during a loadpull measurement. The temperature rise is computed from the difference between the temperature at the top surface, obtained from IR microscopy, and the temperature measured using the thermocouple.

B. Two-Port Results

The measured and simulated power-added efficiency (PAE) as a function of the input power for the three different gate bondpad layouts \((w = 0, 80, 160 \mu m)\) are shown in Fig. 7. For each measurement and simulation the load is
Fig. 7. A comparison of measured vs. simulated power-added efficiency for the three different gate bondpad metallizations. The measured results are indicated by dashed lines and solid lines indicate the simulated results.

Fig. 8. Infrared images of the die for the bondpads with $w = 0 \, \mu m$ and $w = 160 \, \mu m$. The dashed lines indicate the locations of temperature profiles plotted in Figs. 9 and 10.

coupledly matched for maximum efficiency and the source is matched when the transistor is operating at $P_{1dB}$. The uniform bondpad, $w = 0 \, \mu m$, has approximately 20% higher power-added efficiency than the discrete-like bondpad, $w = 160 \, \mu m$.

The overall shapes of the curves and the maximum efficiency values are well-predicted, although there is a systematic discrepancy between the measured and simulated data. This difference is indicative of a slightly different source match between the measured and simulated results. Although we have used pre-matching transformers, the mechanical tuners are lossy and have finite steps unlike the continuously variable impedances available during a loadpull simulation. The slightly lower peak efficiencies predicted by the models indicate an increased loss present in the model over that of the measured devices. While not shown here, the agreement between other measured and simulated parameters such as gain and output power are broadly similar. The observed differences do not affect the overall predictive performance of this modeling technique in terms of illustrating the important internal behaviors of the device, as will be demonstrated in Section IV.

Fig. 9. Measured vs. simulated temperature profiles for the packaged transistor with uniform gate bondpad $w = 0 \, \mu m$.

Fig. 10. Measured vs. simulated temperature profiles for the packaged transistor with the discrete gate bondpad $w = 160 \, \mu m$.

C. Temperature Distributions

While our proposed simulation methodology reports voltages and currents at all of the internal nodes, it is very difficult to verify directly the distributed behaviour. Passive and electro-optic field probing methods are an attractive option [31]–[33]. Unfortunately, the construction of the transistor and the closely spaced bondwires between the gate and the drain prevent standard probes from being lowered close enough to the transistor for sufficient resolution of the fields.

To verify the distributed behaviour, we turn to infrared microscopy [34] and compare the measured and simulated temperature rise across the center of the die. The packaged transistors were mounted in a test-fixture and excited at approximately 23 dBm input power. The resulting temperature distributions for two of the manifold cases are shown in Fig. 8. The expected broad ‘upside-down U-shape’ temperature distribution is seen for the uniform bondpad device [25], but for the device with the discrete bondpads, an interesting triple-peaked distribution is observed.

The simulations are able to reproduce the same behaviour seen in measurements for both manifolds, as shown in Figs. 9 and 10. The dead finger locations can also be identified as low-temperature regions along the transistor die.
The differences between the simulations and measurements are because the IR measurement reports the peak temperature in the middle of each 500 \( \mu m \) finger. The simulation uses the thermal resistance matrix that was obtained by averaging the temperature over the unit gate width. The averaging effect of the 1.6 \( \mu m \) spot size from the IR camera additionally complicates the comparison. It is important to note that the same thermal model is used to compute the temperature rise in Figs. 9 and 10, where only the gate bondpad layout has been changed.

IV. SPATIALLY DISTRIBUTED PERFORMANCE

In our simulations, the voltages and currents are available for the DC, fundamental, and all the harmonics specified in the circuit simulation, and at every node of interest in the large circuit. Specifically, during the simulation of these packaged transistors (comprising 204 unitary transistors), we collect voltages and currents from the unitary transistors, the edges of the package, the end of the wires, and both sides of the manifolds as illustrated in Fig. 2: this amounts to over a thousand nodes. For a harmonic-balance simulation swept over 15 input powers and including 3 harmonics, this yields a 2 MB text file containing all of the voltages and currents.

With this information, we compute the performance of each unitary transistor and plot the data as a function of transistor position along the width of the bondpad. In Fig. 11, we plot the drain efficiency as a function of the input power and the location of each pair of transistors connected to the drain bondpad. For the device with the uniform gate bondpad, \( w = 0 \mu m \), the efficiency exhibits double peaks with a drop in efficiency at the center of the die. For the device with the discrete bondpad, \( w = 160 \mu m \), the drain efficiency surface is remarkably different, with the center of the die exhibiting negative efficiency, as shown in Fig. 12. The center of the die is not generating power as expected, but is in fact dissipating power.

Using the voltages and currents from the harmonic-balance simulation, we constructed the time-domain waveforms for each pair of unitary transistors that connect to the drain bondpad. Using these waveforms, we plotted the dynamic loadlines, over a range of input powers, for a pair of transistors at the end of the drain bondpad and for another pair in the center, as shown in Fig. 13. Although all unitary transistor models are identical, they are operating dramatically different from one another. This is a consequence of the interactive coupling between the transistor, thermal, and electromagnetic models as described in Section II.

In Figs. 14 and 15, we have generated composite plots of the time-domain voltages, currents, and power loss for all unitary transistors. Each plot contains the time-domain waveform for all unitary transistors across the die. By placing each time-domain waveform next to its neighbor, we have in effect created a time-domain surface wave. The wave shows the spatial and temporal distribution of the voltages and currents. By multiplying the voltages and currents at the drains, we can compute the dissipated power per time cycle for each unitary transistor.

We demonstrate the effects of changing the gate bondpad layout by plotting in 3-D the current waveforms for the two limiting cases, \( w = 0 \) and \( 160 \mu m \), as shown in Figs. 16 and 17. We can incorporate the time-dependence and create animations.
of the output current (or any other time-varying parameter). To the best of the authors’ knowledge, this is the first time that the visualization of the output current as a function of time and position has been created for the entire die.

V. TRANSISTOR PERFORMANCE ANALYSIS

The composite plots that show the gate voltage waveforms in Fig. 14 and 15 are surprisingly very different from one another. The maximum gate voltage for the die with $w = 160 \, \mu\text{m}$ appears at the center of the die much later than it does at the edges. Since this voltage distribution controls the drain current for each individual transistor, the output current from the transistors in the center of the die is also retarded. The maximum gate voltage for the die with $w = 0 \, \mu\text{m}$ excites practically all unitary transistors simultaneously and the drain current distribution is virtually in-phase across the width of the bondpad. Note that the vertical lines showing no current are the locations of the non-functioning fingers, as described in Section II.

From the drain voltage and drain current surfaces we can compute the dissipated power surface. The plots generated in Figs 14 and 15, titled ‘Power Loss,’ were computed by taking the product of the instantaneous drain current and drain voltage waveforms. To show only the loss, the values of positive power generation were set to zero, and these are represented by the black regions. The total area of the black region is dictated by the conduction angle of each unitary transistor and the amount of overlap between the current and voltage waveforms. A transistor exhibiting 100% efficiency would be represented by an entirely black plot.

Computed power-loss plots for each device show dissipation in the center of the die. This is the reason for the drop in the drain efficiency in the center of the die for the device with the uniform bondpad and for the huge drop in efficiency for the device with the discrete bondpad. In fact, for the device with discrete bondpads, the drain voltage and current surfaces are sufficiently aligned that the center of the transistor is operating as an active resistor. The delayed voltage distribution in the center of the large transistor is a result of the distributed electromagnetic effects from the discrete gate bondpads in combination with the bondwires and package, as noted in [7].
In Fig. 18, plots of the voltages applied to gates of the unitary transistors as a function of position along the gate bondpads are shown. For the device with the discrete bondpad, the applied gate voltage in the center of the die is much lower than at the ends. This plot shows the voltages at a single instant in time; it represents a single horizontal line on the plots of gate voltage as a function of time and position as shown in Figs. 14 and 15. If the data traces in Fig. 18 are animated as a function of time, we can show that for the device with the discrete bondpads, the voltage applied to the unitary transistors in the center of the die is considerably delayed, compared with the voltage applied at the edges.

To investigate the origins for the retarded gate voltage due to the discrete bondpad, we used Sonnet’s commercially available em planar electromagnetic simulator and emvu to plot the current distributions. The large-signal currents on the bondpads can be generated once the nonlinear circuit simulation is completed. The voltages obtained from the harmonic-balance simulation, at every node connected to the bondpad, are exported and applied to all of the ports in emvu [35]. The resulting current distribution is the in-situ current seen on the manifold while the packaged transistor is in large-signal operation. In Fig. 19 we plot the current for the fundamental frequency, 2.14 GHz for both manifolds, and each plot is on the same current density scale.

For the packaged transistor with the discrete bondpad, large currents flow in the thin metal connecting the discrete bondpads and along the gates of the unitary transistors as seen in Fig. 19. These transverse currents take time to propagate and the time delay causes the unitary transistors located in the center of the die to conduct later than those at the edges of the die. For the packaged transistor with a uniform gate manifold, minimal transverse currents are observed and there is significantly less voltage variation across the gates of the unitary transistors.

VI. Conclusion

A multi-physics methodology, which combines nonlinear electrothermal transistor models for each individual gate finger with electromagnetic simulations and a thermal model in a nonlinear circuit simulator, has been presented. This methodology was applied to study the effects of different gate bondpad layouts on the operation of a physically large, high-power LDMOS transistors. The shape of gate bondpads was shown to have a large influence on the transistor performance. In the worst case, individual transistors at the center of the die were dissipating rather than generating power. Using distributed multi-physics simulations in this manner, we have produced a ‘computational microscope’ that enables access to all of the voltages and currents throughout the entire structure, revealing behaviours that would have otherwise been hidden using conventional modeling approaches. The insights gained using these techniques will be very useful for future designs.

VII. Acknowledgments

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References

Fig. 19. Visualization of the fundamental component of current vs. position within the gate bondpads for the \( w = 0 \) µm and \( w = 160 \) µm cases.


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Travis Barbieri joined Freescale Semiconductor Inc. in 2005 as an RF Technician. He has provided technical support for several projects dealing with the development and modeling of high power LDMOS devices. His professional interests include expanding his knowledge of microwave measurements and modeling techniques. He is currently pursuing a degree in electrical engineering at Arizona State University.
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