Current percolation in ultrathin channel nanocrystalline silicon transistors

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The ultrathin channel nanocrystalline silicon transistor shows greatly improved switching performance and has demonstrated its candidacy for low power applications. In this work, by careful observation of the current-voltage and threshold voltage characteristics, we find that current percolation occurs when the channel is thinner than 3.0 nm due to strong quantum confinement induced large potential variations over the channel. We show that the device channel width must be at least 0.3 μm to avoid percolative "pinch off" for 0.5 μm channel length devices. Theoretical analysis performed on the devices agrees well with the experimental data and provides important guidelines to model and optimize the devices for circuit design. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2965807]

There has been significant interest in silicon nanostructures for electronics, photovoltaic, and optoelectronic applications, including zero-dimensional silicon nanocrystallites, one-dimensional (1D) quantum wires, and two-dimensional (2D) thin layers.[1–3] All these structures are designed to use the quantum confinement effect to enhance the device's performance. To design transistors for integrated electronics, however, the ideal structure must also be compatible with conventional silicon device processing. The 2D silicon layers appear to be the best choice for current fabrication techniques due to the planar geometry that is utilized in current complementary metal oxide semiconductor technology. Recently, by controlling the deposition (chemical vapor deposition) process at a very low deposition rate, ultrathin (<5 nm) flat nanocrystalline silicon (nc-Si) layers were achieved and applied as the channel for transistors in low power applications.[4] It is proven that using such an ultrathin channel effectively improves the switching performance of thin-film transistors in nc-Si.[5] When the channel becomes thinner, the OFF-state leakage current I_{OFF} decreases significantly, which is attributed to the stronger quantum confinement effect along the channel thickness direction. The subthreshold swing (S) also becomes steeper because the effect of gate voltage on the channel surface potential increases. Low I_{OFF} and steep S result in a high I_{ON}/I_{OFF} ratio.[5] The high I_{ON}/I_{OFF} ratio will enable the transistors to be used to design integrated electronics on arbitrary substrates for the applications, where low power and fast access times are demanded.

However, when the nc-Si layer becomes very thin, even the smallest thickness variation can result in highly random potential fluctuations due to the strong quantum confinement effect along the channel thickness direction,[6] and charge traps at grain boundaries (GBs) will also deplete the nc-Si grains of free carriers.[7] These will make the carrier transport from the source to the drain through the device channel become much more complicated, and result in electrical characteristics that may not be described by conventional field-effect transistor (FET) models. In the present study, current percolation is found in the nc-Si transistors with a channel thickness below 3.0 nm, and it is shown that for these devices, the device channel width must contain at least 0.3 μm to avoid percolative "pinch off" by the channel boundaries.

The devices to be studied here are composed of a thin layer of undoped nc-Si, varying from 3.0 to 2.0 nm, a gate insulator with an effective oxide thickness of 22.5 nm, and a 100 nm thick layer of phosphorous-doped poly-Si as the gate electrode, as shown in Figs. 1(a) and 1(b). The channel length is fixed as 0.5 μm. The average grain size of the channel is about 10 nm, as observed from the planar transmission electron microscopy images. Details of the fabrica-

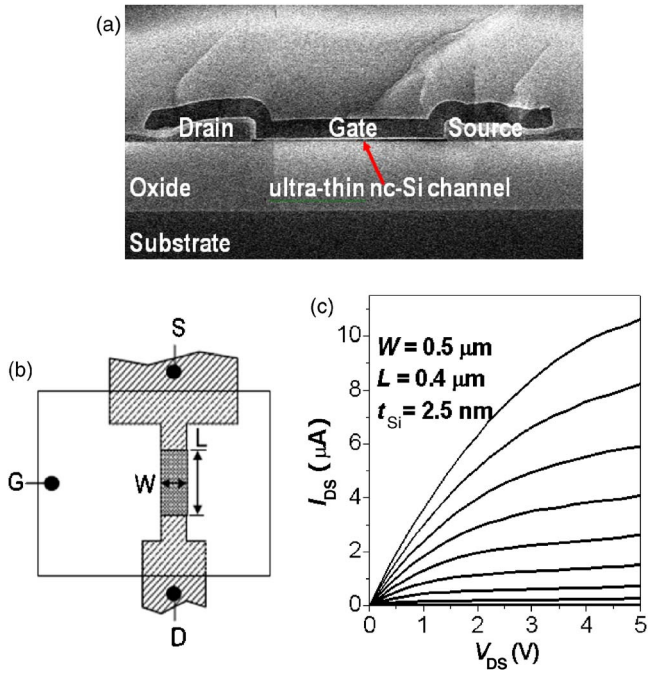

FIG. 1. (Color online) (a) The cross-sectional scanning electron microscopy micrograph of the ultrathin channel nanocrystalline silicon (nc-Si) transistors (the minimum channel thickness is 2.0 nm). (b) Top view of the layout design for the nc-Si transistors. (c) Room temperature I_{DS}-V_{DS} characteristics for the ultrathin channel nc-Si transistors of 2.5 nm thick channel, 0.5 μm channel length, and 0.4 μm channel width. V_{GS} varies from 0 to 5.0 V with a step of 0.5 V.

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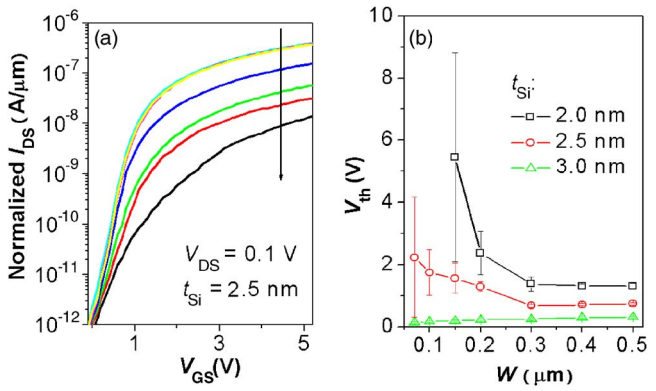

FIG. 2. (Color online) (a) I_{DS}-V_{GS} characteristics at a drain bias of 0.1 V for 2.5 nm thick channel devices of different channel widths, showing the channel width dependence. The displayed current values were normalized for different channel widths, which vary as 0.5, 0.4, 0.3, 0.2, 0.15, 0.1, and 0.07 μm in the direction indicated by the arrow. (b) Dependence of V_{th} on the channel width for different channel thickness devices. V_{th} was defined as the value of V_{GS} at an I_{DS} of 1 nA/μm with the drain bias of 0.1 V. We have measured 100 devices for every dimension.

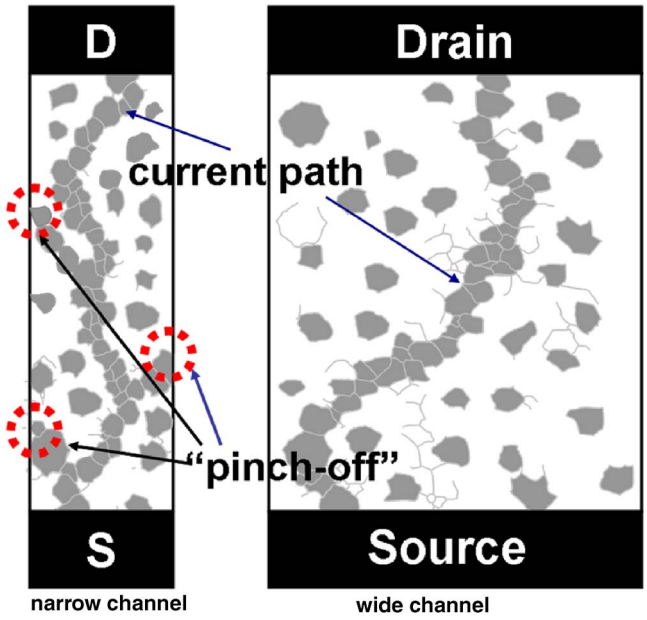

FIG. 3. (Color online) For the narrow channel, the formation of a current percolation path is limited by the pinch-off at the boundaries, and thus a higher fraction of the conductive grains (f) in the narrow channel is required to achieve current percolation.

tion process can be referred to Ref. 4. The uniformity and the reproducibility of the ultrathin nc-Si layers are achieved by controlling the deposition condition carefully. The output characteristics (I_{DS}-V_{DS}) for a 2.5 nm thick channel transistor of 0.5 μm channel length and 0.4 μm channel width are shown in Fig. 1(c), indicating a typical FET behavior.

However, as shown in Fig. 2(a), where the normalized I_{DS}-V_{GS} characteristics measured at V_{DS}=0.1 V for different channel width transistors of a 2.5 nm thick channel are displayed, the current degrades greatly when the channel width (W) is below 0.3 μm.

Figure 2(b) illustrates the extracted threshold voltage V_{th} as functions of the channel width as the channel thickness varies as 2.0, 2.5, and 3.0 nm. The V_{th} was defined as the value of the V_{gs} at a drain current value of 1 nA/μm. We find large V_{th} shifts and also significant increase in V_{th} dispersion in devices of 2.0 and 2.5 nm channel thickness, when the channel width is smaller than 0.3 μm. While for the devices with 3.0 nm thick channel, the measured V_{th} values have little dependence on the channel width. A clear increase in V_{th} was also observed for single crystalline silicon MOSFETs of channel widths narrower than 10 nm due to the quantum confinement in the channel width direction.[8] However, here, the channel width is much larger than the scale at which the quantum confinement may occur. The significantly increased V_{th} and its dispersion for narrower channel devices of 2.0 and 2.5 nm thick channels are attributed to other mechanisms.

In nc-Si films, the defect levels at GBs behave as traps for free carriers. The charging of the traps at the GBs implies a removal of free charges from the grains, thereby, creating potential-energy barriers.[7] Due to the small free concentration of carriers (with the intrinsic carrier concentration of Si) and also the small grain sizes, the crystalline regions within the intrinsic nc-Si grains will be fully depleted, inducing variations of the conduction band edge (E_{C0}) from that in single crystal material.[9] In general, the trapping effects of the GB are related to its structure which is determined by a mutual misorientation of the neighboring crystalline grains.[7] When the film becomes very thin, the quantum confinement also becomes significant and has a strong dependence on the thickness, causing additional changes in E_{C0}, which can be approximated as[6]

$$\Delta E_{C0} = \frac{h^2}{8m_e^* t_{Si}^2}, \tag{1}$$

where m_e^* is the quantization effective mass of an electron, h is the Planck constant, and t_{Si} is the channel thickness.

These factors make E_{C0} very sensitive to the local physical properties of the film (film thickness, crystalline orientation, grain size, etc.), thus inducing large energy potential fluctuations over the whole channel. Current conduction in such an ultrathin nc-Si channel can thus be formalized as a percolation problem in a 2D rectangular lattice system.[10] The lattice is randomly filled with individual sites (grains) and GBs are randomly formed between adjacent sites as bonds. As the gate voltage V_{GS} is increased, localized pockets of electrons will form in the grains with lowest E_{C0}. The fraction of these conductive grains in the channel is denoted as f, which is a function of V_{GS}. As more and more such conductive grains are generated during the increase in gate potential, f reaches a certain value and there is possibly an infinite cluster of conductive grains bridging the source and drain for current conduction. The bond (GB) is assigned as conducting when both neighboring grains are conducting. Then, for very thin channels, actual current path from source to drain under a low gate bias condition is not the whole film but a naturally formed quasi-1D path with only low energy potential parts in a film. Intuitively, for narrow channel devices, the formation of the current path is limited by the boundaries of the channel, and a higher V_{GS} for a higher f is required to achieve current percolation, as shown in Fig. 3. For a more quantitative analysis, that average conductivity of a very thin nc-Si channel with grain size d, length L, and width W can be approximated as[11]

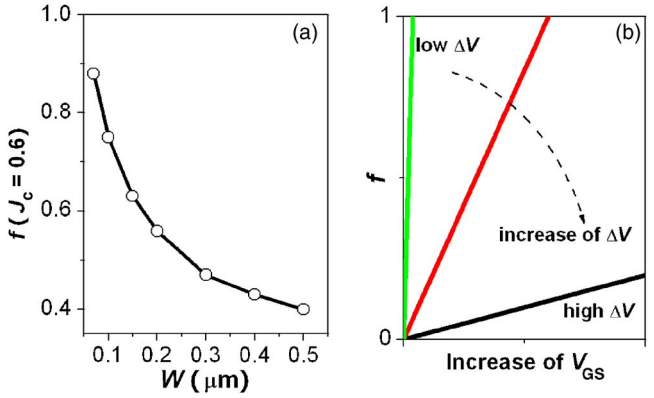

FIG. 4. (Color online) (a) The calculated f (the fraction of the conductive grains in the channel) to achieve a normalized conductivity J_c=0.6 as a function of channel width (W), showing the narrow channel requires a higher f to achieve equally conductive. (b) Illustration to qualitatively describe the relationship between the f and the gate voltage (V_{GS}) with different potential fluctuations (ΔV) over the channel film.

$$J_c \sim \exp\left\{\frac{L}{\xi}\ln[1-(1-d/\xi)^{W/d}]\right\}, \tag{2}$$

here, ξ is a correlation length,

$$\xi \propto d(f-f_c)^{-\upsilon}, \tag{3}$$

where f_c is the percolation threshold and ν is a critical exponent. The values of f_c and ν are 0.33 and 1.33, respectively, in the case of percolation on planar random lattices.[12]

Based on Eqs. (2) and (3), the f value to achieve the same normalized conductivity J_c=0.6 is calculated for different W, as shown in Fig. 4(a). It can be seen that, to achieve a certain current conductivity, for narrower channel devices, a higher f is required. Since f is a function of V_{GS}, it means that a higher V_{GS} is required for the narrow channel to be equally conductive. Therefore, as shown in Fig. 2(b), there is an increase in V_{th} for the 2.0 and 2.5 nm thick channel devices when the channel width is narrower than 0.3 μm. In narrow channel devices, the presence of the channel boundary pinch-off causes various f values being required for different devices to achieve similar conductivity, thus large dispersion of V_{th} in the narrow channel devices is expected as well as observed.

In a thicker channel device, the quantum confinement becomes weaker, and the resultant smaller increase in E_{C0} brings lower V_{th}, as shown in Fig. 2(b). The film is also less rough than the thinner ones. As a result, the potential fluctuations ΔV can decrease greatly since ΔV is given by

$$\Delta V = \frac{\partial \Delta E_{C0}}{\partial d}\delta \propto \frac{1}{d^3}\delta, \tag{4}$$

where the roughness is characterized by the height δ and the lateral correlation length of the Gaussian fluctuations.[6] With a smaller ΔV, there will be a much quicker increase in f with the increase in V_{GS} for current percolation to occur, as illustrated in Fig. 4(b). So the difference between the V_{GS} values of the narrow channel and the wide channel devices to achieve the required f for equal channel conductivity become less. This is the reason why the V_{th} of the 2.5 nm thick channel devices has a much smaller channel width dependence than that of 2.0 nm thick channel devices, as illustrated in Fig. 2(b). For the 3.0 nm thick channel devices, ΔV is small enough, and the V_{GS} to achieve the required f for different channel width transistors are almost identical, and thus V_{th} has little dependence on W.

As a conclusion, for the nc-Si transistors, when the channel is thinner than 3.0 nm, current percolation occurs due to large potential variations over the channel film. It is observed that with the channel length of 0.5 μm, the device channel width must contain at least 0.3 μm to avoid percolative pinch off. The theoretical analysis agrees with the experimental results very well, and gives indications for modelling and optimization of the devices for circuit design. According to the analysis, it can be expected as the channel length decreases, the minimum channel width to avoid percolative pinch off will become smaller. Both channel length and width dependence of the threshold voltage dispersion will need to be investigated to fully model the device operation. Statistical modeling of the device characteristics, as a function of the device geometries, film thickness, average grain size, and size distribution, is another important issue to be solved for practical applications of the devices in large scale system design.

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