A Novel Monolithic Micropower Amplifier Using a SiGe n-MODFET Device

A.Vilches, and K. Fobelets.

Optical and Semiconductor Devices, Department of Electrical and Electronic Engineering, Imperial College London, Exhibition Road, London SW7 2BT.

K. Michelakis, S. Despotopoulos, and C. Papavassiliou.

Analogue Electronics, Department of Electrical and Electronic Engineering, Imperial College London, Exhibition Road, London SW7 2BT.

T. Hackbarth, and U. König

Daimler Chrysler Research Center, D-89081 Ulm, Germany

Contact email: a.vilches@imperial.ac.uk

Abstract

A micropower-relevant model is extracted from the DC characteristics of an n-type buried channel Si/SiGe HMODFET (Hetero-junction Modulation Doped FET). This model is then used to design a novel monolithic SiGe single-stage class-A power amplifier for micropower operation (sub 500μW). The amplifier is fabricated and measured data of the power-gain versus operating power are presented here for the first time.

Introduction

Research on SiGe HMODFETs is motivated by their compatibility with existing CMOS fabrication technology and the promise of superior high-frequency transistor performance when compared to conventional MOSFETs [1]. SiGe HMODFETs contain a buried channel in high mobility strained Si, separated from the gate by further semiconductor layers [2]. The strain in the buried channel and the removal of the carriers from the SiO_2 interface, results in that, for a given gate bias, the transconductance (g_m) increases more rapidly than is the case for Si MOSFETs and is always higher than in conventional FETs [3]. The extra boost in g_m at low bias levels warrants the use of these devices in micropower applications where battery life is of prime importance [4]. In this paper we report on a fabricated, SiGe single-stage class-A amplifier, for operation at micropower levels, consisting of a monolithically integrated 0.5μm x 100μm n-MODFET and resistive 100Ω load.

Device Structure and Characteristics

The n-MODFET structure (see figure 1) was grown by molecular beam epitaxy (MBE) on a 40% Ge-graded virtual substrate (VS), which was prepared by low energy plasma enhanced chemical vapour deposition (LEPECVD).

A standard fabrication technique for n-type SiGe MODFETs was applied, which included dry MESA etching for electrical isolation of the epitaxial active areas and deposited field oxide for electrical isolation of the implanted areas. The ohmic contacts' implant was P activated by low temperature rapid thermal annealing (RTA). The ohmic contacts consist of Ti/Pt/Au and this metal also serves for the circuit interconnections. The Schottky gates were defined by e-beam lithography and lift-off and consisted of Pt/Au. The minimum gate length available on-wafer was 0.1 microns and a number of test devices and structures were available for characterisation including Hall patterns, which were all measured at 300 K. The sheet resistivity of the structure was 811 Ω/square, the sheet electron density was 4.5×10^{12} cm^{-2} and the corresponding mobility was 1700 cm^2/Vs (300 K).

Device Modelling

Measured DC current-voltage data was entered into MWOFFICE (Electronic CAD package) [5] and the software was used to successfully fit a Curtice [6] type equivalent circuit model, figure 2, for operation on micropower supply in the V_{DS} range of 0V to 0.5V and V_{GS} range of –0.5V to 0V, having established that the device's threshold voltage is –0.5V.

Amplifier Design

The single-stage amplifier was simulated in MWOFFICE using the extracted micropower model with an input power level of –40dBm. The FET is worked into a resistive 100Ω load and no microwave matching components were used in the initial design as the circuit's bandwidth was expected to be low at the power operation levels targeted. The circuit's input and output are terminated with standard 50Ω ports and the simulation showed that a maximum transducer power gain of 30 dB, G_{MAX} (see eq. (1)), was achievable with a bias of V_{GS} = -0.2V and V_{DS} = 0.3V (sub 500μW total power supplied).

$$G_{Max} = \frac{|S_{21}|}{|S_{12}|}\left(k - \sqrt{k^2 - 1}\right) \qquad -1$$

where $$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + \Delta^2}{2|S_{12}||S_{21}|} \qquad -2$$

and $$\Delta = S_{11}S_{22} - S_{12}S_{21} \qquad -3$$

Amplifier Characterisation

A HP5783D Network Analyser was used to probe, bias and measure the fabricated monolithic amplifier, a picture of which is given in figure 3. Two-port s-parameters were recorded and converted, using MWOFFICE, into G_{MAX} versus frequency graphs for each power supply level investigated and a chart of measured power gain at the half-power bandwidth frequency vs. power supplied is shown in figure 4. The graph illustrates that for a supplied power of only 26μW, a power gain of ~15 dB is available with an operating bandwidth of 38 MHz.

Conclusion

A SiGe n-MODFET device has been fabricated, measured and a micropower-relevant model extracted for use in the design of a monolithic single-stage class-A amplifier. The SiGe amplifier was fabricated and a graph of measured maximum power gain vs. power supplied has been presented here for the first time. A minimum operating power of 26 μW resulted in a measured power gain of ~15 dB with a corner frequency of 38 MHz.

Acknowledgment

Financial support from EPSRC award N. GR/N65844/01 is gratefully acknowledged.

References

1. O'Neill, A. G., and Antoniadis, D. A.: "Investigation of Si/SiGe-Based FET Geometries for High Frequency Performance by Computer Simulation", IEEE Trans. Electron Devices, Jan. 1997, Vol. 44, pp. 80-88
2. Gluck, M., Hackbarth, T., König, U., Haas, A., Hock, G., Kohn, E.: "High fmax n-type Si/SiGe MODFETs". Electronics Letters, Volume: 33 Issue: 4 , 3 Feb 1997 Page(s): 335 –337
3. Papavassiliou C., Fobelets K., Toumazou C. "SiGe hetero-FET potential for micro-power applications" invited paper, IEICE Trans. Electron, E00-A(2000)
4. Lenk J.D., "Simplifier design of micropower and battery circuits", Butterworth-Heinemann, December 1995, ISBN 0750695102
5. http://www.mwoffice.com/
6. Curtice, W. R., "A Nonlinear GaAs FET Model for Use in the Design of Output Circuits for Power Amplifiers," IEEE Trans. Microwave Theory Tech., Vol. MTT-33, 1983, p.1383.

Figure captions:

Fig. 1 : MODFET Device Structure

Fig. 2 : Measured (□) vs. Modelled (Δ) Device Output Characteristics for V_{GS} = -0.5V to 0V.

Fig. 3: Micrograph of Fabricated SiGe Amplifier on-wafer

Fig. 4: Measured Amplifier Response for Micropower Operation

3.5 nm Si cap
6 nm SiGe cap 40%
5 nm n^+-SiGe 40% : Sb supply
3.5 nm SiGe 40% spacer
9 nm Si channel
4 nm SiGe 40% spacer
5 nm n-SiGe 40% :Sb supply
150 nm SiGe 40%
LEPECVD 40% 5 μm
Silicon substrate: p- > **1000** Ωcm Total MBE Epi: 186 nm

Figure 1

A Novel SiGe Micropower Amplifier Using an n-MODFET Device
A.Vilches, et al.

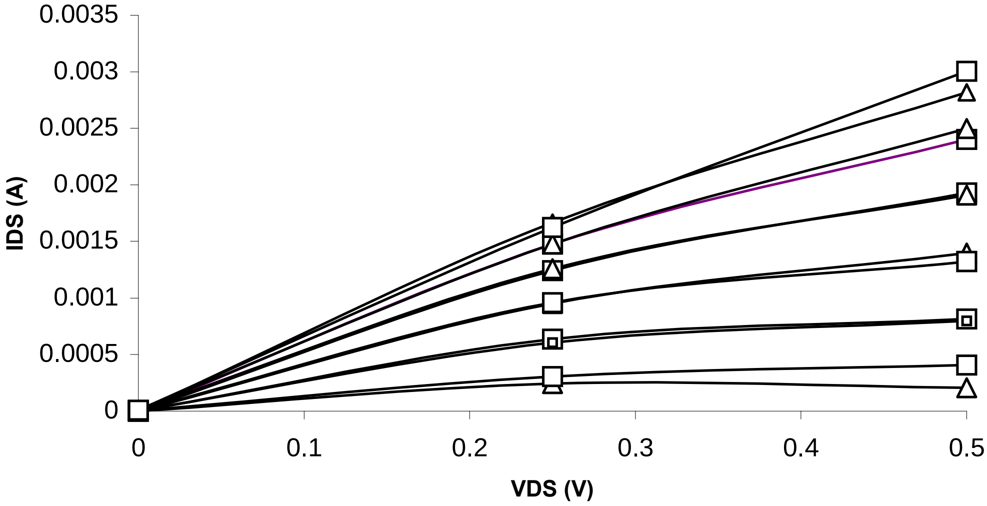
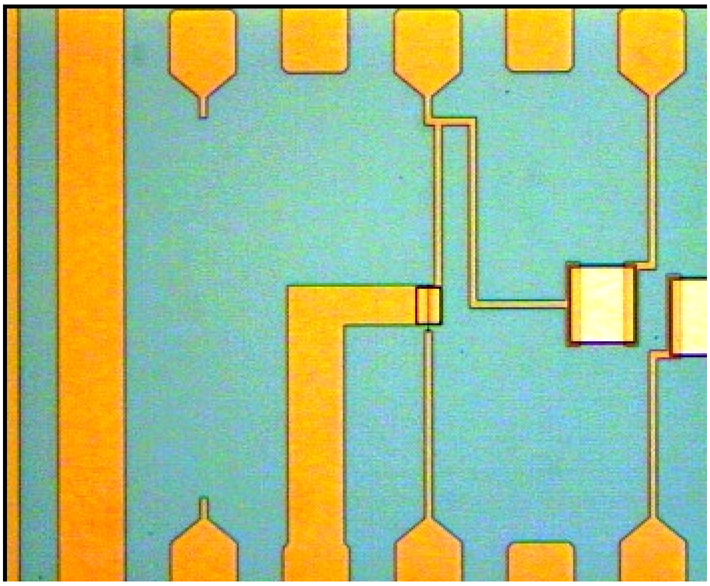


Figure 2

A Novel SiGe Micropower Amplifier Using an n-MODFET Device

A.Vilches, et al.

Figure 3
A Novel SiGe Micropower Amplifier Using an n-MODFET Device
A.Vilches, et al.



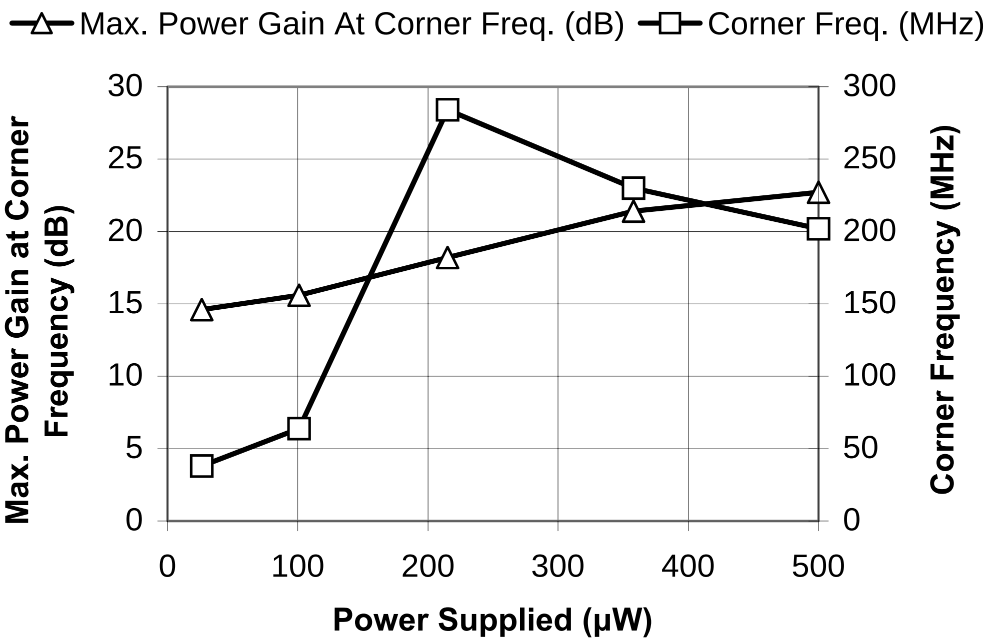


Figure 4
A Novel SiGe Micropower Amplifier Using an n-MODFET Device
A.Vilches, et al.