The authors examine the electrical properties of ultrathin MgO barriers grown on (001) InAs epilayers and the dependence on InAs surface pretreatment and growth conditions. Pretreatment improves the yield of tunnel junctions and changes the roughness of the interface between oxide and semiconductor. Electrical characterization confirms that tunnel barriers with appropriate values of interface resistance for efficient spin injection/detection have been achieved. Using the Rowell criteria and various tunneling models, the authors show that single step tunneling occurs above 150 K. Incorporating a thermal smearing model suggests that tunneling is the dominant transport process down to 10 K. © 2007 American Institute of Physics. [DOI: 10.1063/1.2784933]
greater \(\varphi\). Secondly, the routinely employed expressions for the BDR and Stratton models use the free electron mass and do not take into account the effective electron mass in the barrier material or conductor.\(^{20}\) In a Co/MgO/InAs structure \(m^*\) varies by almost two orders of magnitude as \(m^*/m_e=0.026\) in InAs.\(^{21}\)

To obtain significant spin injection and detection, the interface resistance \(r_b\) needs at least to satisfy the condition \(r_b=r_N=\rho_N l_d\), where \(\rho_N\) is the resistivity and \(l_d\) the spin diffusion length of the nonmagnetic material.\(^{2,6}\) The spin diffusion length in the nondegenerate limit can be defined as \(l_d=(k_B T\mu r_d/2e)^{1/2}\), where \(\mu\) is the mobility and \(r_d\) is the spin lifetime of the carriers. From a knowledge of the spin lifetime in bulk InAs,\(^{22}\) we can estimate the value of \(r_b=10^{-9}–10^{-10}\ \Omega\ m^2\) at room temperature. A direct interface between gold and InAs yields\(^{23}\) an interface resistance of \(\sim 10^{-12}\ \Omega\ m^2\) and this leaves scope for growing a barrier material on the InAs to reach the desired \(r_b\).

TABLE I. Summary of sample properties. \(T_s\) is the growth temperature and \(t\) is the oxide thickness determined by TEM with ±0.3 nm error.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Pretreatment</th>
<th>(T_s) (°C)</th>
<th>(t) (nm)</th>
<th>(r_b) ((\Omega\ m^2))</th>
<th>Tunneling</th>
</tr>
</thead>
<tbody>
<tr>
<td>21472-1</td>
<td>Degreased</td>
<td>100</td>
<td>1.8</td>
<td>(7.54 \times 10^{-10})</td>
<td>no</td>
</tr>
<tr>
<td>21487-1</td>
<td>Degreased</td>
<td>200</td>
<td>1.8</td>
<td>(1.13 \times 10^{-10})</td>
<td>no</td>
</tr>
<tr>
<td>21527-1</td>
<td>Degreased</td>
<td>200</td>
<td>1.8</td>
<td>(2.4 \times 10^{-9})</td>
<td>yes</td>
</tr>
<tr>
<td>21358-2</td>
<td>Single etch</td>
<td>200</td>
<td>1.8</td>
<td>(3.5 \times 10^{-9})</td>
<td>yes</td>
</tr>
<tr>
<td>21424</td>
<td>Single etch</td>
<td>200</td>
<td>1.2</td>
<td>(1.75 \times 10^{-9})</td>
<td>yes</td>
</tr>
<tr>
<td>21472-2</td>
<td>Double etch</td>
<td>100</td>
<td>1.8</td>
<td>(2.47 \times 10^{-9})</td>
<td>yes</td>
</tr>
</tbody>
</table>

The barrier conductance spectra from room temperature down to 10 K showing parabolicity at high temperatures and the emergence of the ZBA at low temperatures. The solid line is a fit to the BDR model at 300 K. The right inset shows the temperature dependence of the zero bias conductance for several junctions on the same wafer. The solid line is a fit to the Stratton model above 200 K. The dashed lines in the main group show the effect of thermally smearing the 10 K data allowing for a small offset in \(G\) and similarly a shift in \(V\) [for \(100\ \text{K (200 K)}\) \(G_{\text{eff}}=6 \times 10^{-4}(1.1 \times 10^{-1})\ \Omega^{-1}\) and \(V_{\text{eff}}=6 (12)\ \text{mV}\). The left inset shows the smearing temperature vs actual temperature.

Higher \(T\) data, as shown by the dashed lines in Fig. 1. The left inset of Fig. 1 shows a \(T^*\) to \(T\) ratio of approximately 2 (the previous study finds a ratio of 1.6–2.0).

The absolute barrier parameters extracted from the fitting can only be treated as a guide to barrier properties due to the uncertainty in \(m^*\). We fix the effective mass to \(m^*/m_e=0.1\) as this gives reasonable values for the fitting parameters. Thus, despite the uncertainty about their absolute values, we can use the fitting parameters as a guide to compare electrical variability between junctions of the same materials.

A spread in \(G_0\) (at fixed \(T\)) between different junctions on each wafer is observed because of a variation in thickness (first Rowell criterion). Figure 2 shows the relationship between \(G_0\) at 300 K and the thickness \(d\), as determined by fitting to the BDR model. The relationship is indeed close to

![FIG. 1.](https://example.com/fig1.png)

![FIG. 2.](https://example.com/fig2.png)
exponential within each wafer except for the wafer with the thinnest barrier. Interestingly, we find a discontinuity in the \(G_0(d)\) dependence between the wafers which we show can be attributed to the influence of barrier roughness. Perhaps not surprisingly, the mean thickness determined by TEM does not reflect the thickness relevant for electrical transport as indicated by the variation across the samples.

Figure 3 compares the barrier thickness \(d\) and height \(\varphi\) as determined by the BDR model for four different growth conditions and pretreatments. The trend of decreasing thickness and increasing barrier height seen across this series of samples corresponds to an increase in interface roughness as determined by TEM. The influence of roughness on the effective parameter values extracted using the BDR model has been discussed by Miller et al. Adopting this model and simulating roughness by assuming that the net conductance is the sum of parallel conductance channels with a Gaussian distribution of thicknesses with standard deviation \(\sigma\). We take the sample series with the sharpest interface, the double etched sample, and use the mean extracted thickness of this series as a reference point. As shown in Fig. 3, we find that an increase in roughness of \(\sigma=1\ \text{Å} (10\%) \text{ and } \sigma=2\ \text{Å} (20\%)\) can account for the apparent decrease in \(d\) and increase in \(\varphi\) for the degreased and single etched samples, respectively. The high roughness of the single etched samples is reinforced by conducting AFM which shows the presence of high current, pinholelike features.12

In summary, we have grown Co/\(\sim 1.3\) \text{ nm MgO/InAs trilayer structures with contact resistance values that are suitable for efficient spin injection/detection. The BDR and Stratton models have been used to determine whether tunneling dominates the conductance. A thermal smearing model gives further confirmation that tunneling dominates at all temperatures. Once the influence of roughness is taken into account, we find that the electrical properties of the barrier are relatively insensitive to surface pretreatment and growth temperature.

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