

Introducing Carrier Localisation in Total Internal Reflection Optical Switches to Restrict Carrier Diffusion in the Guiding Layer

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Abstract

Previous total internal reflection based switches have suffered from the diffusion of carriers in the guiding layer leading to inefficient reflection and carrier injection. In our proposed device this problem is overcome by using a SiO₂ barrier.

Introduction

Optical switches based upon carrier injection and total internal reflection have been previously reported in both silicon¹⁻⁵ and other semiconductor materials⁶⁻⁹. They are advantageous over other switching topologies as they can be made to be wavelength insensitive. The importance of having a precise controllable reflection interface in this type of switch is widely acknowledged^{2-5,9} and problems caused by the high injection currents required for switching has been mentioned⁶.

Attempts have been made to restrict the carriers to certain areas of the device to create a precise controllable reflection interface and/or to reduce the required injection current by O⁺ implantation⁶, using a double-heterojunction layout⁷ or by selective Zn diffusion⁸. Whilst these devices have all reported an improved performance none of the designs show any method of horizontal carrier restriction in the guiding layer itself and therefore carriers are still able to diffuse through the guiding layer freely, compromising device operation.

The use of a thin SiO₂ layer to form an insulating layer in SOI based photonics has been demonstrated in recent years to form both a MOS capacitor structure in a phase modulator¹⁰ and a carrier restrictive boundary in other phase shift based devices¹¹.

In this paper the use of a SiO₂ carrier restrictive barrier in a total internal reflection based switch is proposed to both set up a precise reflection interface and improve the carrier injection efficiency. All optical modelling in this paper is carried out for TE polarised light.

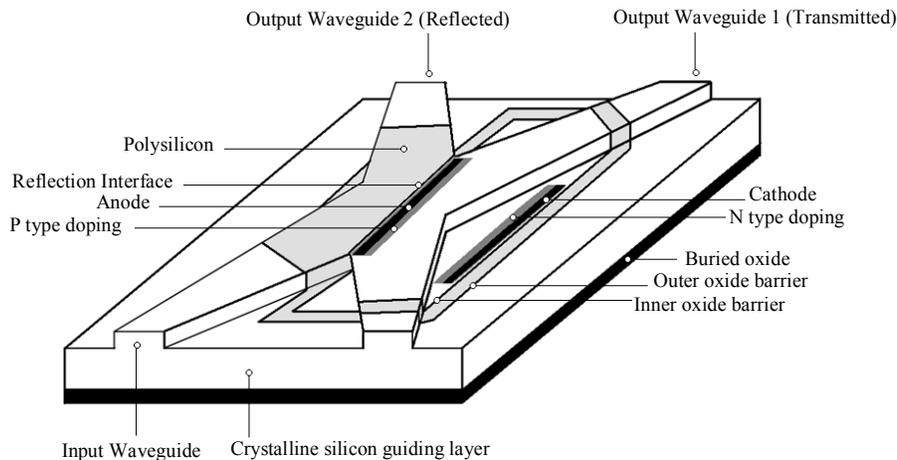


Figure 1 – Diagram of device layout.

Switch design

The layout of the switch can be seen in Figure 1. It consists of two rib waveguides of height 4µm, width 2.8µm and slab height 1.77µm intercepting at an angle θ . Modelling has shown that the switching operation is dominated by multimodal effects at small interception angles and that by tapering the waveguides to double width at the center of the device can reduce the angle at which these effects begin to dominate. Multimodal effects are undesirable since they impair the device performance in terms of wavelength insensitivity.

A 100nm deep, 1µm wide P type doped region ($10^{20}/\text{cm}^3$) is located along the top of the reflection interface and a 1µm deep, 1µm wide N type doped region ($10^{20}/\text{cm}^3$) on the top of the slab exist with

ohmic connections to an anode and cathode respectively. These doped regions are separated by intrinsic single crystal silicon to therefore set up a P-i-N diode structure on one side of the reflection interface. The SiO₂ barrier can be formed by first etching a trench around the region where the injected carriers are to be confined, oxidising the surface of this trench and then refilling it with polycrystalline silicon. Note that away from the reflection boundary, the oxide barrier is kept normal to the direction of the propagating light to minimise the thickness of SiO₂ through which the light propagates. The trench is etched to the buried oxide layer to therefore completely isolate the injection region of the device.

Switching operation

Under zero bias conditions the input light propagates along the input waveguide, passes through the reflection interface to the output waveguide 1. When the device is forward biased carriers are injected into, and fill the region within the inner oxide barrier perimeter. These injected carriers cause a reduction in refractive index due to the free carrier plasma dispersion effect in silicon. The input light will now see a sharp change in refractive index at the reflection interface causing the input light to be reflected and outputted through output waveguide 2 and thus switching occurs.

Oxide Barrier

Using SiO₂ as the barrier material is convenient due to its compatibility with CMOS fabrication processes. Many processes have been reported which can produce reliable SiO₂ films in the sub 3nm regime¹³⁻¹⁷.

For oxides thinner than ~3nm the dominant tunnelling mechanism changes from Fowler-Nordheim tunnelling to direct tunnelling where a reduction in oxide thickness of 0.2nm leads to an order of magnitude increase in direct tunnelling current¹². A 3nm SiO₂ barrier can therefore be used, avoiding the current leakages associated with direct tunnelling. The effectiveness of the 3nm SiO₂ can be seen in the SILVACO¹⁸ modelling shown in Figure 2. Here, a constant 4V forward bias has been applied across a P-i-N diode structure with a 3nm SiO₂ barrier, isolating the injection region of the device from a non-electrically active region.

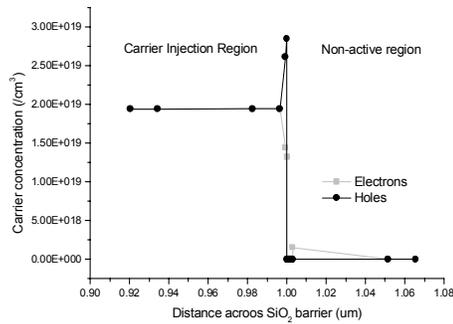


Figure 2 – Carrier diffusion through barrier.

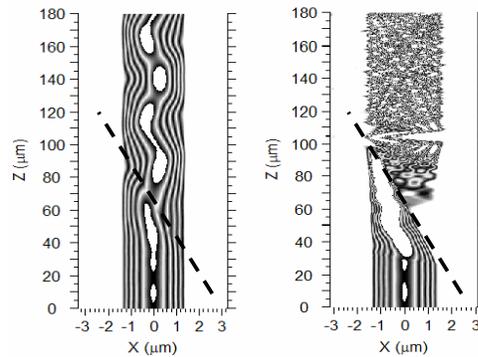


Figure 3 – Propagation along waveguide with (a) 3nm and (b) 100nm barrier crossing at ~2°.

The position of the SiO₂ barrier is at 1 on the x axis. It can be seen that there is no significant diffusion of carrier through the barrier into the non-active region therefore demonstrating the production of a precise reflection interface.

The use of thin SiO₂ layers in the guiding layer of photonic devices has been demonstrated without it significantly perturbing the optical mode and causing significant loss^{10,11}. Preliminary modelling has suggested that the same is true for a 3nm oxide barrier when compared to the use of a 100nm thick barrier along the length of the reflection interface. However it has not yet been possible to optimise the oxide thickness in terms of reflection or loss caused by the oxide due to modelling limitations. The preliminary modelling can be seen Figure 3.

Modelling Evidence

Carrier injection modelling has been carried out in ATLAS¹⁸ to find the change of the electron and hole concentration and therefore the refractive index change with applied current. This change in refractive index has then been imported into a beam propagation modelling program¹⁹ to simulate the device characteristics for a given applied current.

Modelling has shown that using a switch with an interception angle of approximately 4.5° between the input waveguides provides a large difference in transmitted and reflected output waveguide powers with zero bias applied. This angle is also greater than that where multimodal effects become dominant. Figure 4 shows a graph of reflected and transmitted waveguide powers against device current.

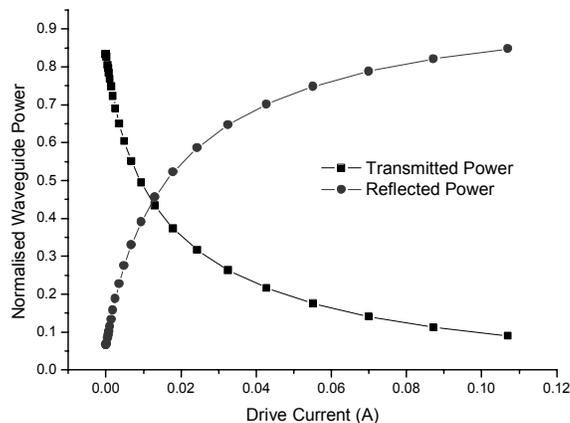


Figure 4 – Output waveguide powers against drive current

It can be seen that as the current increases the output power switches from the ‘transmitted’ to ‘reflected’ output waveguide. The switching current is approximately 100mA although this expected to be reduced through design optimisation.

A single transition in output waveguide power from transmitted to reflected output waveguides with increasing injection current is observed. This is further evidence that the switch is operating under total internal reflection rather than multimodal interference since a periodic transition would be expected in this case.

Conclusions

A total internal reflection based optical switch has been demonstrated in silicon-on-insulator with a SiO_2 carrier restrictive boundary to create a precise reflection interface and improve carrier injection efficiency. Switching current has been modelled to be approximately 100mA although this expected to decrease through design optimisation.

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