High-Performance Thin-Film Transistors in Disordered and Poor-Quality Semiconductors

John M. Shannon and Frantisek Balon

***Abstract*—In general, the range of applications for large-area electronics or macroelectronics is limited by the quality of the semiconductor used to make the electronic devices and circuits. Here, we address the question of how to make high-performance transistors using semiconductors that are defective, have low carrier mobilities, and are unstable. It is proposed that we need to engineer and operate a transistor that minimizes the excess carrier concentration throughout the device combined with high internal fields over small dimensions. Compared with the field-effect transistor, a source-gated transistor more nearly meets these requirements. Using the unstable and defective semiconductor, hydrogenated amorphous silicon, it is shown that high-performance thin-film transistors can indeed be made using the source-gated concept.**

***Index Terms*—Device modeling, disordered semiconductors, field-effect transistor (FET), polymers, Schottky barrier, source-gated transistor (SGT), thin-film transistor (TFT).**

I. Introduction

THERE is a rapidly growing interest in the field of large-area electronics or macroelectronics. This is because electronic circuits and systems over large areas have a direct impact on the man-machine interface whether it be a roll-up flexible display on a plastic substrate, a body imager, wearable electronics, or programmable wall coverings [1], [2]. In general, deposition of semiconductor films used to make electronic circuits has to be carried out at low temperatures to preserve the integrity of the substrate. As a result, inorganic semiconductors are amorphous or microcrystalline. Organic semiconductors are deposited at low temperatures [3]–[5], but these too are highly disordered. The poor quality of these semiconductor layers leads to low circuit speed and electrical instability which seriously limits the applicability of present macroelectronic circuits and systems. The basic building block of all circuits is the transistor. Here, we address the general question of how to make high-performance transistors in semiconductor layers that are defective, have low carrier mobilities and are unstable. Also, we show that by getting away from the only thin-film transistor used today, the field-effect transistor (FET), and using a barrier controlled source-gated structure, we can mitigate against the effects of low mobility and substantially improve stability. This is because the excess carrier concentration in a barrier controlled device is much lower and small structures can be operated with high internal fields leading to devices with higher carrier velocities, shorter transit times, and faster speeds of operation. In addition, these transistors in disordered semiconductors are likely to be more stable.

Manuscript received April 19, 2006; revised September 13, 2006. This work was supported by the Engineering and Physical Sciences Research Council (EPSRC), Swindon, U.K. The review of this paper was arranged by Editor T. Skotnicki.

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Digital Object Identifier 10.1109/TED.2006.888753

II. Disordered and Poor-Quality Semiconductors

Thin-film semiconductors used in macroelectronics range from inorganic semiconductors, such as hydrogenated amorphous silicon, amorphous oxides [6], and metal chalcogenides [4], [7], to organic polymers and plastics and organic–inorganic hybrid semiconductors [8]. All these materials are either amorphous or microcrystalline semiconductors containing a high concentration of defects.

The effect of disorder and impurities in thin-film semiconductors is to introduce a wide range of defects in the band gap. These range from states caused by bond angle and bond length variations, coordination defects in amorphous materials, and grain boundary defects in microcrystalline materials [9]. Defects are characterized by both positional and energetic disorder, and contribute to a distribution of states across the band gap which increases sharply toward the band edges. It has been concluded by Stutzmann [9] that defect formation under charge injection is a general phenomenon in disordered semiconductors. Occupation of localized defect states, such as the weakly bound states in band tails, leads to structural relaxation and defect formation. The assumption is that states are created in the disordered network to minimize excess charge carriers in strained or weak bonds. In hydrogenated amorphous silicon, for example, occupation of weak silicon–silicon bonds by electrons causes them to break, leaving silicon dangling bond defect states deep in the band gap with the process mediated by hydrogen [9], [10]. Defects continue to be generated until the material reaches a new chemical equilibrium corresponding to the new position of the electron quasi-Fermi level leading to severe instability.

Fermi-level dependent defect generation is also expected in polymer semiconductors. Here, as well as localized states due to disorder, we have self-localization of injected carriers. This leads to structural distortion and the formation of defect states in the band gap [11]. Furthermore, the coulombic interaction between carriers or between ionized dopants and charge carriers creates deep states and broadens the distribution of tail states [12]. Therefore, the more excess carriers we have, more carriers are there in localized states, the greater is the magnitude of the instabilities and faster these changes occur. We deduce from Stutzmann's work [9] that to minimize the defect formation

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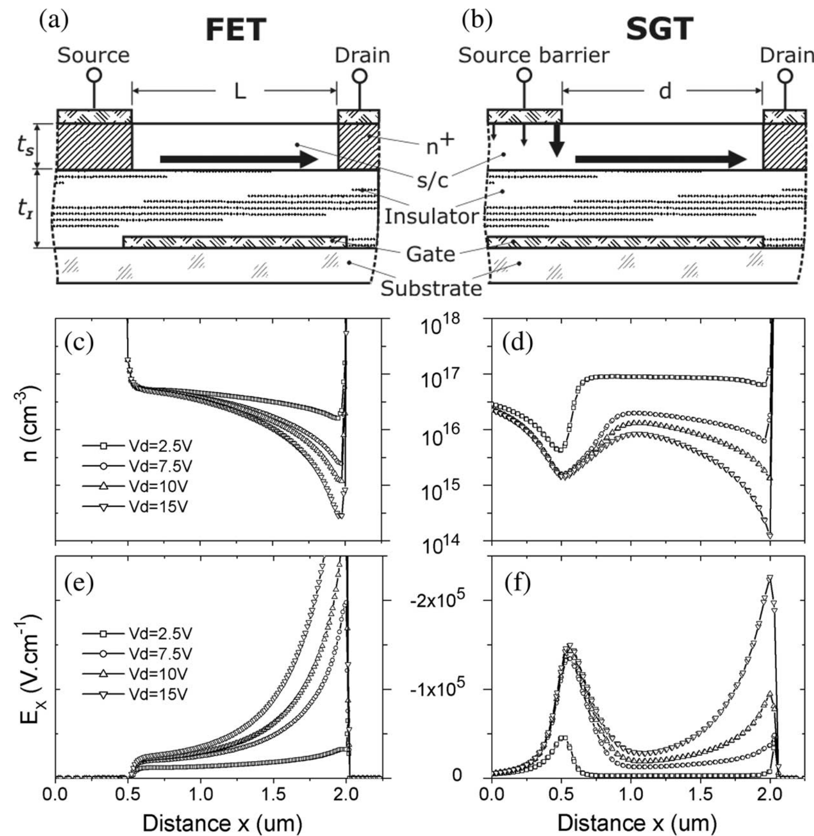

Fig. 1. Structure of a (a) FET and (b) SGT and the differences in key parameters that determine device performance. The electron concentration (c) and (d) and the electric field (e) and (f) are calculated along the semiconductor-insulator interface for a given drain current $(4.10^{-8}$ A/um), $t_S = 100$-nm a-Si:H, $t_I = 300$-nm SiN. The source-barrier height for the SGT is 0.45 eV, source length is 2 μm, and $L = d = 1.5$ μm.

when a transistor is switched on, we must design and operate a transistor such that the excess carrier concentration is low throughout the device.

Another key transistor parameter is the carrier mobility. Increasing the degree of disorder in inorganic semiconductors reduces carrier mobility because carriers spend more of their time in localized states and transport occurs via hopping or tunneling between states leading to low effective mobilities. Similarly in polymers charge transport is by hopping in a disordered system [13] with a mobility that seems to be related in a complicated and unresolved manner to charge density and film morphology [14]. A low carrier mobility is therefore a basic property of hopping transport, and there is not very much we can do about it. However, carrier velocities can be increased by operating with high internal fields. If we wish to maximize the speed of a transistor, then it should be designed and operated so that there are high fields throughout the active region of the device and this region should have small dimensions. Furthermore, in some cases, the mobility itself increases with electric field, thus enabling even higher carrier velocities to be obtained [12], [15], [16].

Based on these considerations, we conclude that to make stable transistors with a useful frequency response, we have to: 1) reduce the carrier concentration and 2) operate with high internal fields throughout the active part of a transistor with small dimension. Condition 1) improves the device stability and reduces device capacitance by lowering carrier concentrations, while condition 2) improves carrier transit time and speed of response by increasing carrier velocity over small distances.

III. Thin-Film Transistors

To date, all transistors used in macroelectronics are of the metal–insulator field-effect type (FET), in which a gate is used to modulate the conductance between a source and drain contact [17]. This transistor has acceptable characteristics for less-demanding applications. However, there is a problem with the FET in the context of requirements mentioned above. The source end of the channel is strongly accumulated with excess carriers when the transistor is switched ON, and this strong accumulation is accompanied by low electric fields.

Recently, a different type of unipolar thin-film transistor was introduced, named a source-gated transistor [18] (SGT), in which the source comprises a potential barrier to current flow and a gate is used to modulate the electric field at the reverse-biased source barrier and change the current. A major difference between the SGT and a FET is that a reverse-biased source barrier controls the current in the ON-state and current saturation is determined by the electrostatics at the source barrier [19] rather than pinch-off at the drain end of a channel. In addition, the geometry of the SGT leads to a much smaller susceptibility to short-channel effects and a higher output impedance because the source barrier is screened from the drain field by the gate [19], [20]. What is interesting in the

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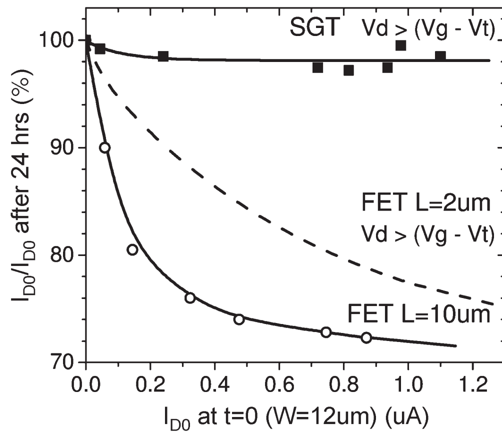

Fig. 2. Current stability of transistors after prolonged temperature-bias stressing. The SGT devices in curve (■) had $d \sim 1.5\ \mu$m as in the simulation (Fig. 1) and were stressed with high drain voltages. The dashed curve is that expected had the source drain separation of the FET been 2 μm since I_D is proportional to $1/L$. The measurements were normalized to a device width of 12 μm.

context of our requirements for high-performance transistors in poor-quality semiconductors is that the carrier concentration in the source region is low and there are high fields sweeping the carriers away toward the drain. Furthermore, these transistors operate very well with small dimensions.

The basic differences in geometry of the FET and SGT are shown in Fig. 1(a) and (b). The FET has ohmic source and drain contacts separated by a gap L. The gate lies under this gap and is able to modulate the conductance of the semiconductor between the contacts. In the SGT, the source is a potential barrier to current transport and the drain is assumed to be ohmic. The gate lies under the source barrier and extends under the source–drain separation d to the drain contact. Although a doped layer is used to make a drain ohmic contact, it is not essential. When the transistor is switched on, the current in the FET [Fig. 1(a)] is determined by the conductivity of the channel between source and drain contacts, while for the SGT [Fig. 1(b)], it is determined by the emission over the source-barrier contact [21], and the channel forms a parasitic resistance. Most of the SGT current flows at the periphery of the source barrier opposite to the drain [22].

IV. Measurements and Modeling of Transistors in a-Si:H

To compare the performance of these structures, we have measured and modeled transistors in hydrogenated amorphous silicon (a-Si:H). This semiconductor is highly defective and notoriously unstable [23]. It is therefore a good example of a poor-quality semiconductor. Furthermore, all the parameters required for modeling of device behavior are known [23]. The values of the main electrical parameters used in this analysis are given in [22]. Simulations of the two devices using the two-dimensional Silvaco Atlas device simulator (v.8.10.0.R) show that the carrier concentration in the source region in the SGT [Fig. 1(c) and (d)] is very much smaller which is to be expected, because the source is reverse biased and the a-Si:H under the source is depleted. For this example, the reduction at the edge of the source where most of the current flows in the

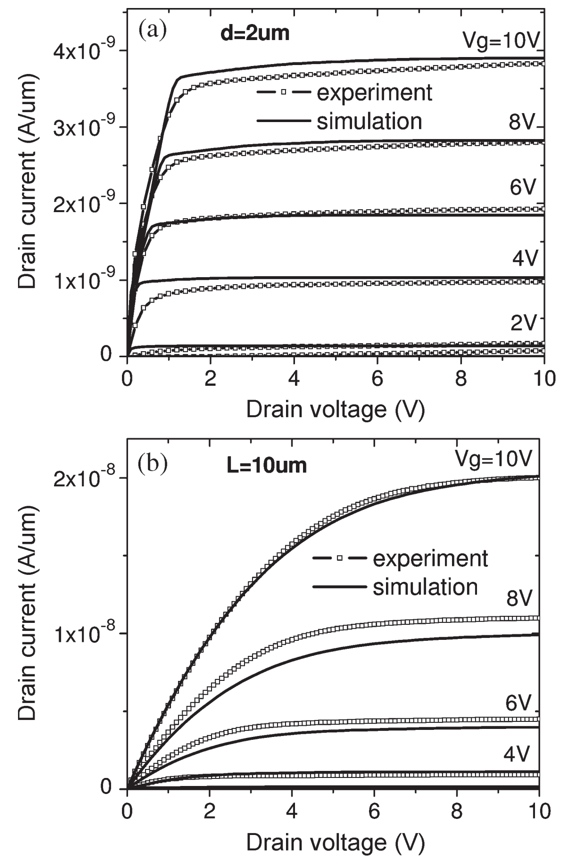

Fig. 3. Comparison between measured and simulated transistor characteristics (a) SGT and (b) FET (t_S = 100-nm a-Si:H, t_I = 300-nm SiN).

SGT is ~100 at high drain voltages. Furthermore, excess carrier concentration decreases with increasing drain voltage.

Measurements of the stability of FETs and SGTs with the same insulator and a-Si:H depositions to that simulated in Fig. 1 are shown in Fig. 2. Transistors were made using the process described in [19]. The source was a Cr Schottky barrier backed up with Al. The effective Schottky barrier height was controlled using a phosphorous donor implant. The gate and drain voltages were kept constant during stressing for 24 h at 30 °C at the values needed to give the current I_{D0} at time $(t) = 0$. It is seen that at the highest currents, the SGT is very much more stable than the FET. At high drain voltages $(V_D > V_G - V_T)$ and with small source–drain separations, the change of current is $< 2\%$ which is quite remarkable. Under these conditions, the electron concentration is lowered not only under the source but throughout the device, as can be seen in the simulations shown in Fig. 1(d). These measurements confirm that just as can be deduced from Stutzmann's work, reducing carrier concentrations decreases the defect formation and the SGT is very much more stable than an equivalent FET. Alternatively, we can say that for a given stability, the SGT can be operated at a higher current.

As discussed above, the way to obtain a good frequency response for a given geometry despite having a low carrier mobility is to operate with high internal fields over short distances to reduce carrier transit times combined with low carrier concentrations for low capacitance. The simulations in Fig. 1(e) and (f) show that the electric field along the interface

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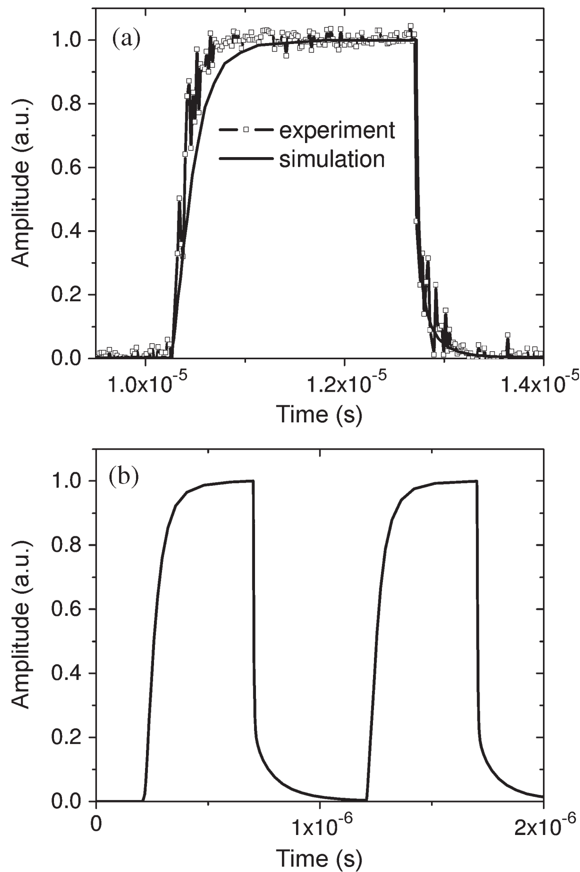

Fig. 4. Comparison between a measured and simulated SGT transient responses. For (a) the source barrier is 0.49 eV, source length is 4 μm, and $d = 6$ μm ($t_S = 100$-nm a-Si:H, $t_I = 300$-nm SiN). For (b) the source-barrier height is 0.4 eV and $d = 1.5$ μm ($t_S = 40$-nm a-Si:H, $t_I = 120$-nm SiN).

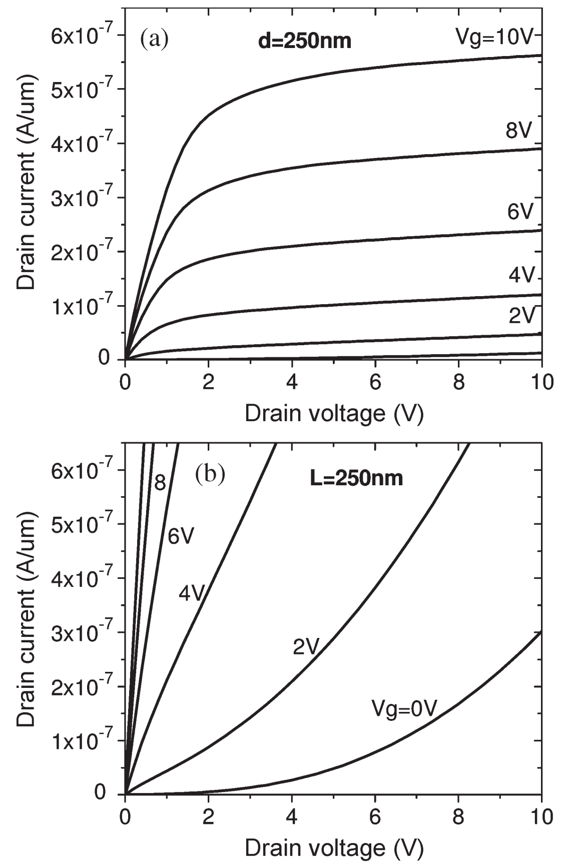

Fig. 5. Comparison of (a) SGT and (b) FET output characteristics for short source–drain separations. Source-barrier height is 0.35 eV, source length is 1 μm, $L = d = 250$ nm ($t_S = 40$-nm a-Si:H, $t_I = 120$-nm SiN).

for the SGT at the edge of the source, where most of the current flows [22], is as much as six times greater than in the corresponding FET. It is also apparent from Fig. 1(c) and (d) that the SGT is more tolerant to short channel effects. At high drain voltages, the FET is in punchthrough and the carrier concentration is affected right up to the source ohmic contact. This causes a deterioration in the output characteristics. In the SGT, however, the current is limited by the source barrier; therefore, at high drain voltages, the carrier concentration at the source is unaffected. This feature of the SGT enables it to operate with much smaller source–drain separations.

The frequency response of the SGT and FET structures can be ascertained using the Atlas device simulator provided, of course, that the simulation is reasonably accurate. A comparison between simulated characteristics and those measured on SGT and FET devices is shown in Fig. 3(a) and (b). It is seen that there is a good agreement between the shape of the characteristics and how the current changes with gate voltage. The field effect mobility is $\sim$0.4 $\mathrm{cm^2/V \cdot s}$. Furthermore, the simulated transient response for a SGT [Fig. 4(a) and (b)] also shows good agreement with measurements. In addition, despite having large dimensions, this SGT is able to respond at frequencies close to 1 MHz. Transient response simulations of a device with thinner layers and a lower source-barrier height to increase transconductance perform well above 1 MHz [Fig. 4(b)] with a cutoff frequency (f_T) of 5 MHz. Decreasing the source barrier further or increasing the gate voltage will increase f_T until it becomes transit time limited at $\sim$20 MHz. In comparison, an equivalent FET becomes transit time limited at $\sim$15 MHz because of lower internal fields. To obtain even higher frequencies, we need to shrink the lateral dimensions and reduce carrier transit times. In the limit, however, the maximum that can be obtained is determined by short channel effects and the ability to preserve transistor characteristics. Simulations show that the SGT [Fig. 5(a)] is much less sensitive to short channel effects compared with a FET [Fig. 5(b)]. While the SGT has a good ON-characteristics with strong saturation, the corresponding characteristics of the FET are very poor and of little use. The presence of a source barrier, even a small one also improves the blocking state as can be seen from Fig. 5 at $V_G = 0$ V. Since the source barrier is a maximum for $V_G < 0$ V, a high ON to OFF current ratio can be obtained especially when the unmodulated source barrier is high. The SGT simulation gave an $f_T \sim 25$ MHz at $V_D = 10$ V. The electric field $\mathrm{E_X}$ was $> 3 \times 10^5$ V/cm throughout the active device giving a transit-time limit > 100 MHz.

V. Conclusion

We conclude that in order to make high-performance transistors in disordered and poor-quality semiconductors, we have

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to engineer devices with low excess carrier concentrations and high fields over short distances. The low carrier concentration reduces the change in the carrier quasi-Fermi level between ON and OFF states of the transistors and improves stability while high internal fields increase the carrier velocity and mitigates against low carrier mobility.

It is shown that compared with a standard FET, the SGT more nearly meets these requirements, and it is demonstrated using a-Si:H that the source-gated concept leads to thin-film transistors with excellent stability and good frequency response in unstable semiconductors with low mobilities. These results have implications for transistors in all disordered and poor-quality semiconductors, since the requirements for high performance are broadly the same and bring the possibility of fully integrated digital and analog macroelectronic circuits and systems very much closer.

ACKNOWLEDGMENT

The authors would like to thank Philips Research Laboratories, Redhill, Surrey, U.K., for the manufacture of the transistors.

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