Pronounced hysteresis and high charge storage stability of single-walled carbon nanotube-based field-effect transistors

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In this letter, pronounced hysteresis loops were observed in single-walled carbon nanotube-based field-effect transistors (CNTFETs). The shift in threshold voltage was found to increase with increasing gate voltage sweep ranges. A significant enhancement in the charge storage stability over 14 days was obtained at room temperature after a two-stage hydrogen and air annealing process was applied to the CNTFETs. The passivation of interface traps by annealing in hydrogen and the removal of physisorption solvent molecules by annealing in air are suggested to be responsible for the improvement of the charge storage stability. © *2005 American Institute of Physics*.
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In recent years, a significant interest in carbon nanotube-based devices has been witnessed, including field-effect transistors (FETs),[1,2] room-temperature single-electron transistors,[3] electron field emitters,[4,5] diodes,[6] and biosensors.[7] The performance of one particular group of devices, carbon nanotube-based field-effect transistors (CNTFETs), has improved steadily[8,9] since the first successful batch of CNTFETs was reported in 1998.[1,2] Most recently, there have been several reports of the observation of memory effects in various CNTFETs. Fuhrer *et al.*[10] constructed a nonvolatile charge storage memory element using a high-mobility (9000 $cm^2/V\,s$) semiconducting single-walled carbon nanotube (SWNT) (2.7 nm in diameter) based transistor. As the gate voltage was swept back and forth between +10 and −10 V, a large hysteresis was observed in the curves of the drain current versus gate voltage at room temperature. The threshold gate voltage at which the nanotube began to conduct was shifted by more than 6 V. The retention time of the charge memory effect of their CNTFETs exceeded 5000 s. Radosavljevic *et al.*[11] reported an air-stable *n*-type CNTFET with a similar hysteresis phenomenon and the bit storage time of at least 16 h at room temperature. Cui *et al.*[12] presented molecular memory devices fabricated using semiconducting SWNTs. Charge storage was achieved by sweeping the gate voltage in the range of ±5 V, associated with a storage stability of at least 12 days at room temperature. A significant threshold voltage shift, combined with a long charge retention time, is the prerequisite for memory devices. However, for practical applications, the performance of CNTFET memory devices needs to be further improved especially in terms of their long-term stability. To date, little systematic work has been reported on the charge storage stability of the CNTFET memory. In this letter, we report the fabrication of memory devices using 1.8 nm diameter SWNTs, employing a simple two-stage annealing process involving hydrogen and air treatment which resulted in good memory characteristics with a pronounced hysteresis which was stable for at least 14 days.

Figure 1(a) shows a schematic diagram of the structure of the CNTFETs. A highly doped *p*-type Si substrate served as the backgate. A 200-nm-thick SiO_2 layer was thermally grown on the top of the Si substrate, annealed at 150 °C for 0.5 h in a hydrogen atmosphere. The electrodes were fabricated using 10-nm-thick titanium (Ti) and 90-nm-thick gold (Au), and were patterned on the SiO_2/Si substrate using a conventional lift-off process. The SWNTs used in this work were grown by an arc-discharge technique in the form of soot. SWNT soot was sonicated in dichloroethane to produce individual SWNTs. A droplet of SWNT suspension was then spin coated onto the SiO_2/Si substrate which contained predefined Au/Ti contact patterns. The metallic SWNTs were selectively burned by current induced oxidation.[13] Following the oxidation procedure we were able to select a single, well bridged SWNT that contacted both the source and the drain electrodes, while removing other nanotubes from this structure using an atomic force microscope (AFM) in a contact

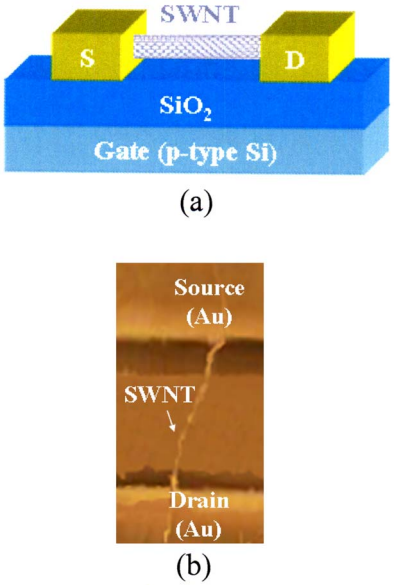

FIG. 1. (Color online) (a) Schematic diagram of the CNTFET structure. The highly doped *p*-type Si substrate served as a backgate. (b) AFM image of a typical CNTFET sample. A SWNT bridged the source (*S*) and the drain (*D*) electrodes.

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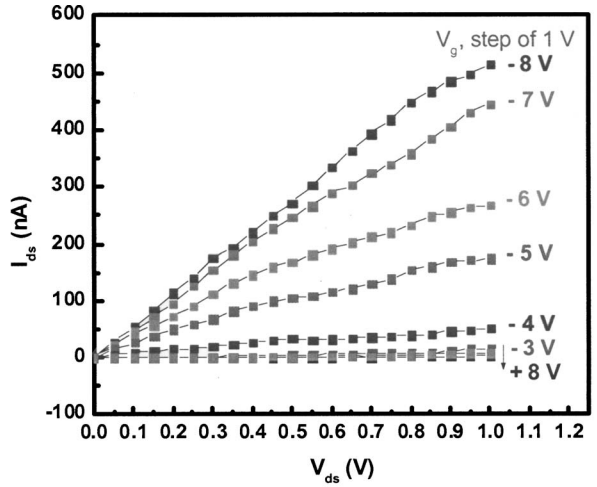

FIG. 2. Transistor characteristics of the CNTFETs with a channel length of 800 nm. The measurement was carried out with V_g ranging from −8 to 8 V in a step of 1 V at ambient environment.

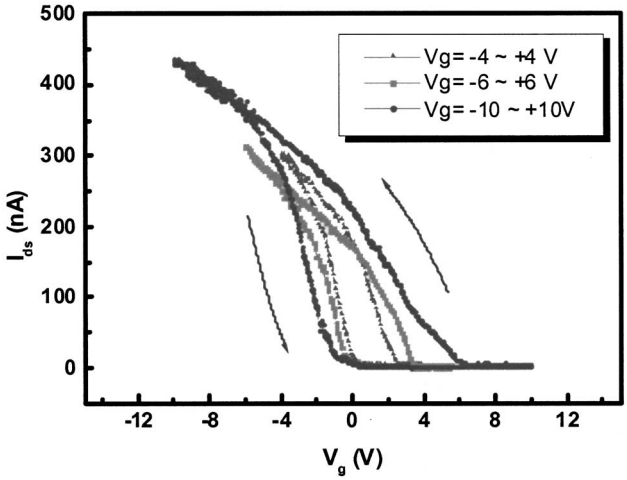

FIG. 3. $I_{ds}-V_g$ curves measured at the voltage sweeps of −4 to +4, −6 to +6 and −10 to +10 V with $V_{ds}=1$ V at room temperature, respectively. Pronounced hysteresis behavior was clearly observed.

mode. The completed devices were finally annealed at 140 °C for 0.5 min in air (oxygen atmosphere). Figure 1(b) shows an AFM image of one of the investigated CNTFET samples. One can see that a SWNT bridges the two gold electrodes, which correspond to the source (*S*) and the drain (*D*), respectively. The SWNT functioned as a conducting channel, with a channel length of 800 nm. The diameter of a single SWNT was around 1.8 nm measured using a JEOL 2010 transmission electron microscope (TEM).

A HP-4156B precision semiconductor parameter analyzer was used to measure the transfer characteristics of the CNTFETs at ambient conditions. Figure 2 shows the transistor characteristics ($I_{ds}-V_{ds}$) of the as-fabricated CNTFETs. One can observe that the forms of the $I_{ds}-V_{ds}$ plots change by increasing the gate voltage from −8 to 8 V. The channel conductance decreases as the gate voltage V_g becomes more positive, indicating a *p*-type channel. The hole mobility, which was determined by assuming the classical FET model,[14] is found to be ~500 cm^2/V s even at a large 1 V source-drain potential. This value is higher than that of 20 cm^2/V s reported by Martel *et al.*. for SWNTs,[2] whereas lower than that of 9000 cm^2/V s, which was obtained by Fuhrer *et al.*[10]

Figure 3 presents $I_{ds}-V_g$ data which were taken at room temperature with $V_{ds}=1$ V applied to the source electrode for gate voltage sweeps of −4 to +4, −6 to +6, and −10 to +10 V, respectively. Pronounced hysteresis loops, which reflect memory effects, are clearly observed in the drain current versus the gate voltage, and the hysteresis loops were found to be reproducible. The corresponding threshold voltage shifts, defined as the shift of the gate voltage at which $I_{ds}=5$ nA, which can also be considered as the memory window of the device, are 2.3, 3.8, and 6.7 V, respectively. This reflects that the charge storage capabilities of the device increase with increasing gate voltage sweep ranges. The memory effects are suggested to be originated from the charge traps in the underlying SiO_2/Si substrate at room temperature. TEM observation indicated that the diameter of our SWNT was only 1.8 nm, such a small diameter SWNT can cause a highly localized electric field at the nanotube surface.[10,11] Charges are therefore easily reversibly injected and removed from the SiO_2 dielectric by applying a bias voltage across the dielectric between the carbon nanotube and the substrate. This characteristic makes the CNTFETs possible to function as nonvolatile charge storage memories.[10,12] In order to improve the memory performance, a CNTFET with a charge storage node is under construction. Our observation that a larger gate voltage sweep range leads to a larger threshold voltage shift might be due to an increase in the amount of charges stored in the dielectric with increasing injected charges from the SWNT channel.

In the roadmap of nonvolatile memories, besides the threshold voltage shifts, the charge storage stability (retention time) is another very important factor for their practical applications. However, little attention has been paid to this subject for the CNTFET memory to date. In order to improve the charge storage stability of the CNTFETs, a two-stage annealing process was employed. The first annealing stage was applied using hydrogen, after the growth of the SiO_2. The second stage was carried out on the completed CNTFETs in air. Figure 4 shows the retention characteristic of the CNTFETs with and without the annealing treatment at a temperature of 22±2 °C. The threshold voltages at the "On state" and "Off state" were obtained by multiple measure-

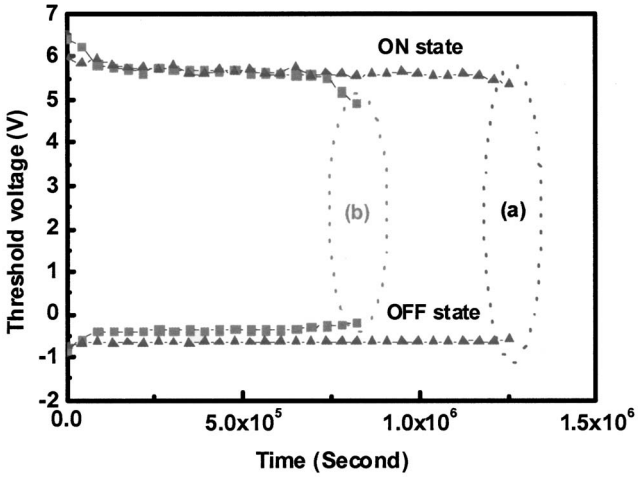

FIG. 4. Retention characteristics from the CNTFETs (a) with and (b) without two-stage annealing treatment. The measurements were carried out at the gate voltage sweeps of −10 to +10 V at ambient conditions.

ment of the I_{ds}–V_g curves after writing to "On" state and "Off' state for only one time, respectively. One can see that for the two-stage annealed CNTFET, as shown in Fig. 4(a), the threshold voltage shifts show little variation over a period of more than 14 days at room temperature. In contrast, for the CNTFET without annealing treatment, as shown in Fig. 4(b), one can observe that the threshold voltage shifts initially decrease after 2.5 days, then reach a steady value and finally decrease again after a further 8 days. Similar short-term degradation in threshold voltage shift has previously been reported on non-annealed CNTFET devices.[15] Figure 4 indicates that the two-stage annealing process can effectively improve the charge storage stability of CNTFETs.

Choi *et al.*[16] measured the drain current as a function of time at 5 K. They observed that the current was stable for a period of 100 s. Lee *et al.*[17] and Yang *et al.*[15] held their CNTFET device at zero gate voltage, and the device maintained a hysteresis loop for at least 7 days. Cui *et al.*[12] reported a CNTFET memory device with a storage stability of at least 12 days at room temperature. Compared to the reported CNTFET memory devices, our two-stage annealed devices show a higher charge storage stability. We attribute this higher stability to the effect of the two-stage annealing process carried out on the devices in hydrogen and air. On the one hand, annealing in hydrogen is believed to efficiently passivate the interface traps and generate the lower interface trap density,[18,19] therefore resulting in a slow degradation of the threshold voltage and drain current. On the other hand, annealing in air could remove the physisorption solvent elements such as water and alcohol molecules[15] at the nanotubes, besides, it can also reduce the interface trap density,[20] leading to an enhancement of the charge storage stability. The detailed mechanism needs to be studied further.

In conclusion, distinct hysteresis was clearly observed at the curves of the drain current against gate voltage of carbon nanotube-based field-effect transistors. The threshold voltage shift values are found to increase with increasing gate voltage sweep ranges. The device also exhibits high charge storage stability with a storage retention time of more than 14 days. A two-stage annealing process in hydrogen and air is believed to be responsible for the improvement of the storage stability. The pronounced hysteresis and the high charge storage stability make CNTFETs potential candidates for the development of the ultrahigh density nonvolatile memory devices.

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