Source-Gated Transistors for Versatile Large Area Electronic Circuit Design and Fabrication

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Source-gated transistors (SGTs) comprise a blocking contact or potential barrier at the source, which control the current. The paper describes how SGTs can be optimized for particular applications and for specific semiconductor material systems. It is shown how the saturation voltage can be designed to be an order of magnitude smaller than in equivalent FETs to give power savings of over 50% for the same current output. The SGT also achieves a better saturation regime, with lower output conductance over a larger range of drain voltages. Flat-panel lighting, remote sensing and signal processing and large-area circuits made using inexpensive but imprecise patterning techniques are some of the applications which could benefit from incorporating these devices.

Introduction

Improvements in material science and fabrication techniques are rapidly increasing the speed, analog capabilities and cost-effectiveness of complex large area electronic (LAE) systems. For future power-efficient, robust applications, similar gains can be foreseen by advances in device engineering.

The source-gated transistor (SGT) (Figure 1) is a type of thin-film transistor in which the current is mainly controlled by the effective height of a source barrier [1]. The gate lies opposite and overlaps the source and represents the means through which the source barrier height can be controlled during operation. SGTs can be produced in any technology which permits staggered electrode configurations and is compatible with semiconductor systems for which a potential barrier can be created at the source. There are several routes to engineering this barrier, the most convenient of which is the Schottky (rectifying metal-semiconductor) contact [2, 3].

Due to their structure, the operation of SGTs [1, 4] is quite different from that of conventional thin-film field effect transistors (FETs). However, SGTs are compatible with FET technologies and both types of devices can be used in a given design, exploiting the advantages of each, as required.

In this paper we examine the key areas in which SGTs have the potential of superior performance in comparison with conventional FET devices of similar geometry and operating under comparable conditions. The discussion begins with an enumeration of essential performance aspects and an explanation of how the design of the SGT allows improvements in these specific areas, and we conclude with a description of the manner in which these advantageous features can be applied to different material systems and common circuit functions.

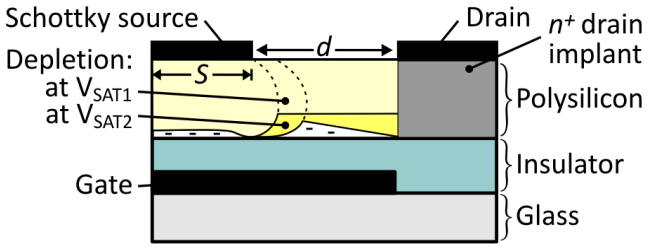

Figure 1. Schematic cross-section of a SGT in which the drain is self-registered to the gate, showing: the parasitic FET channel which forms between source and drain, source length (S), source-drain separation (d) and depletion region when the FET channel pinches off at the source ($V_{DS}=V_{SAT1}$) and at both the source and the drain ($V_{DS}=V_{SAT2}$).

Main Performance Characteristics of the Source-Gated Transistor

The presence of a reverse biased potential barrier at the source [1 - 4] has several effects on the operation of the device. Specifically, because the current through the entire transistor is limited by the source barrier, it will be lower than that developed by a FET with the same geometry and bulk doping. The current will also have a positive temperature coefficient [5] and will not be influenced significantly by some of the parameters which define the operation of a FET, such as the size of the source-drain gap (*d*, Figure 1). There are a number of advantages of the SGT architecture as well; a brief description of the main differences between SGT and FET operation follows.

Saturation voltage

In FETs, the current saturates at a drain voltage equivalent to the difference between the gate bias and the threshold voltage. As such, a 1V increase in gate voltage will raise the saturation voltage by 1V. In comparison, the saturation voltage of SGTs is governed by the electrostatics of the stack formed by the source electrode, semiconductor, insulator and gate electrode [6]; if a thick insulator or very thin semiconductor are used, then the change in saturation voltage with SGT gate voltage can be significantly lower than that of a FET (Figure 2). For a given drain current the power dissipation in any transistor increases proportionally with the serial voltage drop on the device and a lower saturation voltage translates directly in power savings. In Figure 2, the SGT draws around 60% less power than the FET at the onset of saturation.

The drawback of low saturation voltage is the reduced value of transconductance, and it occurs as a consequence of increased insulator thickness, which effectively lowers the gate field for a given gate bias.

Output impedance in saturation

As the barrier controls the current in saturation, the operating regime of the parasitic FET which forms between the source and the drain becomes less important. Strong saturation can be achieved well below $V_D = V_G - V_T$. When the parasitic FET is in saturation, the characteristic becomes extremely flat, which is advantageous for high-impedance active loads, current sources and analog amplifiers. Furthermore, in high mobility semiconductor technologies, the source barrier greatly reduces the kink effect [4] by extracting minority carriers and preventing bipolar amplification [7].

Overall, this means that the flat saturation region is increased toward both lower and higher voltage compared to that of a regular FET for improved dynamic range, and it is worth noting that this may lead to additional improvements in energy efficiency by not allowing the current to increase significantly with drain voltage.

Operating frequency

Another consequence of the control of current by the source barrier is that the distance between the source and the drain plays no role so long as it is not large enough to make the FET channel too resistive. The source-drain gap can be made very small, giving a higher operating speed to the device while maintaining a flat saturated current. The operation of the gate-source stack also leads to current crowding at the edge of the source, which means that the source length can be decreased for improved source current density. It has been shown that the operating frequency is proportional to average current density [8]; low-mobility semiconductor technologies could greatly benefit [9], especially in the realm of analog design, as the high output impedance characteristic is retained.

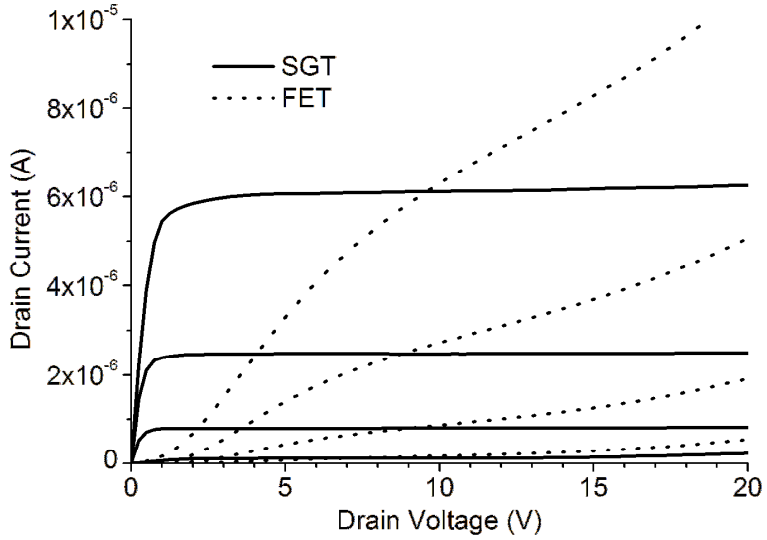

Figure 2. Output characteristics for SGT and FET devices in polysilicon with identical geometries and biased for similar saturated currents. The lower saturation voltage and flatter saturation characteristic of the SGT are apparent. Owing to lower transconductance, to achieve the same drain current, the drive voltage of the SGT is higher than that of the FET. Top to bottom gate voltages: –3, –4, –5, –6 V (FET); 20, 9, – 1, –3V (SGT).

Tolerance to process variations and suitability to cost-effective patterning techniques

The SGT architecture is also well suited for emerging technologies such as inkjet printing and stamping, where fabrication tolerances may be high. As seen in Figure 3, the current is independent of source-drain gap and, due to current crowding at the source edge, can be made to be very insensitive to source length [10]. This is a useful feature which can improve consistency of performance across a large-area substrate and, to some extent, the reliability of complex analog circuits realized with these technologies.

Off-current

The minimum off-current through a FET is strongly dependent on bulk doping; SGTs can have a much lower off-current: the reverse leakage through the source barrier [2, 3, 5]. A diagrammatic representation of this effect is given in Figure 4.

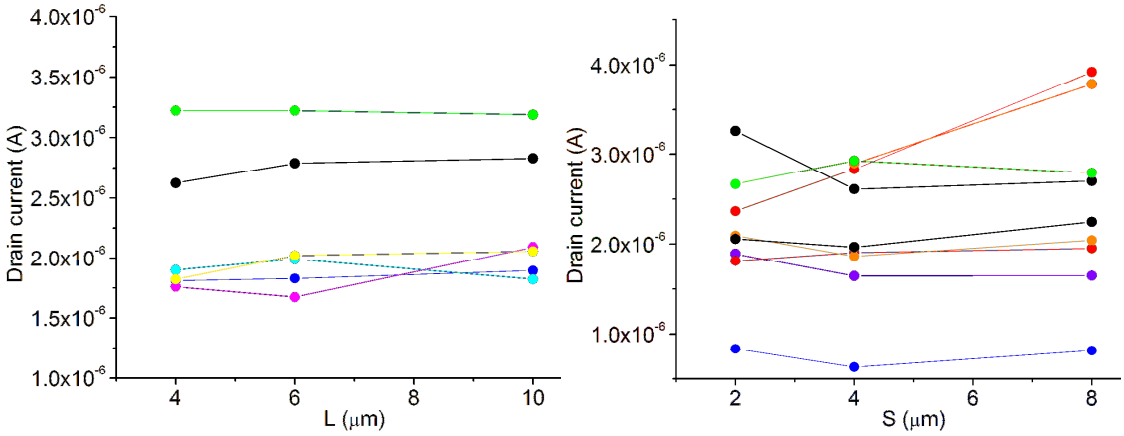

Figure 3. Drain current measured on poly-Si SGTs of various sizes biased at roughly the same current, showing little change with: *a)* source-drain gap and *b)* source length.

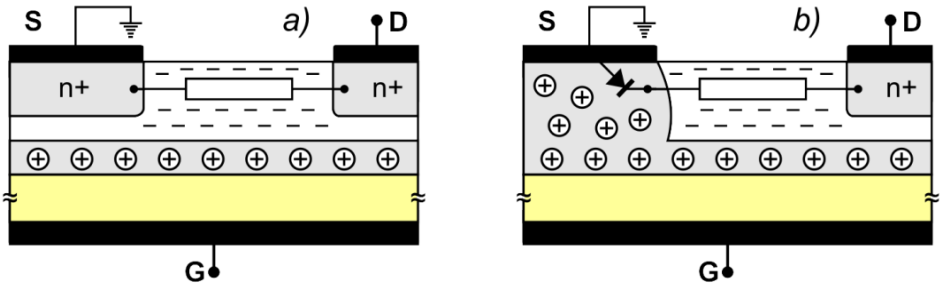

Figure 4. Schematic diagram explaining why an n-type FET (*a*) realized in a strongly n-type semiconductor does not turn off well but a similar SGT (*b*) does.

Stability under electrical stress

During SGT operation, the number of excess carriers in the device is dictated by the operating conditions of the source barrier and, as such, can be substantially smaller than in a similar FET. In amorphous semiconductors especially, this produces a large improvement in electrical stress-induced threshold voltage instability [10], as it has been proven that defect generation is related to excess carrier density [11].

Temperature coefficient of drain current

When high Schottky barriers are used, the current through the device is strongly temperature dependent [2, 3, 5]. On the one hand, this effect can be turned into a useful feature by applying the high barrier SGT as a very sensitive temperature sensor. On the other hand, the temperature dependence can be minimized by designing lower source barriers. Low barrier polysilicon SGTs have shown positive temperature coefficients in

the order of those of FETs [5]. A trade-off between the quality of saturation and the temperature coefficient must be made in choosing the specifications of the source barrier.

Benefits of Source Gated Transistors to Common Applications and Material Systems

In the previous section we have shown how the operation of the SGT, and specifically the existence of a reverse-biased potential barrier at the source, leads to some improvements in key parameters over conventional FET structures. Several common circuit applications (Table I) could benefit from incorporating SGTs.

For current sources and active matrix pixel drivers, the low saturation voltage translates into low supply voltage operation for greater energy efficiency, and the flat saturation characteristic over a wide range of voltage improves signal amplification and reduces crosstalk through the power lines.

Low barriers can be used to ensure low temperature coefficients; conversely, the SGT can function as a high-resolution sensor.

The improved stability to electrical stress is advantageous to all analog applications, reducing the need for compensating schemes and lowering circuit complexity.

As switches, SGTs may have lower off-current than similar FETs, which would improve static power dissipation. Their use could contribute to a smaller circuit footprint in mixed signal circuits such as pixel drivers: as a result of lower leakage and improved charge retention, storage capacitors can be reduced in size.

TABLE I. Common applications and their key performance characteristics which could be improved by implementing with SGTs

Performance characteristic	Current source and pixel driver	Analog gain stage	Temperature sensor	Digital switch
Output impedance in saturation	●	●	●	
Operating frequency		○		○
Saturation voltage and static power dissipation	●	●	●	
Temperature coefficient of drain current	○	○	●	
Off-current				●
Sub-threshold slope				○
Stability under electrical stress	●	●	●	

● – feature which could improve if using SGT implementation
○ – feature which does not change if using SGT implementation

Some detrimental material peculiarities can be worked around by using source-gated transistors in place of regular FETs (Table II): stability is improved in amorphous materials; the kink effect is minimized in high-mobility semiconductors and the operating frequency of organic SGT can be increased by taking advantage of the field-dependent mobility [9]. In virtually all materials the output impedance in saturation is increased and the saturation voltage can be greatly diminished leading to greater energy efficiency.

As the current through the SGT is nearly insensitive to changes in source length or source-drain gap, registration and size errors are not critical. Printing, stamping and other

high-volume, cost-effective fabrication processes can be employed with minimal impact on circuit performance.

These characteristics of SGTs may open the path to analog and mixed signal circuit applications which were previously impractical to consider or too expensive to fabricate, e.g. flexible, printed sensors, displays and other analog and mixed signal designs.

TABLE II. Material systems and their key performance characteristics which would improve significantly by implementing with SGTs

Performance characteristic	a-Si:H and other low-mobility inorganic	Poly-Si and high mobility inorganic	Solution-processed organic
Output impedance in saturation	●	●	●
Operating frequency	●	○	●
Down-scaling and process variability	●	●	●
Stability under electrical stress	●	○	●

● – feature which could improve significantly if using SGT implementation
○ – feature which could improve somewhat if using SGT implementation

Conclusions

We have outlined a number of performance characteristics which make the source-gated transistor (SGT) preferable for certain circuit application to standard thin-film field-effect transistors (FETs). The versatility of the SGT would allow designs containing it to potentially improve operational parameters or circumvent undesirable properties of particular material systems: power dissipation, analog amplification, leakage current, stability and uniformity of performance over a large substrate area. Flat-panel lighting, remote sensing and signal processing are some of the areas which could benefit from incorporating these devices. SGTs and FETs can be included in the same design and the advantages of each exploited simultaneously, which may prove a great benefit when optimizing future designs for specific low-power, large area applications.

Acknowledgments

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