Raised Source / Drain (RSD) for 50nm MOSFETs – Effect of Epitaxy Layer Thickness on Short Channel Effects.

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Abstract

We present raised source/ drain MOSFET devices with channel lengths down to 50nm. The raised source/ drain structures are fabricated by growing a selective epitaxial silicon layer in the source and drain regions of the MOSFET device after sidewall spacer creation and before HDD implant. The layers were grown in a low pressure LPCVD epitaxy reactor with a mixture of silane and dichlorosilane. A pre epitaxy process that eliminates the need for a pre epitaxy bake in hydrogen has been developed. In this study we have varied the thickness of this selective epitaxial silicon layer to investigate the effect of this parameter on device performance. Reducing the channel length of the devices has a detrimental effect on SCE and DIBL. In this paper we will show how short channel performance can be retrieved by adding the raised source/ drain structures, and how increasing the thickness of these structures improves these parameters further.

1. Introduction

As MOSFET devices are scaled into the decananometre era, good control of short channel effects requires the formation of ever shallower junctions [1]. These shallower junctions increase the parasitic series resistance of the source and drain. This extra resistance can be reduced by reducing the thickness of the sidewall spacer, but this degrades short channel performance as lateral diffusion of the HDD under the spacer "swallows" the extension [2]. The elevation of the source and drain suppresses the sub diffusion of the HDD dopant under the edge of the sidewall spacer [3], allowing the spacer to be thinner while maintaining short channel performance.

In this paper we have fabricated raised source/ drain MOSFET devices with channel lengths down to 50nm [4,5]. The thickness of the epitaxial raised source/ drain structure has been varied to investigate the effect of this parameter on device electrical performance.

2. Device Fabrication

Devices were fabricated on 8" wafers in the clean room facility at LETI. The epitaxy layers were grown on part processed wafers at the University of Southampton, using a process developed at the University. After growth of the epitaxy layers, the wafers were returned to LETI for process completion.

Device processing started with the growth of a 180nm thick LOCOS field oxide and well implantation. A 2nm gate oxide was then grown and 150nm of polysilicon deposited on top of this oxide to form the polysilicon gate electrode. Polysilicon was pre-doped by implantation before etch, and gates were defined by electron beam lithography. Polysilicon was then dry etched. A diagram showing the processing of the devices up to this stage is shown in figure 1. Source/ drain extensions were then implanted and 25nm wide silicon nitride sidewall spacers created, as shown in figure 2. Selective epitaxial silicon layers were then grown in the source and drain regions of the devices in a LPCVD reactor. The epitaxy layers were grown with a mixture of silane and dichlorosilane gases at a growth pressure of 1 Torr. Pre-epitaxy hydrogen bake was eliminated and replaced by new wet process that entailed a dip in a 2% HF acid solution followed by a rinse in IPA immediately prior to the growth of the epitaxial silicon layers. The growth temperature was 750C so that the total thermal budget of the process is compatible with a 50nm CMOS process. The growth time of the selective epitaxial silicon layer was 10 minutes for the wafer with the thickest epitaxy layer. This gives an epitaxial silicon layer that is approximately 100nm thick. For the other wafers reported on in this paper the growth time was reduced to 8, 6 and 4 minutes, to give epitaxial layers of

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thickness 80nm, 60nm and 40nm. After growth of the epitaxy layers the HDD was implanted into the epitaxial silicon, and dopants were activated by rapid thermal anneal. Device processing was completed with a back end of a BPSG inter level dielectric and Ti/TiN/Al metal. A diagram of a finished device is shown in figure 3. A cross sectional SEM picture of a completed MOSFET structure is shown in figure 4, and a tilted SEM picture of a MOSFET structure, showing the active area bounded by the LOCOS oxidation oxide, is shown in figure 5. The epitaxial layers are facet free, the process is selective to both silicon dioxide and silicon nitride, and there is no bridging between the raised source and drain and the polysilicon gate electrode.

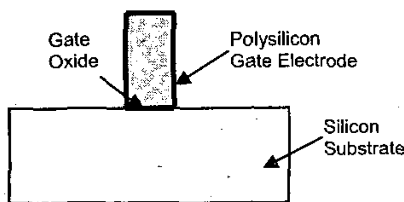

Figure 1. MOSFET device after etch of the polysilicon gate electrode.

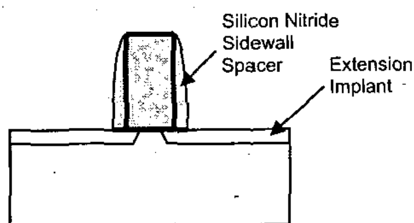

Figure 2. MOSFET device after creation of silicon nitride sidewall spacers.

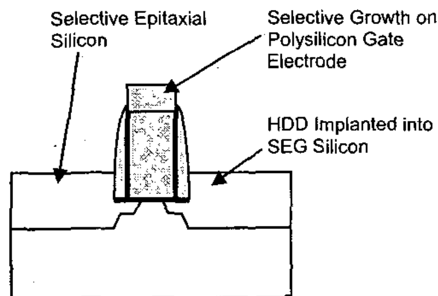

Figure 3. Final MOSFET device structure.

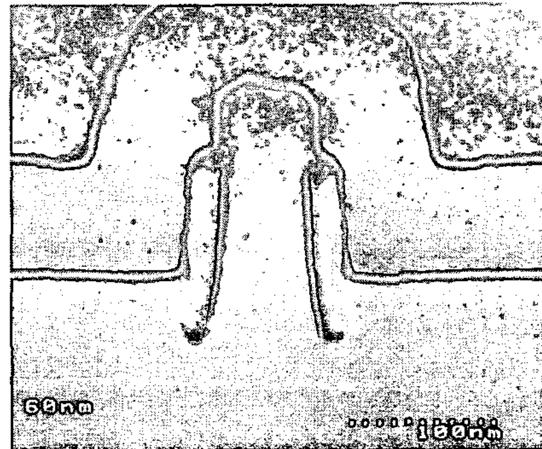

Figure 4. Cross sectional SEM picture of a MOSFET structure.

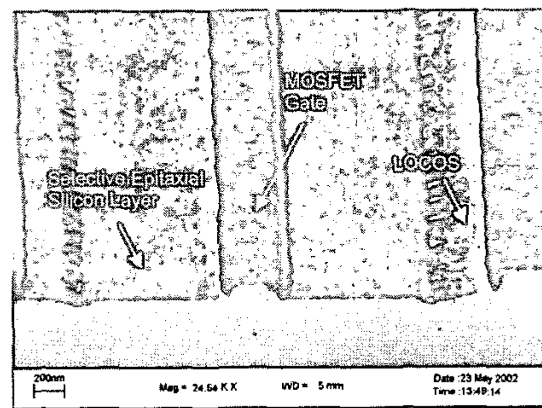

Figure 5. Tilted SEM picture of a MOSFET structure, showing growth of selective epitaxial silicon in the source and drain regions.

3. Electrical Results

Id vs. Vg curves measured on a 50nm RSD NMOS device at high and low drain bias are shown in figure 6. A plot of threshold voltage vs. device channel length is shown in figure 7. The threshold voltage roll off (the difference between the threshold voltage of 50nm devices and long channel devices) is shown in figure 8. The effect of the selective epitaxial silicon process reducing the threshold voltage roll off can clearly be seen. The threshold voltage roll off of the 50nm silicon reference devices (with no raised source/ drain structure) is 198mV, compared to just 53mV for the devices with the 100nm thick epi layers.

The improvement in DIBL performance of the devices can be seen in figure 9, showing the difference in threshold voltage (Vdibl) of the devices measured at Vd=0.1V and Vd=1.5V. Vdibl for the 50nm reference

device is 0.284V, but this reduced to 0.15V by the addition of a 100nm RSD structure.

The RSD structures also reduce the current drive (Ion) of the RSD devices, as shown in figure 10. The Ion of the 50nm RSD device, measured at Vg=Vd=1.5V with 100nm RSD structures is 395μA/μm width, compared to 515μA/μm width for the 50nm reference device.

The relationship between Ion and Ioff was also investigated, as shown in figure 11. Ioff, measured at Vg=0V, Vd=1.5V is 0.272nA/μm width for RSD 50nm device with 100nm RSD structures, compared to 511nA/μm width for the 50nm reference device. No improvement or degradation in Ion is seen in these devices for a given Ioff.

The sub-threshold slope (S) of small devices is also improved by the addition of RSD structures. The 50nm reference non-elevated silicon device has a sub-threshold slope (S) of 102mV/dec. S for the 50nm device with 60nm RSD structures is 101.5mV/dec, the 50nm device with 80nm RSD structures has a subthreshold slope of 94.8mV/dec, and 100nm RSD structures give an S of 81.9mV/dec.

4. Discussion

The addition of the RSD structures suppresses the lateral diffusion of the highly doped source and drain (HDD) under the sidewall spacers [3]. The effect of this is to reduce the amount of dopant diffusing into the extensions during processing. This means that the extensions of the raised source/ drain devices are shallower and more resistive than these of the silicon reference device, and that this effect is more marked as the thickness of the epitaxial silicon layer is increased. The shallower junctions of the elevated devices give better short channel behaviour and DIBL [2]. The steeper sub threshold slope of the RSD devices is explained by the better gate control on the channel potential as the shallower junctions reduce the penetration of the electric field from the source and drain into the device channel. The higher resistivity of the extensions and reduction in short channel threshold roll off accounts for the loss of current drive in the elevated devices. This can be compensated for by optimisation of the HDD implant for the elevated devices.

5. Conclusions

Raised source/ drain MOSFETs, with channel lengths down to 50nm, have been made with a facet free selective epitaxial silicon process with a thermal budget compatible with a decananometre CMOS processes. Electrical measurements show that the raised source drain devices have improved SCE and DIBL over their conventional non-elevated counterparts, and that this performance increases as the thickness of the epitaxy layers increases. No improvement or degradation in Ion is seen for a given Ioff.

6. Acknowledgements

We would like to thank the European Commission for funding this work through the SIGMOS program.

7. References

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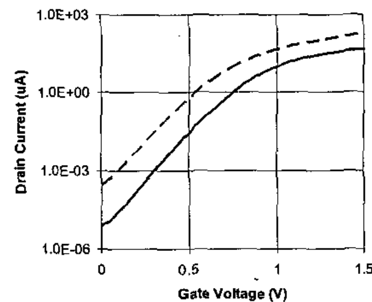

Figure 6. Plot of gate voltage vs. drain current for a 50nm raised source/ drain MOSFET with a 100nm epitaxy layer, measured at a drain voltage of 1.5V (dashed line), and 0.1V (solid line).

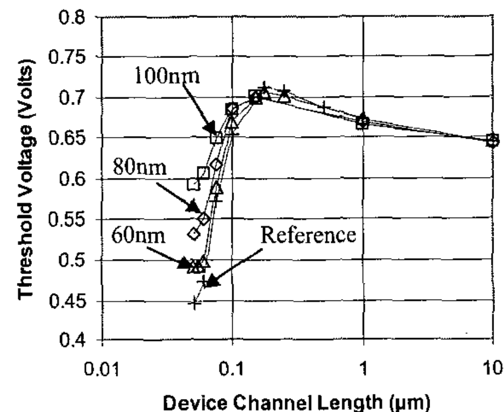

Figure 7. Plot of Threshold voltage vs. channel length for devices with various selective epitaxy silicon layer thicknesses.

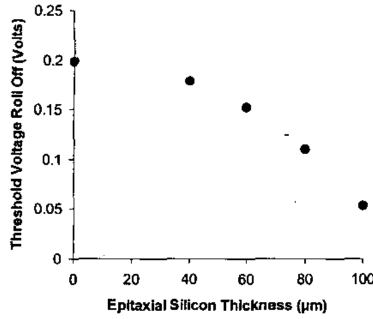

Figure 8. Plot of threshold voltage roll off of 50nm raised source/ drain devices, showing how the threshold voltage roll off is reduced as the thickness of the selective silicon layer is increased.

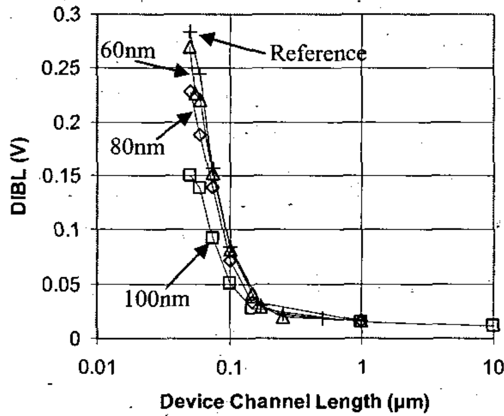

Figure 9. Plot of Vdibl vs. channel length for devices with various selective epitaxy silicon layer thicknesses. Vdibl is the difference in threshold voltage of the devices measured at Vd=0.1V and Vd=1.5V.

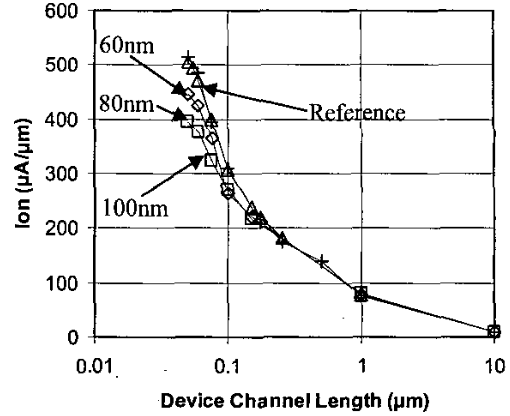

Figure 10. Plot of Ion vs. channel length for devices with various selective epitaxy silicon layer thicknesses. Ion is measured at Vg=Vd=1.5V.

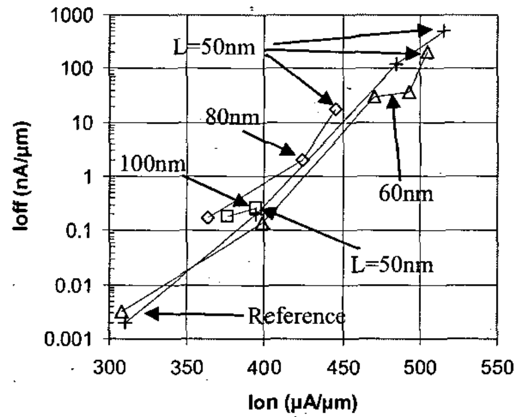

Figure 11. Plot of Ion vs. Ioff for devices with various selective epitaxy silicon layer thicknesses. Ion is measured at Vg=Vd=1.5V, Ioff is measured at Vg=0V, Vd=1.5V. Both Ion and Ioff have been normalised to a device width of 1 micron. Devices with channel length of 50nm are marked on graph.