Source-Gated Transistors for Thin Film Electronics

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Abstract

A new form of thin film transistor named the source-gated transistor (SGT) is described. The current is determined by a source barrier located opposite a gate that controls the effective source barrier height. The SGT has several advantages compared with a standard FET. These include a much lower saturation voltage, higher output impedance and in the case of amorphous silicon, a much better stability.

1. Introduction

Thin film field effect transistors are the basic building blocks for circuits on glass and plastic substrates. They are used extensively in display addressing circuitry and pixel circuits as well as in imaging arrays for optical and x-ray detectors. The most commonly used semiconductor is hydrogenated amorphous silicon but polysilicon is becoming important, as are various semiconducting organic polymers [1]. All the transistors made to date use the field-effect concept in which a voltage applied to the gate modulates the conductance of a channel region [2]. Here we are concerned with a source-gated transistor (SGT) in which the current is controlled by a source barrier the height of which can be modulated by a gate located opposite to the barrier [3].

The source-gated transistor has been shown to have important advantages compared to the standard FET. In particular it can have a very much smaller saturation voltage and therefore it can be operated with a smaller drain voltage and with lower power dissipation.

In this paper, particular attention is paid to the SGT in hydrogenated amorphous silicon (a-Si:H) with a source barrier formed using a metal-semiconductor Schottky barrier. This transistor is relatively easy to make using ion implantation technique to control the source barrier height and provide passivation and field relief [4].

2. Source-Gated Transistor Concept

A general form of SGT is shown in Fig.1. This is a symmetric structure with an ohmic drain contact on either side of a source barrier. The gate lies opposite the source so that it can modulate the whole of the source barrier when a voltage is applied. The current flows over the source barrier to the semiconductor-insulator interface and then laterally to an ohmic drain region. The drain current saturates with drain bias when the semiconductor under the source is depleted by the reverse-biased source barrier. It has been shown that the saturation voltage can be as much as ten times lower than in an FET [4]. This structure is suited to high mobility semiconductors such as polysilicon since the extrinsic drain resistance between the source and the drain contact will be low. In this case the off-state depends on the height of the source barrier and its dependence on drain voltage whilst the on-state is determined by the effect of the gate voltage on the effective barrier height.

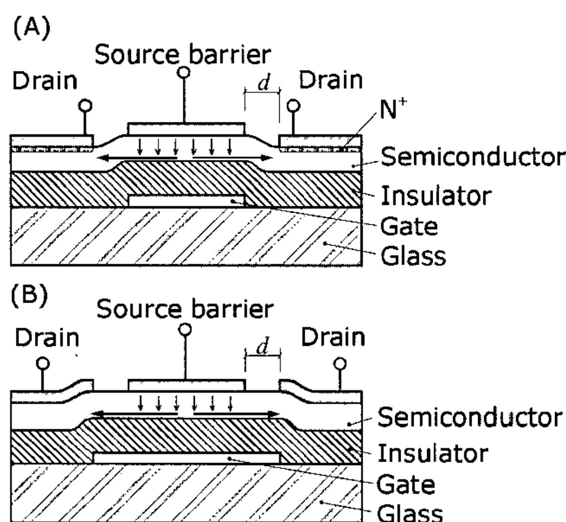

Fig.1. (a) Shows general form of SGT where the gate lies opposite the source barrier and the drain contacts are ohmic; (b) SGT with extended gate in order to minimize the extrinsic drain resistance.

For low mobility semiconductors the extrinsic drain resistance is prohibitive without using conductivity modulation at the semiconductor-insulator interface as in an FET. The structure (Fig.1b) has more parasitic capacitance but low drain resistance. Effectively we now have an SGT in series with an FET of length *d*. The off-state is now determined by the threshold characteristics of the FET whilst the on-state is determined by the characteristics of the SGT. In Fig.1b the drain and source

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contacts are assumed to be Schottky barriers; reverse biased at the source and forward biased at the drain.

3. The SGT in Hydrogenated Amorphous Silicon

Source-gated transistors have been made in hydrogenated amorphous silicon (a-Si:H) using ion implantation technique to control the effective barrier height of a chromium Schottky source barrier and to provide compensation and passivation at the edge of the source contact [4][5]. Since the a-Si:H has a very low mobility, a structure with a modulated extrinsic drain conductivity similar to that schematically shown in Fig.1b was used. The SGT was made using 300nm SiN and 100nm of a-Si:H both deposited on glass using PECVD. The Cr source Schottky barrier was lowered using $1x10^{14}cm^{-2}$ P^{31} at 10kV.

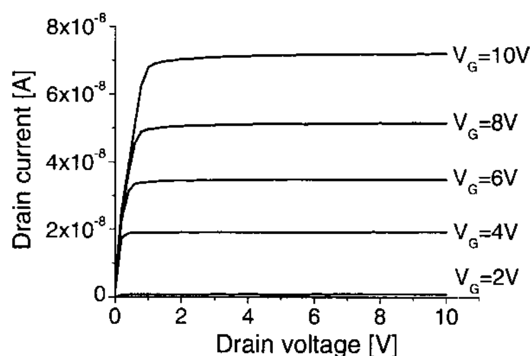

Fig.2. Transistor characteristics of an SGT. The width of the source was 600um.

The SGT transistor characteristics (Fig.2) have excellent characteristics with sharp saturation at voltages (V_{SAT}) very much smaller than found in a conventional FET. At V_G=10V for example V_{SAT} is <1.5 volts. For an FET this corresponds with ≈7V (V_G-V_T). The SGT can therefore be operated in saturation at much lower drain voltages and with smaller power dissipation. Since the characteristics are controlled by the effect of the gate on the source barrier we expect the characteristics to be independent of the separation between the source and drain contacts *d* Fig.1. This is indeed the case as shown in Fig.3 where the saturated drain current at V_G=5, 10, 15 and 20V is plotted against the length *d*. The drain current in an SGT, therefore, scales only with source width *w* whilst for an FET it scales as *w/L* where *L* is the channel length. The linear relationship between saturation current and source width *w* is shown in Fig.4 for four different gate voltages.

The physical processes that determine the output impedance of an SGT are very different from those in an FET. In the SGT the impedance is controlled by field penetration from the drain towards the source barrier when a drain voltage is applied. In the FET there is an effective shortening of the channel with drain voltage, which increases the conductivity of the channel. In the SGT, however, the source is screened by the close proximity of the gate, which should lead to high output impedance. Fig. 5 shows the characteristics of an SGT and an FET in which *d*=*L*=2microns. The same semiconductor and insulator deposition was used in both cases. It is evident from Fig.5 that the output impedance of the SGT is higher the FET which suggests that the SGT should be able preserve its characteristics with smaller dimensions.

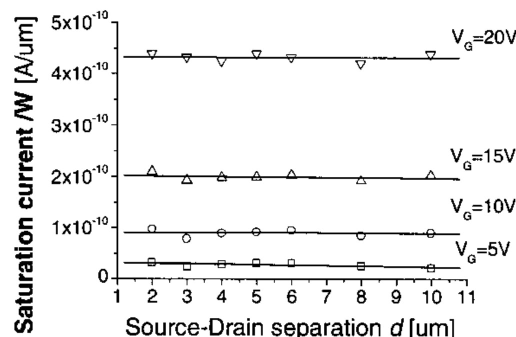

Fig.3. Plot of the normalised saturation current per unit width as a function of source-drain separation *d*.

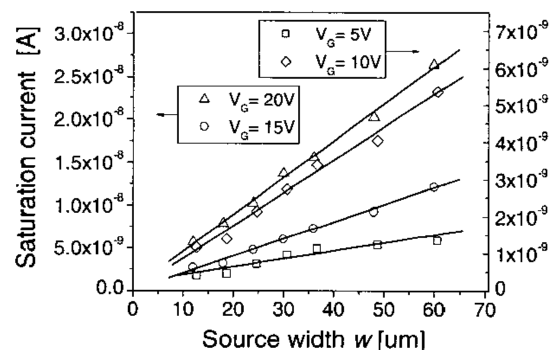

Fig.4. Plot of the saturation current as a function of source width *w*.

The stability of an a-Si:H SGT is also much improved compared to an FET. The instability in a-Si:H is related to the position of the electron quasi-Fermi level in the device during operation and its deviation from the equilibrium level. Changes in the quasi-Fermi level lead to defect generation and trapping and the threshold voltage changes. In general the greater the electron concentration the higher the generation rate. Therefore in the accumulated channel of an FET large numbers of defects are formed while in the depleted source region of an SGT the defect generation rate is small [6]. A comparison between an FET and SGT both stressed in the same way and made using the same semiconductor and insulator layers is shown in Fig.6. The FET shows a large threshold shift due to defect generation as expected. The SGT has some threshold shift when the current is determined by the parasitic FET, however in the on-state, when the current is controlled by the source barrier the device is much more stable than the FET.

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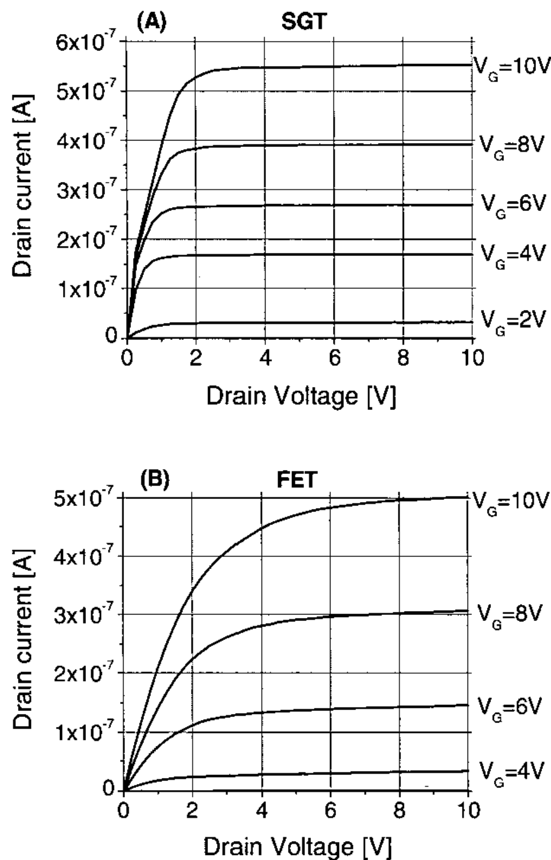

Fig.5. Transistor characteristics of (a) SGT and (b) FET. The source-drain separation d of the SGT and channel length L of the FET was 2um.

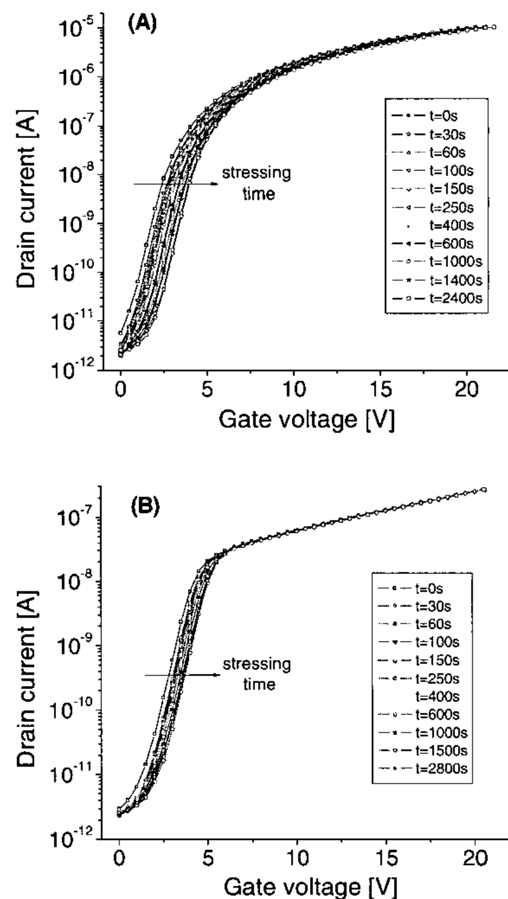

Fig.6. Transfer characteristics of (a) FET and (b) SGT plotted for different stressing times at V_G=20V and T=30°C.

4. Extension to Defective Semiconductors

In principle the SGT does not require doped layers and is relatively easy to make using thin film technology. The SGT is therefore compatible with technologically difficult materials such as plastic and organic polymers. All that is required is a method of obtaining a potential barrier. A further consideration is the benefit of being able to pin the quasi-Fermi level, because trapping and defect generation can be very pronounced in these highly disordered materials leading to instability and hysteresis.

5. Conclusions

It has been shown that the source-gated transistor, a new transistor for thin film electronics, has a number of important advantages over the FET. The SGT is relatively easy to make using thin film technology and lends itself to technologically difficult semiconductors where doping and stability are an issue.

6. Acknowledgement

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